Odin TeleSystems Inc.

Alvis-PCIe
Technical Description

Doc. No. 1111-1-HCA-1021-1

Rev. 1.1

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1   Abstract

This document provides a technical description of Odin TeleSystems' Alvis-PCIe card. This presentation is targeted to systems integrators and application developers who are developing telecommunications systems and/or software applications utilizing the Alvis-PCIe modules together with Odin Telecom frameworX (OTX) Network Interface Cards (NICs). The purpose of this document is to provide the needed information about the hardware to allow software developers to efficiently integrate Alvis-PCIe into their overall system under design.

For information on how to develop host applications utilizing the OTX Hardware Device Driver Application Programming Interface (API), please refer to the "Programmer's Guide for OTX Hardware API" document (Odin TeleSystems Inc. document number 1411-1-SAA-1006-1). For information on how to develop custom DSP applications, please refer to "Programmer's Guide for OTX C64x+ DSP Software Development Kit" (Odin document number 1412-1-SAA-1014-1). And finally, for help on how to install the Alvis-PCIe card and the OTX Device Driver Software, please refer to the Installation Guide for OTX PCI and PCIe Adapters (Odin TeleSystems Inc. document number 1512-1-HCA-1001-1).

2   Alvis-PCIe Overview

The Alvis-PCIe is a member of the Odin Telecom frameworX (OTX) product family. It is supported by the OTX device driver (Window and Linux) and accessed through the OTX Hardware Application Programming Interface (API).

- Alvis-PCIe is available in 4 different options which depend on the number of. Digital Media Processor (DMP) device installed (8, 4 or 1).

The DMP device has a single DM6443 chip containing two cores. One core is a C64x+ DSP code rated at 4752 MIPS. The other core is an ARM9 core clocked at 297 MHz. Both cores share the same memory map and can very efficiently process Digital Media, such as voice and video encoding and decoding.

TDM data can be routed to and from the processors on the Alvis-PCIe board via the time-space switch (TSS) device on the board. After the data has been encoded or decoded by the DSP core of an Alvis processor it can easily be packaged by the ARM9 core (running MontaVista Linux or Windows CE) and transferred to and from the Ethernet port. Ethernet packages are switched locally on the Alvis board and can leave the Alvis board via a 10/100/1000 Ethernet port provided by the Alvic-PCIe board.

The DSP core on the DMP can also be used to run Odin provided standard DSP applications or they can be used to run customized user applications. Alvis-PCIe is delivered with a number of Odin's Standard Program Modules (SPM) that provide supports for many common telecom applications; such as audio and video encoding and decoding, tone detection and generation, and HDLC sending and receiving.

For custom DSP application development, Alvis-PCIe supports the Texas Instruments development tools, such as Code Composer Studio. These tools can be purchased directly from Texas Instruments or from any of their distributors.

For more information on custom DSP application development, please refer to the "Programmer's Guide for OTX C64x+ DSP Software Development Kit" (Odin document number 1412-1-SAA-1014-1).

Equipped with the appropriate OTX software modules, Alvis-PCIe can be utilized in a variety of Voice over IP (VoIP), TVoIP, Soft-switch, Trans-coding and Signaling System #7 (SS#7) applications.

The Alvis-PCIe has an optional I/O extender card available which will allow access to the USB ports as well as provide separate Console ports for each DMP.

3   System Architecture

The overall system architecture can be best described and understood through different architectural views or aspects. This document explores the systems architecture from the following angles:

1.   Physical Specifications View. Provides the dimensions of the board.
2.   External Interface View: The external interface view describes the external interfaces of the adapter board, and how they are connected to the various internal devices and modules.
3.   Data Architecture View: The data architecture view illustrates how the Time - Division Multiplexed (TDM) serial data is connected and transferred through the board.
4.   Control Architecture View: The control architecture view describes how the internal devices and modules can be controlled by the host processor.
5.   Clock Architecture View: The clock architecture view specifies what clocking and synchronization options are available, how clocking is derived, and how it distributed to the various devices.
6.   Logical Subsystem View: The logical subsystem view describes the logical design subsystems in the system. Each subsystem can comprise hardware, firmware and driver or on-board processor software.

It is important to note that one device within the board can be involved in several of these views, each view describing how one aspect of the device interfaces with other devices.

3.1 Physical Specifications

The physical dimensions of Alvis-PCIe and external interfaces are shown in Figure 1.
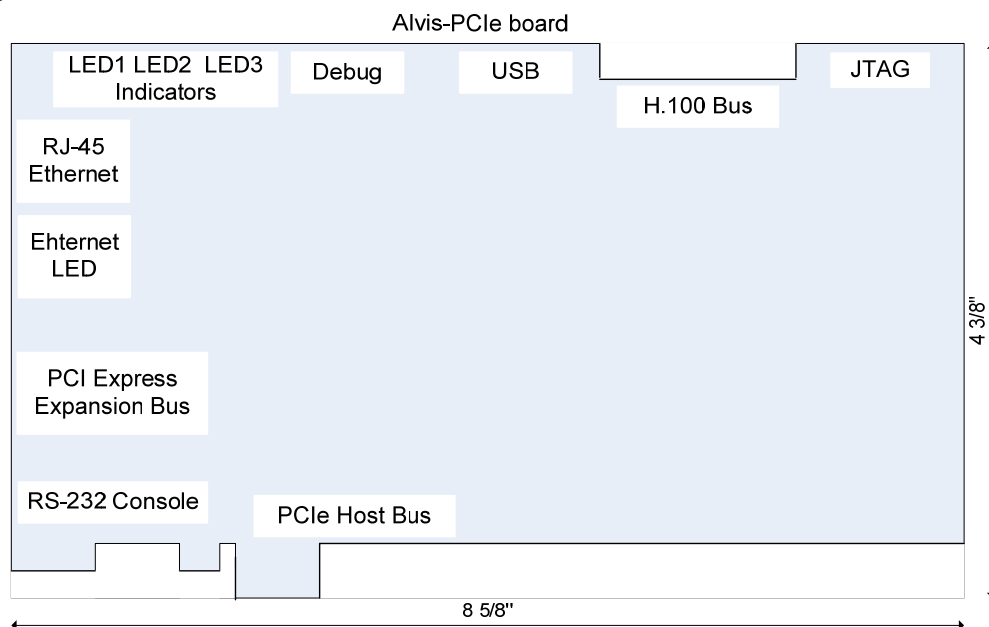
Figure 1

3.2 External Interfaces

- PCIe Host Bus
- RS-232 Consolee
- PCI Express Expansion Bus
- Ethernet 10/100/1000
- LED Indicators
- Debug
- USB
- H.100 Computer Telephony Bus
- JTAG Port for DSP Control

The external interfaces of the Alvis-PCIe card are illustrated in Figure 1.

3.2.1 PCIe Host Bus

1-lane PCI Express (PCIe) to 32-bit, 66MHz generic local bus bridge offers complete protocol translations between these two standards. The PCIe interface conforms to the PCI Express Specification r1.0a.

3.2.2 RS-232 Console

The Console port provides an interface to one of the DMP (DM6443) devices. The port

can monitor any of the eight DMP devices for debug and configuration.

3.2.3   PCI Express Expansion Bus (Optional)

Optional interface used for chassis to chassis communication.

3.2.4   GB Ethernet connector

The Gigabit Ethernet (1000BaseT) connector is accessible via the RJ-45 connector on the board edge connector

The pin out for the GB Ethernet connector is shown in Figure 2 and Table 1.

RJ-45 connector
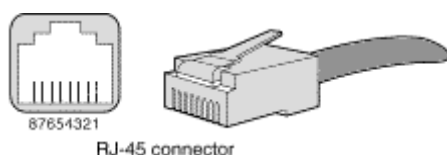
Figure 2

Pin #	Signal Name	Function
1	BI_DA+	Bi-directional pair +A
2	BI_DA-	Bi-directional pair -A
3	BI_DB+	Bi-directional pair +B
4	BI_DC+	Bi-directional pair +C
5	BI_DC-	Bi-directional pair -C
6	BI_DB-	Bi-directional pair -B
7	BI_DD+	Bi-directional pair +D
8	BI_DD-	Bi-directional pair –D

Table 1

Note that the GB Ethernet connector can be connected to legacy Ethernet speeds (100 Mbit/s and 10 Mbit/s) as well as 1000 Mbit/s.

3.2.5   LED Indicators

The LED indicators are defined as:
1. LED1 Power OK
2. LED2 AUX (User defined)
3. LED3 Done (Hardware configuration completed)

3.2.6   Debug (Optional)

The debug port provides the user with access to all eight DMP Console ports using the optional Alvice-PCIe-I/O expander board (HMA-1160-1). Note use of the expansion board will disable the RS-232 Console port provided on the edge connector.

3.2.7   USB (Optional)

The USB connector provides the user access to the eight USB ports one per DMP using the optional Alvice-PCIe-I/O expander board (HMA-1160-1).

3.2.8   H.100 Computer Telephony Bus Interface

Alvis-PCIe supports the H.100 Computer Telephony Bus standard. The H.100 bus is a collection of TDM digital telephony highways designed to carry telephony traffic between extensions boards within one PC chassis. The H.100 bus supports 32 TDM highways. The highways can be operated at 2.048, 4.096, or 8.192 MBit/s carrying 32, 64, or 128 64 kbit/s time-slots, respectively. Up to 20 boards can be connected to one H.100 bus. The maximum distance between boards is 7 inches.

Within the PC chassis the data streams are passed from card to card using a 60 pin ribbon cable and AMP 1-557089-2 connectors. The H.100 connector is a 60-finger edge connector on the upper right-hand side (Figure 1) of the board.

3.2.9   JTAG Connector

The Alvis-PCIe contains several JTAG chains which are used for board testing and board configuration during the manufacturing process. The JTAG chains are accessed from the JTAG connector J8.

TMS#	Devices
TMS0	Other Alvis devices
TMS1	Other Alvis devices
TMS2	DMP0 and DMP1 devices
TMS3	DMP2 and DMP3 devices
TMS4	DMP4 and DMP5 devices
TMS5	DMP6 and DMP7 devices

Table 2

Table 2 shows the JTAG chains that are used on the Alvis-PCIe board. The TMS2-TMS5 chain covers the DMP devices exclusively. A DSP development software with DSP emulator can be connect to chain to facilitate development and debugging of customized DSP applications. To connect to the standard 13-pin JTAG connector from the DSP emulator to the OTX NIC board, the Hermod-JTAG adapter board (HMA-1057-1) is needed. The Hermod-JTAG board plugs onto the JTAG connector of the OTX card, and the DSP Emulator connects to the Hermod-JTAG board.

3.3   Data Architecture

The Alvis-PCIe provides each of the DMP devices access to transfer data via Ethernet packets and via serial TDM data streams. The serial TDM data streams are referred to as "Highways." The serial highways provide data paths between physical devices as shown in Figure 3.
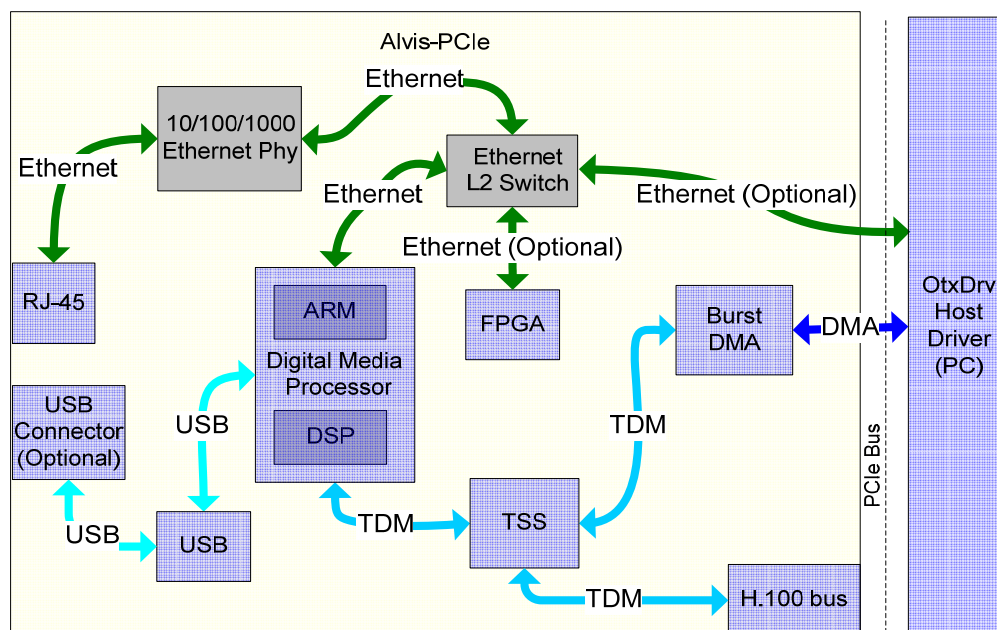
Figure 3

3.3.1   TDM Data Path

The OTX TDM highways run at 3 different speeds (2.048 Mbps, 4.096 Mbps, or 8.192 Mbps) depending on the architecture of the OTX NIC Base card. In the case of a Alvis-PCIe all the highways run at 8.192 Mbps See Figure 3 shows the physical TDM highways.

TDM connections (pipes) are made using the standard OtxDrvConnectPipe() OTX API function.

The TSS highway numbers are used when the TSS pipe connection method is used (see the OTX Programmers Guide). See Table 3 for the highway numbers used on the Alvis-PCIe board.

TSS HWY#	Devices	TSS HWY#	Devices
TSS HWY0	DMP0 device	TSS HWY8	Burst device Hwy 0
TSS HWY1	DMP1 device	TSS HWY9	Burst device Hwy 1
TSS HWY2	DMP2 device	TSS HWY10	Reserved (not used)
TSS HWY3	DMP3 device	TSS HWY11	Reserved (not used)
TSS HWY4	DMP4 device	TSS HWY16	H.100 bus Hwy 0
TSS HWY5	DMP5 device	TSS HWY17	H.100 bus Hwy 1
TSS HWY6	DMP6 device	TSS HWY18	H.100 bus Hwy 2
TSS HWY7	DMP7 device	TSS HWY19	H.100 bus Hwy 3

Table 3

Note that when Device-Device connections are used the OTX Driver will automatically connect (and pick the correct time-space path) between two devices on the board (in this case a DMP0 device and a DMP7 device). Please note that the devices can even be located on different OTX boards in the host system. In that case the OTX driver will choose a timeslot over the H.100 bus and make the proper connections in both TSS devices (of each of the OTX boards).

3.3.2   Packet Data Path

The data packets travel via an internal Ethernet network on the Alvis-PCIe card. The packets are switched by an on-board L2 Ethernet switch device (OTX_DEVICE_ETHERNET_SWITCH) that offers the following support:

- L2 switching with self learning (up to 4k MAC addresses). The switch also supports IP multicast address learning, and IP Multicast with IGMP snooping (up to 4k IP Multicast groups).
- Supports jumbo frames of up to 4k in size.
- Provides the ability to monitor a link, detect a simple link failure, and provide notification of the failure to the Host PC. The application on the Host PC can then failover that link to an alternate link.
- Supports the following spanning standards: IEEE 802.1D spanning tree and IEEE 802.1w rapid spanning tree.
- Ethernet multicasting and broadcasting and flooding control
- Provides powerful QoS functions for various multimedia and mission-critical applications using strict priority and/or WFQ transmission scheduling and WRED dropping schemes. The device provides 2 transmission priorities (4 priorities for uplink port) and 2 levels of dropping precedence. Each packet is assigned a transmission priority and dropping precedence based on the VLAN priority field in a VLAN tagged frame, or the DS/TOS field, or the UDP/TCP logical port fields in IP packets.

Data packets that have a non-Alvis destination are routed to the 10/100/1000 Ethernet PHY on Alvis-PCIe card. It is connected via the card to a standard RJ-45.

3.4   Control Architecture

The PCIe Interface provides 32-bit processor bus, which is used by the host PC to control the physical and logical devices on the Alvis-PCIe board. This interface offer functions to load programs into the DSP core, ARM core and to the persistent NAND flash memory.

A subset of the control functions are listed below:

- OtxDmpRunCodecEngineServer() - Load and Run a Codec Engine Server on a the ARM core from a formatted program file.
- OtxDmpRunStandardProgramModule() - Load and Run an OTX SPM on the DSP core from a program image stored in the OTX library.
- OtxDmpIoControl() - Send a user command to a DMP application.
- OtxDmpReadData() - Read data from a DMP application
- OtxDmpUploadFile() – Upload a file to the ARM core file system
- OtxDmpDownFile() – Download a file from the ARM core file system

- OtxDmpSetNetworkParams() –
- OtxDmpRunStandaloneProcess() -
- OtxDmpKillStandaloneProcess() -

3.5 Clock Architecture

All the internal TDM data highways and all the devices processing TDM data on the Alvis-PCIe board are synchronized to one clock reference. The clock reference can be derived from two sources and then switched to all the devices. The Alvis-PCIe board supports an internal clock mode (master) or an external clock mode (slave) provided by the H.100 bus. The H.100 bus requires a single card to provide the clocks all other cards will synchronize to this clock source.

3.6 Logical Subsystem

The logical subsystem view describes the logical design subsystems within the Alvis-PCIe board. Each subsystem can comprise hardware, firmware, and driver or on-board processor software. The Alvis-PCIe comprises of only one subsystem:

- Processor Subsystem
- Packet switching Subsystem
- Host-PC Communication Subsystem

3.6.1 Processor Subsystem

The processor subsystem on the Alvis-PCIe board contains between one and eight Texas Instruments TMS320DM6443 Digital Media Processors (DMP). These processors are sometimes also referred to as "System On Chip" since they are equipped with two different cores; one DSP C64x+ core and one ARM9 core.

The DSP core is clocked at 597 MHz and with an 8 lane wide instruction cache it is rated at 4752 C64x+ MIPS. The ARM9 core is clocked at 297 MHz.

Each DMP is connected to 256 Mbytes of DDR2 memory and a 64 MByte NAND Flash memory device for persistent storage. Both the DSP core and the ARM core share access to the memory devices. Both cores operate in the same memory space.

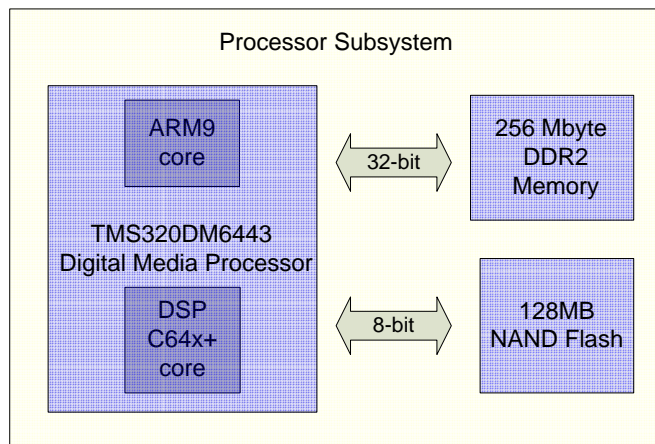The processor subsystem is depicted in Figure 4.

Figure 4

In addition, the processor subsystem provides LEDs (two per DMP) which can be turned on and off under DMP software control. The LEDs are typically used as heart-beat indicators (blinked on and off by the DMP applications) or displaying other custom status indications. There is also a Power-Good LED indicating that the DMP is powered adequately to function properly.

3.6.2   Packet Switching Subsystem

The heart of the packet switching subsystem is the OTX_DEVICE_ETHERNET_SWITCH device which switches Ethernet packets between the different Ethernet MACs on the Alvis-PCIe board. It also switches Ethernet packets to and from the 10/100/1000 Ethernet PHY, which can be connected to the internet, LAN, or a WAN.

The Packet Switching Subsystem on the Alvis-PCIe board is shown in Figure 5.
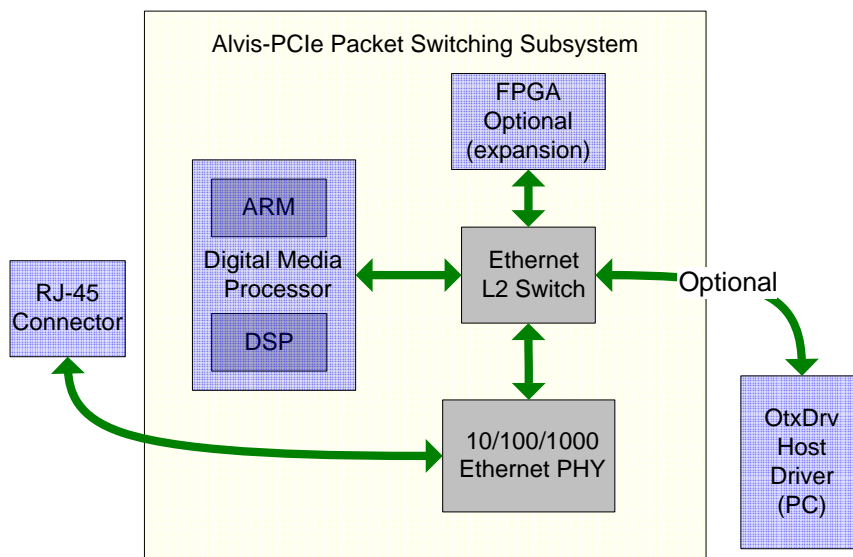
Figure 5

3.6.3 Host PC Communication Subsystem (Optional)

The Host PC communicates with the devices on the Alvis-PCIe board via its Host PC Communication Subsystem. An application that runs in User Mode on the Host PC can send commands and receive events from the Alvis devices via the API functions in the OTX Hardware API. The communication path goes via OTX HW Driver, the OTX NIC Board and the FPGA on the Alvis-PCIe board. Figure 6 illustrates this communication path.

Figure 6

4   API Supported Devices

4.1   Physical Devices

4.1.1   Digital Media Processor (DMP) Device (OTX_DEVICE_DMP)
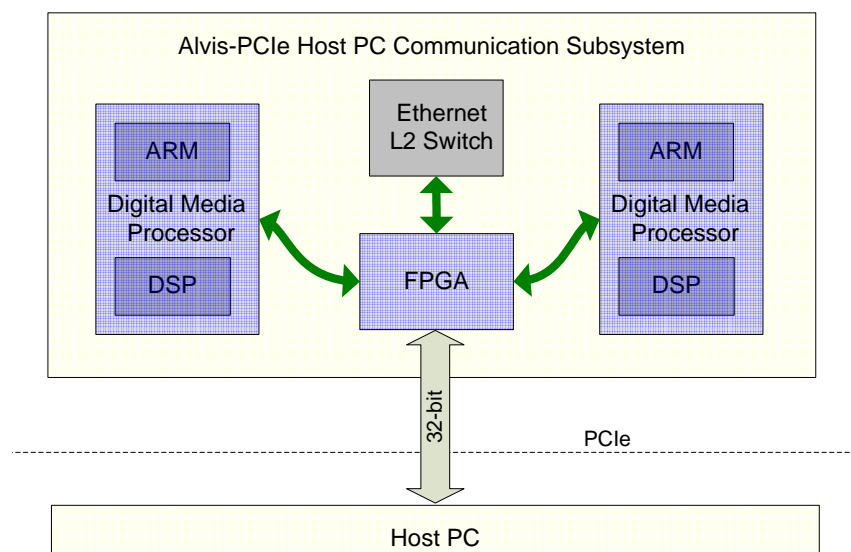
The Alvis-PCIe boards hosts a number of Digital Media Processor devices
OTX_DEVICE_DMP). The number of DMP devices that are hosted by the board varies
with the different Alvis-PCIe board options (1, 2, and 4).

The sequence number of the first DMP device is 0 (zero) and increases by one for every
DMP devices that is populated on the board.

When a DMP device is opened it is booted into its standard configuration. The boot
image can be changed using the OtxDmpUploadFile() API function. The Boot image is
stored in a persistent NAND flash device on the Alvis-PCIe board.

The DMP device has two cores:

- ARM9 core
- DSP C64x+ core

The ARM9 core runs either Linux or Windows CE as its operating systems. The ARM
core can run standard OTX libraries such as OTXRTP and OTXHDLC. It is also possible
to run custom supplied libraries and applications.

The ARM9 core also controls the DSP core. It loads the DSP program into memory
region for the DSP and then executes the program.

The DSP core of the DMP devices on the Alvis-PCIe can also be used to run the Standard
Program Modules (SPMs) provided in the OTX SDK library. These SPMs, or DSP
application packages, provides supports for many common telecom applications; such as
tone detection and generation, FSK, and HDLC sending and receiving.

The DSP core can also be used to run user developed custom applications. For more
information on custom DSP application development, please refer to "Programmer's
Guide for OTX C64x DSP Software Development Kit" (Odin document number 1412-1-
SAA-1014-1).

4.1.2   Ethernet Switch Device (OTX_DEVICE_ETHERNET_SWITCH)

The Ethernet switch device (OTX_DEVICE_ETHERNET_SWITCH) handles the data
packets between the DMP devices, the FPGA, and the external Ethernet PHY devices on
the Alvis-PCIe board. It is optional to open this device. The Alvis-PCIe board will
automatically switch Ethernet packets even if this device is not open. Only if an
application wishes to override the standard Ethernet switching behavior (such as enabling
the Traffic Mirroring feature) this device should be opened.

The sequence numbers of this device is always zero (0).

For more information regarding the Ethernet switch device please see chapter 3.3.2.

4.1.3   Burst Device (OTX_DEVICE_BURST)

The Alvis-PCIe board contains a Direct Memory Access (DMA) system allowing the user to send two 8 MHz highways of data directly into and from the host PC's memory. This greatly reduces the host CPU time required for data transfer to or from the host. The TSS can be used to cross-connect the DMA system into any incoming or outgoing time-slot to the DMP, or H.100 Highways.

4.2   Logical Devices

The Alvis-PCIe board supports a number of logical devices depending on which Codec Engine Server and which Standard Program Module that is loaded into the DSP core.

A subset of the supported devices is listed below:

- OTX_LDEVICE_VOICE_CODEC_G723_ENCODER – logical device that compresses (encodes) voice audio in 30 ms frames according to the ITU-T G.723.1 codec standard. G.723.1 is commonly used in Voice over IP (VoIP) applications.
- OTX_LDEVICE_VOICE_CODEC_G723_DECODER – logical device that decodes voice audio according to the ITU-T G.723.1 standard.
- OTX_LDEVICE_VOICE_CODEC_G729_ENCODER – logical device that support audio data compressing (encoding) according to the ITU G.729 algorithm (Annex A and B). Operates at 6.4 kbps, 8 kbps, and 11.8 kbps. G.729AB is commonly used in Voice over IP (VoIP) applications.
- OTX_LDEVICE_VOICE_CODEC_G729_DECODER - logical device that support audio data decoding according to the ITU G.729 algorithm (Annex A and B).
- OTX_LDEVICE_TONE_DTMF_DIALER – logical device that generates DTMF dial tone sequences.
- OTX_LDEVICE_TONE_MF_DIALER - logical device for generating MF tone sequences.
- OTX_LDEVICE_TONE_DTMF_DETECTOR - logical device for detecting DTMF tones.
- OTX_LDEVICE_TONE_MF_DETECTOR - logical device for detecting MF tones.
- OTX_LDEVICE_TONE_DATA_HDLC_SENDER - logical device for sending (encoding) HDLC frames.
- OTX_LDEVICE_TONE_DATA_HDLC_RECEIVER - logical device for receiving (decoding) HDLC frames.

5   Power

Board power is provided by the PCIe host interface.

6 Certifications

Final certifications are TBD. The Alvis-PCIe will be designed with the following list of planned certifications:

- FCC Part 15 (CFR47, Part 15, Subpart B)
- CE EMC (EN61326-1 Class B Equipment, AS/NZS 2064 Class B Limits)
- Safety EN60950 and UL60950

7 Reference documents

The following documents provide further detailed information related to the Alvis-PCIe board:

- Programmer's Guide for OTX Hardware Driver (Odin document # 1412-1-SAA-1006-1)
- Installation Guide for OTX PCI Adapters (Odin document number 1512-1-HCA-1001-1)
- Programmer's Guide for OTX C64x+ DSP Software Development Kit (Odin document number 1412-1-SAA-1014-1)
- Alvis-PCIe Product Brief (Odin document number 2020-1-HCA-1018-1)

8 Glossary

- API – Application Programmer Interface
- CPU – Central Processing Unit. Refers to the host PC in this document
- DMA - Direct Memory Access
- DMP – Digital Media Processor. Refers to the dual core System On Chip processors on the Alvis board.
- DSP – Digital Signal Processor
- EEPROM – Electrically Erasable Programmable Read Only Memory.
- FPGA – Field Programmable Gate Array.
- LED – Light Emitting Diode
- LS – Least Significant
- NIC – Network Interface Card. Refers to the OTX Base board that this ASM board is connected to. Examples of OTX NIC cards are Thor-8-PCI-Plus, Thor-2-PCI-Plus, and Thor-2-PCI-Express.
- MS – Most Significant
- OTX – Odin Telecom FrameworX
- PCIe - PCI Express
- SDK – Software Development Kit
- SPM - Standard Program Modules
- TDM - Time - Division Multiplexed
- TSS - Time-Space Switch