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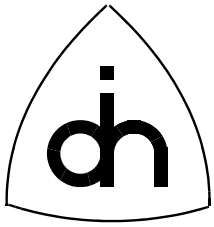

Technical Description for Thor-2-PCMCIA+

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Odin TeleSystems Inc.
http://www.OdinTS.com

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Odin TeleSystems Inc.
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1. Abstract

This document provides a technical description of Odin TeleSystems' Thor-2-PCMCIA-Plus adapter card. This presentation is targeted to systems integrators and application developers who are developing telecommunications systems and/or software applications using the Thor-2-PCMCIA-Plus platform. The purpose of this document is to provide the needed information about the hardware to allow software developers to efficiently integrate Thor-2-PCMCIA-Plus into their overall system under design.

For information on how to develop host applications utilizing the OTX Hardware Device Driver Application Programming Interface (API), please refer to the "*Programmer's Guide for OTX Hardware API"* document (Odin TeleSystems Inc. document number 1411-1-SAA-1006-1). For information on how to develop custom DSP applications, please refer to "*Programmer's Guide for OTX C54x DSP Software Development Kit"* (Odin document number 1412-1-SAA-1007-1). And finally, for help on how to install the Thor-2-PCMCIA-Plus card and the OTX Device Driver Software, please refer to the *Installation Guide for OTX PCMCIA Adapters* (Odin TeleSystems Inc. document number 1512-1-HCA-1003-1).

2. Table of Content

3. Introduction to Thor-2-PCMCIA-Plus

Thor-2-PCMCIA-Plus is multi-purpose T1/E1 interface adapter. The Thor-2-PCMCIA-Plus card allows laptops, hand-held PCs, and other portable devices with a PCMCIA slot to be interfaced with T1/E1 links.

Thor-2-PCMCIA-Plus is a member of the Odin Telecom frameworX (OTX) product family. Thor-2-PCMCIA-Plus is supported by the OTX device driver and by the OTX Hardware Application Programming Interface (API). Equipped with the appropriate OTX software modules, the Thor-2-PCMCIA-Plus can be utilized in a variety of T1/E1, Integrated Services Digital Network (ISDN), Frame Relay, and Signaling System #7 (SS#7) applications. The ideal uses for Thor-2-PCMCIA-Plus include mobile network testing, surveillance, and maintenance applications.

The Thor-2-PCMCIA-Plus supports two T1 or E1 interfaces at the speeds of 1.544 Mbps and 2.048 Mbps, respectively. Throughout the document the T1/E1 interfaces are referred to as Line Interfaces (LIs). The same board supports both T1 and E1. The operation mode as well as the line terminating impedance of 75 ohms or 100/120 ohms are software switchable.

The card also has support for a 20dB amplifier in each dongle which can be turned on (via software) for monitoring of an T1/E1 span through an attenuated monitor port. A high-impedance mode is available as well for a bridged monitoring scenario.

Consequently, the Thor-2-PCMCIA-Plus card can be used to terminate two T1/E1 links or to monitor one link.

Thor-2-PCMCIA-Plus also contains two on-board Digital Signal Processors (DSPs). The DSPs used are Texas Instruments TMS 320C549 with 120 MIPS (Million Instructions Per Second) processing power each. By loading and running different programs in the DSP, the Thor-2-PCMCIA-Plus adapter can support a variety of different telecom functions, such as tone detection and generation, HDLC sending and receiving, voice encoding and decoding, etc.

4. Specifications

Thor-2-PCMCIA-Plus is a PCMCIA type II card. The physical dimensions of Thor-2-PCMCIA-Plus are shown in Figure 1.

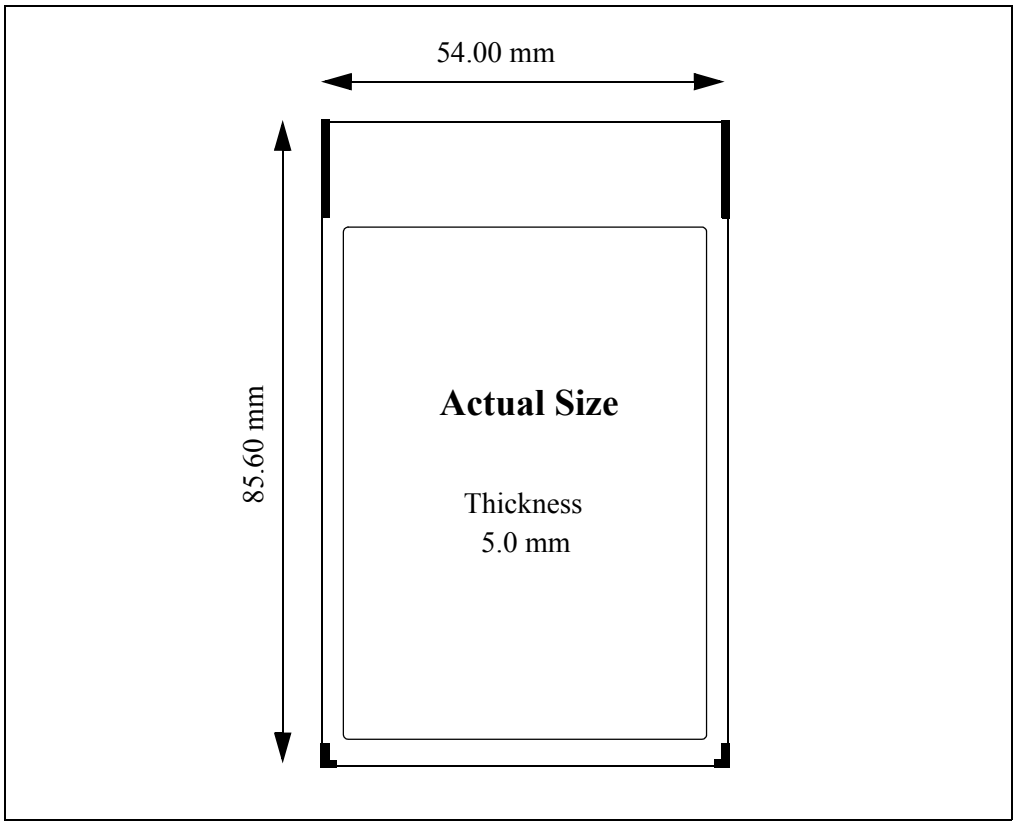

Figure 1. Thor-2-PCMCIA-Plus Physical Dimensions.

The Thor-2-PCMCIA-Plus operates with +5.0 V supply voltage.

5. Supported Driver Devices

5.1 Physical Devices

The Thor-2-PCMCIA-Plus supports the following physical API driver devices:

TABLE 1. OTX Physical Driver Devices supported by Thor-2-PCMCIA-Plus

Host Device	Device Type	Max #	Description
0	*OTX_DEVICE_THOR_PCMCIA*	1	Board Device
OTX_DEVICE_THOR_PCMCIA	*OTX_DEVICE_LI_T1E1*	2	T1/E1 Line Interface Devices
OTX_DEVICE_THOR_PCMCIA	*OTX_DEVICE_DSP*	2	TI TMS320C549 Digital Signal Processors

5.2 Logical Devices

The Thor-2-PCMCIA-Plus supports the following logical API driver devices:

TABLE 2. OTX Logical Driver Devices supported by Thor-2-PCMCIA-Plus

Host Device	Device Type	Max #	Description
OTX_DEVICE_LI_T1E1	*OTX_LDEVICE_HDLC_SENDER*	1	Logical Device for sending Hdlc Framing
OTX_DEVICE_LI_T1E1	*OTX_LDEVICE_HDLC_RECEIVER*	1	Logical Device for receiving Hdlc framing.

In addition, the DSPs can be loaded with various program packages to provide support for a variety of Logical Devices types. For example, the Signal Processing Package One (OtxSpm1) provides support for the following API logical devices:

- *OTX_LDEVICE_TONE_CONST_VAL_GENERATOR*
- *OTX_LDEVICE_TONE_EFFECTS_GENERATOR*
- *OTX_LDEVICE_TONE_SINEWAVE_GENERATOR*
- *OTX_LDEVICE_TONE_DTMF_GENERATOR*
- *OTX_LDEVICE_TONE_DTMF_DIALER*
- *OTX_LDEVICE_TONE_SILENCE_DETECTOR*
- *OTX_LDEVICE_TONE_DTMF_DETECTOR*
- *OTX_LDEVICE_DATA_CONVERTER*
- *OTX_LDEVICE_HDLC_SENDER*
- *OTX_LDEVICE_HDLC_RECEIVER*

For mode information on the physical and logical driver devices, please refer to "*Programmer's Guide for OTX Hardware API"* (Odin document # 1412-1-SAA-1006-1).

6. System Architecture

The overall system architecture can be best described and understood through different architectural views or aspects. This document explores the systems architecture from the following angles:

1. **External Interface View:** The external interface view describes the external interfaces of the adapter board, and how they are connected to the various internal devices and modules.

2. **Data Architecture View:** The data architecture view illustrates how the Time - Division Multiplexed (TDM) serial data is connected and transferred through the board.

3. **Control Architecture View:** The control architecture view describes how the internal devices and modules can be controlled by the host processor.

4. **Clock Architecture View:** The clock architecture view specifies what clocking and synchronization options are available, how clocking is derived, and how it distributed to the various devices.

5. **Logical Subsystem View:** The logical subsystem view describes the logical design subsystems in the system. Each subsystem can comprise hardware, firmware and driver or on-board processor software.

It is important to note that one device within the board can be involved in several of these views, each view describing how one aspect of the device interfaces with other devices.

6.1 External Interfaces

The Thor-2-PCMCIA-Plus contains the following external interfaces:

- PCMCIA Bus
- 2 T1/E1 Line Interfaces

The external interfaces of the Thor-2-PCMCIA-Plus card are illustrated in Figure 2.

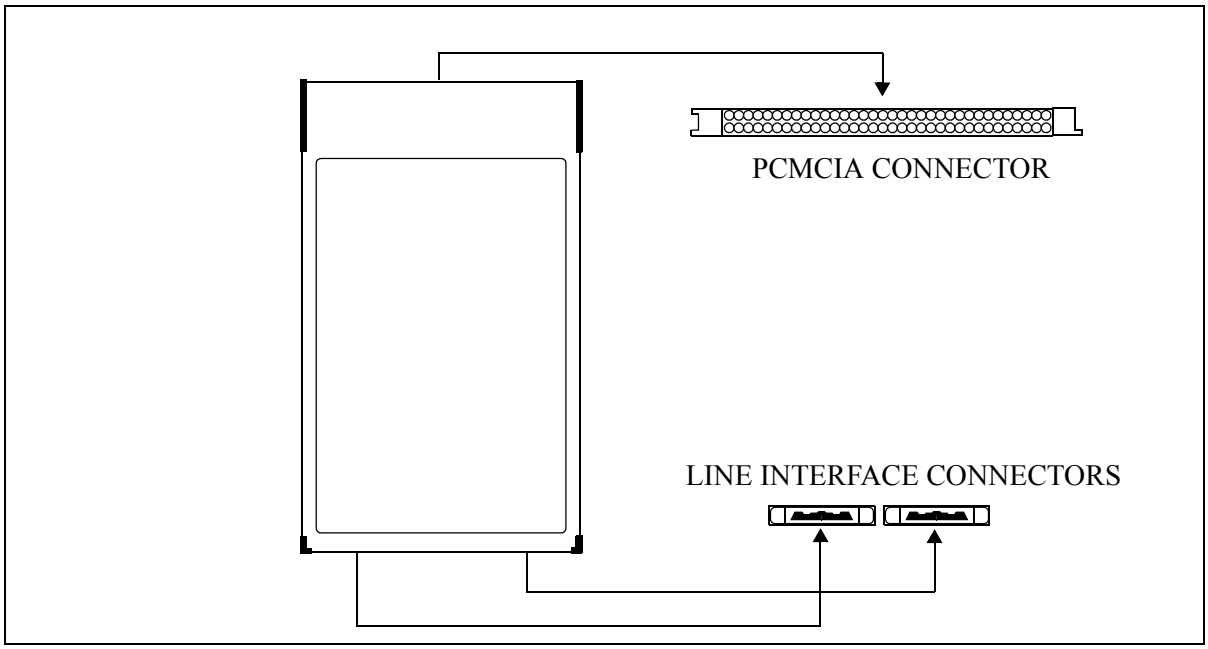

Figure 2. OTX PCMCIA External Interfaces.

6.1.1 PCMCIA Bus Interface

The electrical interface between the Thor-2-PCMCIA-Plus board and the PCMCIA Host Bus Adapter (HBA) is a 68-pin connector specified by the PCMCIA standard. The pin-out of the PCMCIA connector is shown in Figure 3 and the pins are described in Table 3.

Figure 3. Standard (+5V) PCMCIA Card and Socket Keying Interface.

TABLE 3. PCMCIA Standard Connector Pin-Out

#	Name	#	Name	#	Name	#	Name
1	Ground	2	Data 3	3	Data 4	4	Data 5

TABLE 3. PCMCIA Standard Connector Pin-Out

#	Name	#	Name	#	Name	#	Name
5	Data 6	6	Data 7	7	CE1#[1]	8	Address 10
9	OE#[2]	10	Address 11	11	Address 9	12	Address 8
13	Address 13	14	Address 14	15	WE#[3]	16	IREQ#[4]
17	Vcc	18	Vpp1	19	Address 16	20	Address 15
21	Address 12	22	Address 7	23	Address 6	24	Address 5
25	Address 4	26	Address 3	27	Address 2	28	Address 1
29	Address 0	30	Data 0	31	Data 1	32	Data 2
33	IOIS16#[5]	34	Ground	35	Ground	36	CD1#[6]
37	Data 11	38	Data 12	39	Data 13	40	Data 14
41	Data 15	42	CE2#	43	VS1#	44	IORD#[7]
45	IOWR#[8]	46	Address 17	47	Address 18	48	Address 19
49	Address 20	50	Address 21	51	Vcc	52	Vpp2
53	Address 22	54	Address 23	55	Address 24	56	Address 25
57	VS2#	58	RESET	59	Wait#	60	INPACK
61	REG#	62	SPKR#	63	STSCHG#	64	Data 8
65	Data 9	66	Data 10	67	CD2#	68	Ground

1. Card Enable 1
2. Output Enable for Memory Access
3. Write Enable for Memory Access
4. Interrupt Request
5. 16-bit I/O access
6. Card Detect 1
7. I/O Read
8. I/O Write

For more information on the PCMCIA Interface, please refer to the appropriate PCMCIA standards.

6.1.2 T1/E1 Line Interfaces

The back edge of the Thor-2-PCMCIA-Plus contains two 15-pin connectors for:

- Two T1/E1 interfaces
- JTAG Boundary Scan interface for board testing
- DSP Emulation Interface for DSP Software Development Tools
- Input for External Synchronization Clock
- Output of Used synchronization clock
- Control signals for switching line termination

The connector pin-outs for Line Interface #0 (LI-0) and Line Interface #1 (Li-1) are listed in Table 4.

TABLE 4. Thor-2-PCMCIA-Plus Network Connector Pin-out.

#	LI-0 Connector		LI-1 Connector	
	Pin Name	**Description**	**Pin Name**	**Description**
1	NC	Not Connected	NC	Not Connected
2	20DB	20 dB Amplifier control	20DB	20 dB Amplifier controld
3	XL1	Transmit Line 1 (tip)	XL1	Transmit Line 1 (tip)
4	XL2	Transmit Line 2 (ring)	XL2	Transmit Line 2 (ring)
5	E1_75	75 ohm balanced control	E1_75	75 ohm balanced control
6	GND	Ground	GND	Ground
7	RL1	Receive Line 1 (tip)	RL1	Receive Line 1 (tip)
8	RL2	Receive Line 2 (ring)	RL2	Receive Line 2 (ring)
9	100OHM	100 ohm control	100OHM	100 ohm control
10	VCC	+5V Supply Voltage	VCC	+5V Supply Voltage
11	TDI	JTAG Test Port Data In	CLKIN	External Synch Clock In
12	TRST	JTAG Test Port Reset	EMU0	DSP Emulation Port 0
13	TMS1	JTAG Test Port Chain 1	TMS0	JTAG Test Port Chain 0
14	EMU1	DSP Emulation Port 1	TDO	JTAG Test Port Data Out
15	CLKOUT	Sych Clock Out	TCLK	JTAG Test Port Clock

Thor-2-PCMCIA-Plus is delivered with two dongles which are used to connect the board to actual T1/E1 lines. The dongles contain the protection circuitry designed to protect both the adapter and the host PC from power surges and currency spikes possibly transported through the network interfaces. The dongles connect to the board with 15-pin board connectors and provide a RJ-45 connector for the external T1/E1 links, as illustrated in Figure 4.

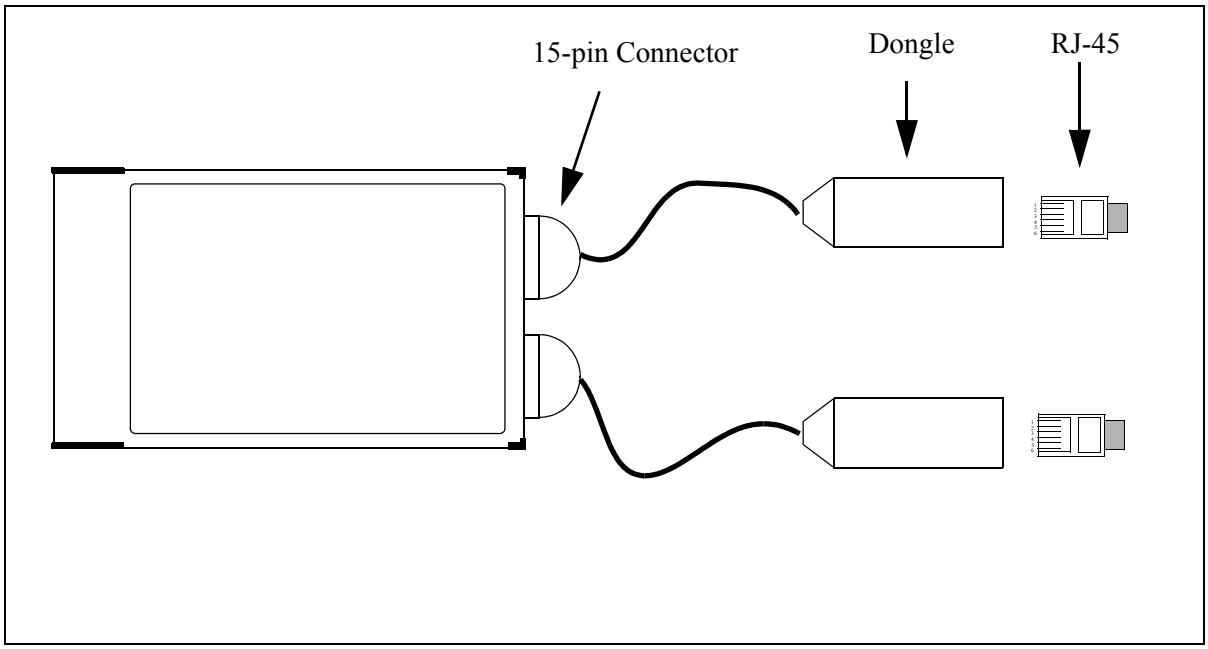

Figure 4. Thor-2-PCMCIA-Plus External Line Interface Connectors.

The dongle RJ-45 pin-outs for the 4-wire T1/E1 line interfaces are shown in Figure 5.

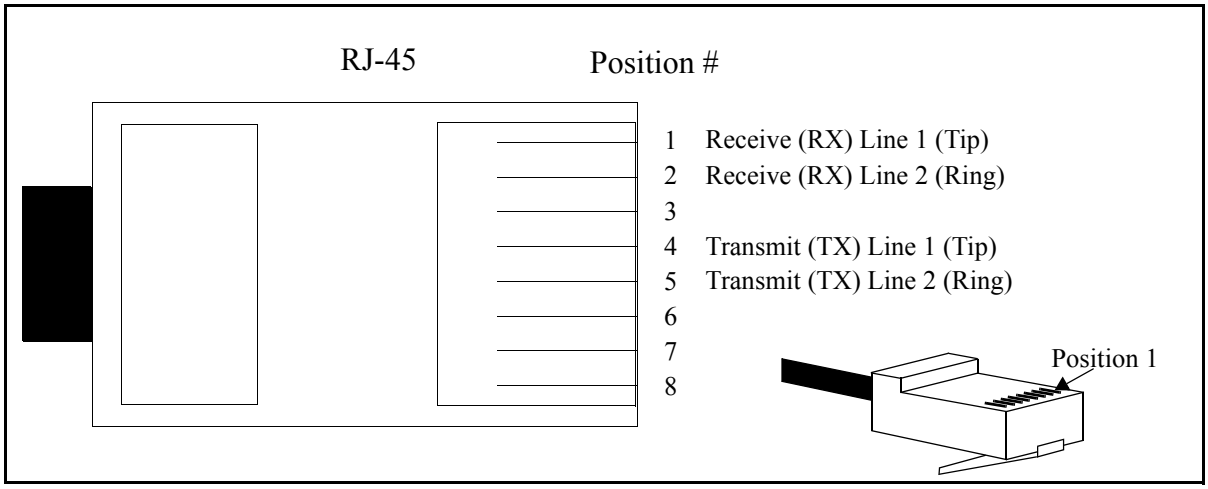

Figure 5. RJ-45 Connector for the T1 or E1 Interface.

The board and the dongles also support switching of the T1/E1 line termination. The switching is software controlled and the supported line terminations are:

- 75 Ohms
- 100/120 Ohms

- High Impedance

6.2 Data Architecture

Internally, Thor-2-PCMCIA-Plus utilizes serial TDM (Time-Division Multiplexed) data streams for transfer of data or voice. The internal serial TDM data streams are called “Highways.” External interfaces are called spans.

The serial highways provide data paths between physical devices as shown in Figure 6. If the physical device connects to more than one highway, the device specific highway port number is also shown in Figure 6.

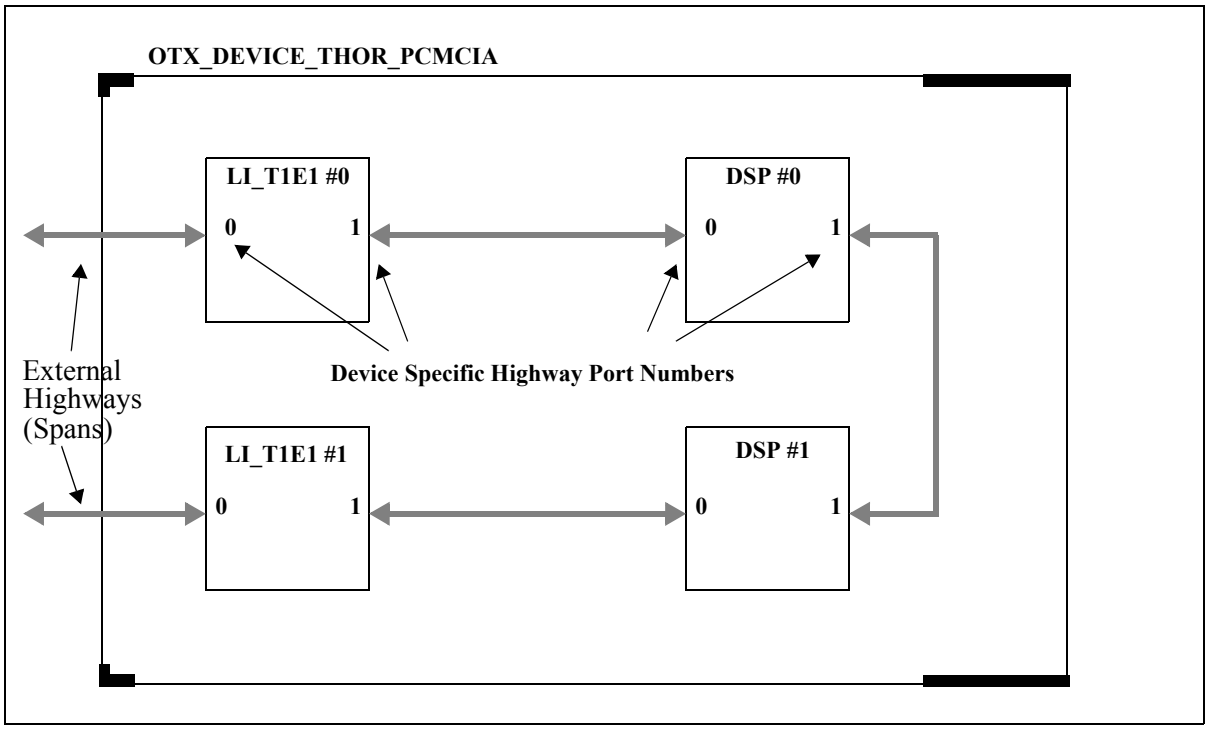

Figure 6. Thor-2-PCMCIA-Plus Highway Connections.

6.3 Control Architecture

The host PC can controlled the physical devices on the Thor-2-PCMCIA-Plus board through the PCMCIA bus. The Thor-2-PCMCIA-Plus control architecture is illustrated in Figure 7.

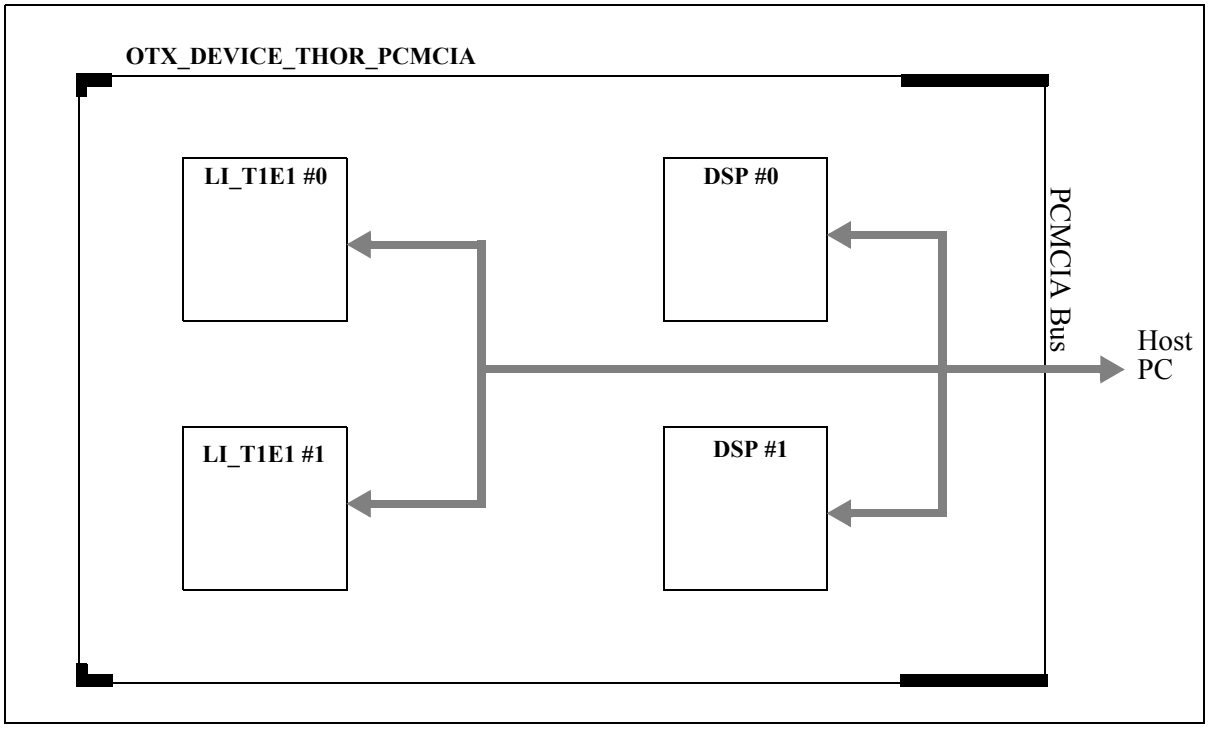

Figure 7. Thor-2-PCMCIA-Plus Control Architecture.

6.4 Clock Architecture

On Thor-2-PCMCIA-Plus all the internal TDM data highways and the all the devices processing TDM data are synchronized to one clock reference. The clock reference can be derived from multiple sources and then switched to all the devices. The used clock is also available to clock external equipment through the one of the 15-pin board connectors (Table 4). The clocking sources supported by Thor-2-PCMCIA-Plus are illustrated in Figure 8 and listed in Table 5.

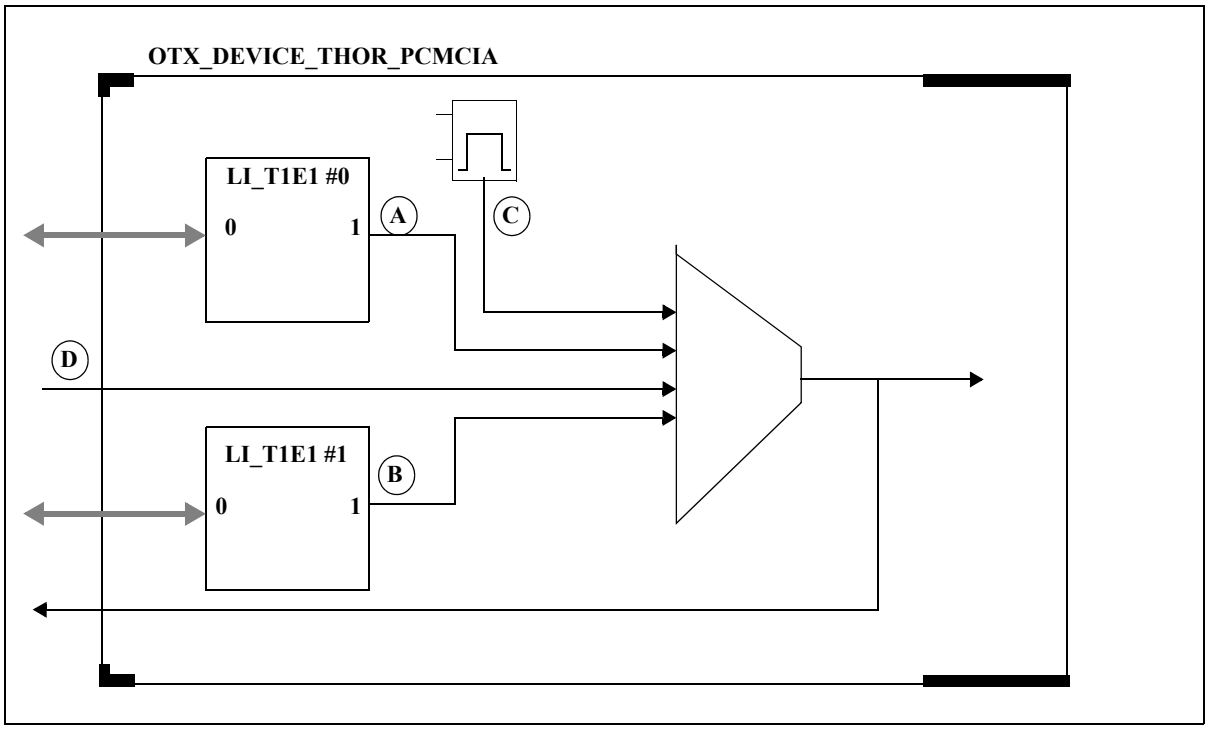

Figure 8. Thor-2-PCMCIA-Plus Clock Architecture Overview.

TABLE 5. Thor-2-PCMCIA-Plus Clocking Sources.

Clock Source	Description
A	8 kHz frame clock extracted from the incoming T1/E1 span 0 (LI-0).
B	8 kHz frame clock extracted from the incoming T1/E1 span 1 (LI-1).
C	On-board free running oscillator.
D	External 8 kHz framing clock
E	Split clock. LI-0 and LI-1 are operating independently extracting clocks from their individual spans.

6.5 Logical Subsystems

The logical subsystem view describes the logical design subsystems within the Thor-2-PCMCIA-Plus adapter. Each subsystem can comprise hardware, firmware, and driver or on-board processor software. The Thor-2-PCMCIA-Plus consists of two subsystems:

1. Line Interface Subsystem
2. Digital Signal Processing Subsystems

6.5.1 Line Interface Subsystem

The Line Interface subsystem is responsible for interfacing the Thor-2-PCMCIA-Plus card with the external T1/E1 links. The subsystem provides the connectors, terminating resistors, transformers, and overvoltage protection.

6.5.1.1 Line Configurations

The Thor-2-PCMCIA-Plus line interfaces support several different line codes:

- HDB3 - High Density Bipolar 3
- B8ZS - Bipolar 8 Zero Substitution
- AMI - Alternate Mark Inversion
- AMI with NZC

For the T1 operation mode, the following framing formats can be used:

- F4 - 4-frame multiframe
- F12 - 12 frame multiframe
- ESF - Extended Superframe
- F72 - 72 frame multiframe

For the E1 operation mode, Thor-2-PCMCIA-Plus supports the following framing formats:

- Doubleframe
- CRC multiframe

6.5.1.2 Fault Monitoring

The line interface subsystem supports fault and performance monitoring. The transceiver subsystem detects and reports the following alarms in the receive streams:

- Framing errors
- Cyclic Redundancy Check (CRC) errors
- Code violations
- Loss of frame alignment
- Loss of Signal (LOS)
- Alarm Indication Signal (AIS)
- E bit errors (E1 only)
- Slip
- Remote Alarm Indication (RAI, Yellow Alarm)

The line interface subsystems also supports the transmitting of the following alarms towards the remote end:

- Alarm Indication Signal (AIS)
- Remote Alarm Indication (RAI, Yellow alarm)
- Auxiliary Pattern (AUXP)

6.5.1.3 Loopbacks

The line interface subsystem implements a remote loopback for line testing. In the remote loopback mode, the clock and data recovered from the line inputs are routed back to the line outputs through the analog transmitter.

6.5.1.4 Error simulation

The line interface subsystem has support for insertion of single bit defects into the transmit data stream. The single bit errors can be generated:

- FAS defect
- Multiframe defect
- CRC defect
- CAS defect
- PRBS defect
- Bipolar violation

6.5.2 Digital Signal Processing Subsystem

The Digital Signal Processing Subsystem consists of two Texas Instruments TMS 320C549 Digital Signal Processors (DSPs). The DSPs provide 120 MIPS processing power each. The DSPs contain 3 serial ports: two buffered and one TDM. Buffered serial port #0 is connected with a highway to the T1E1_LI device. Buffered serial port #1 and TDM serial port is connected to the other DSP to provide a physical highway between the DSPs.

For more information on how to develop software for the DSPs, please refer to *Programmer's Guide for OTX DSP Application Development* (Odin product #1412-1-SDA-1012-1). For more information on the capabilities of the DSPs, please refer to the appropriate documentation from Texas Instruments, Inc.

6.6 Customization Options

The Thor-2-PCMCIA-Plus board can be customized in the following ways:

- It can be delivered with custom (customer supplied) labels.

- A custom string of a maximum length of 31 bytes can be programmed into the Flash memory of the card. This string can be read by the user application by reading the OTX_ATTR_BRD_USER_STRING from the board handle.
- The Card Information Structure (CIS) which is stored on the board can be customized to contain a product and company name other than “Odin TeleSystems Thor-2-PCMCIA-Plus”.

7. Host Control Interface

Thor-2-PCMCIA-Plus communicates with the Host PC over the PCMCIA bus. The Thor-2 board is I/O mapped and utilizes interrupts.

Thor-2-PCMCIA-Plus requires the following system resources:

- Free 16 address I/O-address range
- Free 32 address I/O-address range
- Free Interrupt (IRQ)

Doc. No. 1111-1-HAA-1043-1
For more information on this product, please contact:

Odin TeleSystems Inc.
800 East Campbell Road, Suite 334
Richardson, Texas 75081-1873
U. S. A.

Tel: +1-972-664-0100
Fax: +1-972-664-0855
Email: Info@OdinTS.com
URL: http://www.OdinTS.com/