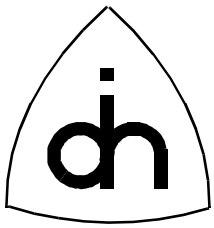
Odin TeleSystems Inc.



Technical Description for Thor-2-PCI

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1. Abstract

This document provides a technical description of Odin TeleSystems' Thor-2-PCI adapter card. This presentation is targeted to systems integrators and application developers who are developing telecommunications systems and/or software applications using the Thor-2-PCI platform. The purpose of this document is to provide the needed information about the hardware to allow software developers to efficiently integrate Thor-2-PCI into their overall system under design.

For information on how to develop host applications utilizing the OTX Hardware Device Driver Application Programming Interface (API), please refer to the *"Programmer's Guide for OTX Hardware API"* document (Odin TeleSystems Inc. document number 1411-1-SAA-1006-1). For help on how to install the Thor-2-PCI card and the OTX Device Driver Software, please refer to the *"Installation Guide for OTX PCI Adapters"* (Odin document number 1512-1-HCA-1001-1).

2. Table of Content

3. Introduction to Thor-2-PCI

Thor-2-PCI is multi-purpose T1/E1 interface adapter. The Thor-2-PCI card allows Personal Computers (PCs) and other systems with a PCI bus to be interfaced with T1/E1 links.

Thor-2-PCI is a member of the Odin Telecom frameworX (OTX) product family. Thor-2-PCI is supported by the OTX device driver and by the OTX Hardware Application Programming Interface (API). Equipped with the appropriate OTX software modules, Thor-2-PCI can be utilized in a variety of T1/E1, Integrated Services Digital Network (ISDN), Frame Relay, and Signaling System #7 (SS#7) applications.

The Thor-2-PCI supports two T1 or E1 interfaces at the speeds of 1.544 Mbps and 2.048 Mbps, respectively. Throughout the document the T1/E1 interfaces are referred to as Line Interfaces (LIs). The same board supports both T1 and E1. The operation mode as well as the line terminating impedance of 75 ohms or 100 ohms are software switchable. The card also supports a high-impedance mode for monitoring. Consequently, the Thor-2-PCI card can be used to terminate two T1/E1 links or to monitor one link.

The Thor-2-PCI provides H.100 Computer Telephony Bus. The H.100 bus comprises of thirty-two (32) 2, 4, or 8 Mbit/s Time-Division Multiplexed (TDM) highways for board-to-board communication. On the Thor-2-PCI board the H.100 highways are connected to a non-blocking time-space switch. The time-space switch allows 256 time-slots to be switched between H.100 highways and the local highways. 1024 time-slots can be switched locally between on-board devices. The H.100 bus is backwards compatible with the MVIP bus and SCBus.

The Thor-2-PCI board also contains an OTX Application Specific Module (ASM) socket. The ASM interface can be used to add daughter boards providing additional resources. For example, Thor-2-PCI can be augmented with Vidar-5x4-ASM providing 4 TI TMS320C548 Digital Signal Processors (DSPs). By loading and running different programs in these DSPs, the Thor-2-PCI adapter can support a variety of different telecom functions, such as tone detection and generation, HDLC sending and receiving, voice encoding and decoding, etc.

Finally, Thor-2-PCI contains four (4) codecs. The codecs perform Analog-to-Digital (A/D) and Digital-to-Analog (D/A) conversions. Both the A-law and the u-law are supported. The codecs can be switched to any time-slots on the board. Standard handsets can be connected to the codecs to provide phone functionality.

4. Specifications

Thor-2-PCI is a half-length PCI board. The physical dimensions of Thor-2-PCI are shown in Figure 1.

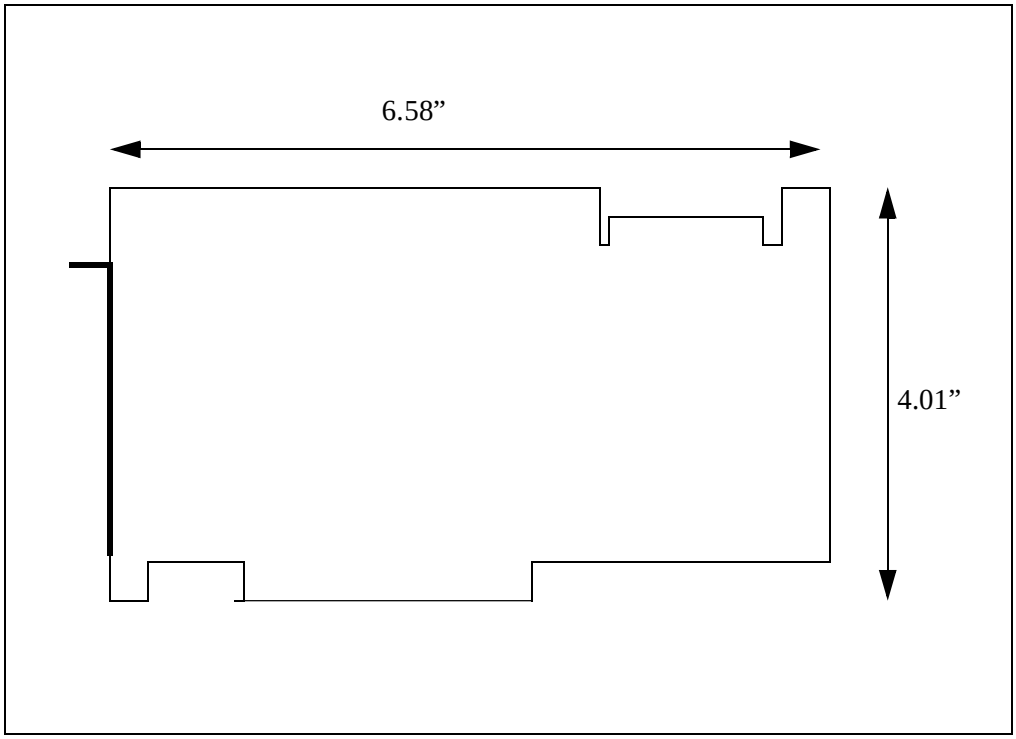

Figure 1. Thor-2-PCI Physical Dimensions (inches).

The Thor-2-PCI operates with +5.0 V supply voltage.

5. Supported Driver Devices

5.1 Physical Devices

The Thor-2-PCI supports the following physical API driver devices:

TABLE 1. OTX Physical Driver Devices supported by Thor-2-PCI

Host Device	Device Type	Max #	Description
0	*OTX_DEVICE_THOR_PCI*	1	Board Device
OTX_DEVICE_THOR_PCI	*OTX_DEVICE_LI_T1E1*	2	T1/E1 Line Interface Devices
OTX_DEVICE_THOR_PCI	*OTX_DEVICE_TSS*	1	Time-Space Switch

TABLE 1. OTX Physical Driver Devices supported by Thor-2-PCI

Host Device	Device Type	Max #	Description
OTX_DEVICE_THOR_PCI	*OTX_DEVICE_CODEC*	4	Codec performing A/D and D/A conversions for analog front ends.
OTX_DEVICE_THOR_PCI	*OTX_DEVICE_VIDAR_5x_ASM*	1	Vidar-5x4-ASM Daughter Board (OPTIONAL)

5.2 Logical Devices

The Thor-2-PCI supports the following logical API driver devices:

TABLE 2. OTX Logical Driver Devices supported by Thor-2-PCI

Host Device	Device Type	Max #	Description
OTX_DEVICE_LI_T1E1	*OTX_LDEVICE_HDLC_SENDER*	1	Logical Device for sending Hdlc Framing
OTX_DEVICE_LI_T1E1	*OTX_LDEVICE_HDLC_RECEIVER*	1	Logical Device for receiving Hdlc framing.
OTX_DEVICE_LI_T1E1	*OTX_LDEVICE_CAS_T1E1_SENDER_RECEIVER*	1	Logical Device for T1/E1 Channel Associated Signalling (CAS)

In addition, DSPs on an ASM board can be loaded with various program packages to provide support for a variety of Logical Devices types. For example, the Signal Processing Package One (OtxSpm1) for Vidar-5x4-ASM provides support for the following API logical devices:

- *OTX_LDEVICE_TONE_CONST_VAL_GENERATOR*
- *OTX_LDEVICE_TONE_EFFECTS_GENERATOR*
- *OTX_LDEVICE_TONE_SINEWAVE_GENERATOR*
- *OTX_LDEVICE_TONE_DTMF_GENERATOR*
- *OTX_LDEVICE_TONE_DTMF_DIALER*
- *OTX_LDEVICE_TONE_SILENCE_DETECTOR*
- *OTX_LDEVICE_TONE_DTMF_DETECTOR*
- *OTX_LDEVICE_DATA_CONVERTER*
- *OTX_LDEVICE_HDLC_SENDER*
- *OTX_LDEVICE_HDLC_RECEIVER*

For mode information on the physical and logical driver devices, please refer to *Programmer's Guide for OTX Hardware Driver* (Odin document # 1412-1-SAA-1006-1).

6. System Architecture

The overall system architecture can be best described and understood through different architectural views or aspects. This document explores the systems architecture from the following angles:

1. **External Interface View:** The external interface view describes the external interfaces of the adapter board, and how they are connected to the various internal devices and modules.

2. **Data Architecture View:** The data architecture view illustrates how the Time - Division Multiplexed (TDM) serial data is connected and transferred through the board.

3. **Control Architecture View:** The control architecture view describes how the internal devices and modules can be controlled by the host processor.

4. **Clock Architecture View:** The clock architecture view specifies what clocking and synchronization options are available, how clocking is derived, and how it distributed to the various devices.

5. **Logical Subsystem View:** The logical subsystem view describes the logical design subsystems in the system. Each subsystem can comprise hardware, firmware and driver or on-board processor software.

It is important to note that one device within the board can be involved in several of these views, each view describing how one aspect of the device interfaces with other devices.

6.1 External Interfaces

The Thor-2-PCI contains the following external interfaces:

- PCI Host Bus
- H.100 Computer Telephony Bus
- Centronics Network Interface with
  - 2 T1/E1 Line Interfaces
  - 4 Analog Interfaces for Handsets
  - 2 External Synchronization Clock Inputs
- OTX ASM Socket
- JTAG Port for DSP Control

The external interfaces of the Thor-2-PCI card are illustrated in Figure 2.

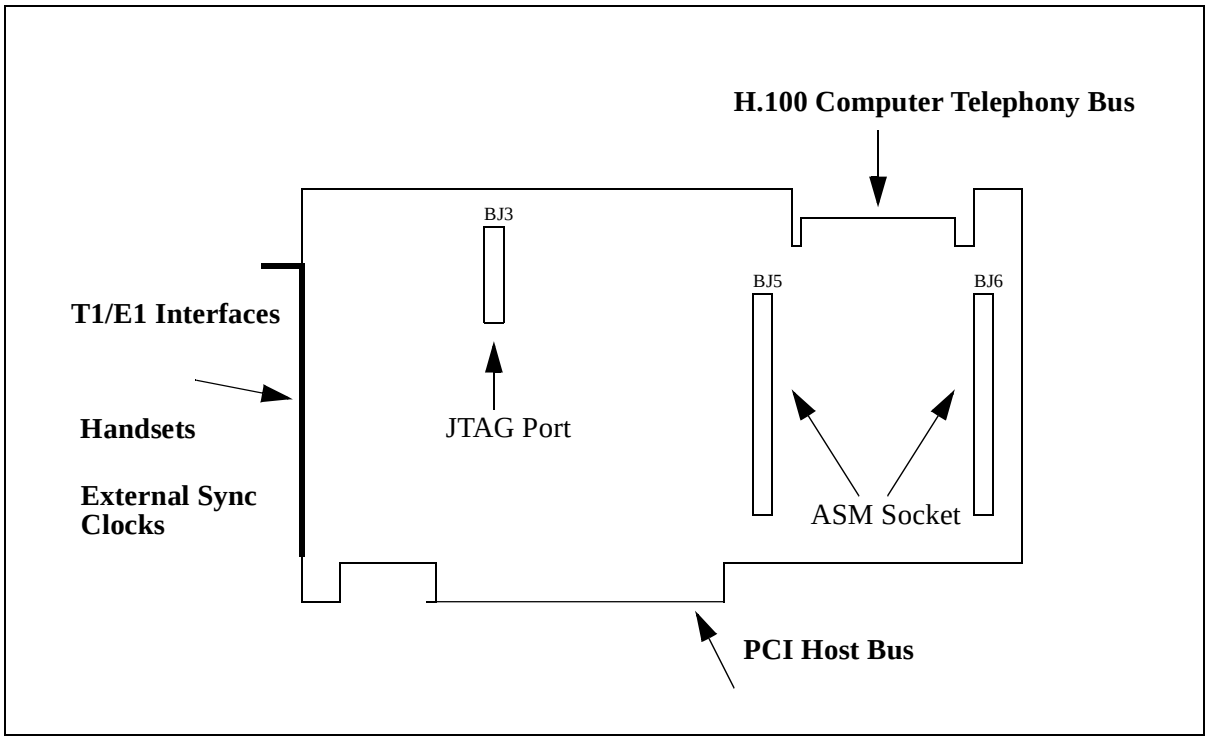

Figure 2. Thor-2-PCI External Interfaces.

6.1.1 PCI Host Bus Interface

The interface between the Thor-2-PCI board and the Host Computer is the PCI (Peripheral Connection Interconnect) bus. The electrical characteristics comply to the PCI Standard, Revision 2.1. For more information on the PCI bus, please contact the PCI special interest group, PCI SIG, ***http://www.pcisig.com*** .

6.1.2 H.100 Computer Telephony Bus Interface

Thor-2-PCI supports the H.100 Computer Telephony Bus standard. The H.100 bus is a collection of time-division multiplexed (TDM) digital telephony highways designed to carry telephony traffic between extensions boards within one PC chassis. The H.100 bus supports 32 TDM highways. The highways can be operated at 2.048, 4.096, or 8.192 MBit/s carrying 32, 64, or 128 64 kbit/s time-slots, respectively. Up to 20 boards can be connected to one H.100 bus. The maximum distance between boards is 7 inches.

Within the PC chassis the data streams are passed from card to card using a 60 pin ribbon cable and AMP 1-557089-2 connectors. The H.100 connector is a 60-finger edge

connector on the upper right-hand side (Figure 2) of the board. The pin-out of the H.100 connector is listed in Table 3.

TABLE 3. Thor-2-PCI H.100 Pin Assignments

Pin	Signal	Pin	Signal
1	Reserved	2	Power to active devices (CT_+5Vdc)
3	TDM Highway 31 (CT_D31)	4	TDM Highway 30 (CT_D30)
5	TDM Highway 29 (CT_D29)	6	TDM Highway 28 (CT_D28)
7	GND	8	TDM Highway 27 (CT_D27)
9	TDM Highway 26 (CT_D26)	10	TDM Highway 25 (CT_D25)
11	TDM Highway 24 (CT_D24)	12	GND
13	TDM Highway 23 (CT_D23)	14	TDM Highway 22 (CT_D22)
15	TDM Highway 21 (CT_D21)	16	TDM Highway 20 (CT_D20)
17	GND	18	TDM Highway 19 (CT_D19)
19	TDM Highway 18 (CT_D18)	20	TDM Highway 17 (CT_D17)
21	TDM Highway 16 (CT_D16)	22	GND
23	TDM Highway 15 (CT_D15)	24	TDM Highway 14 (CT_D14)
25	TDM Highway 13 (CT_D13)	26	TDM Highway 12 (CT_D12)
27	GND	28	TDM Highway 11 (CT_D11)
29	TDM Highway 10 (CT_D10)	30	TDM Highway 9 (CT_D9)
31	TDM Highway 8 (CT_D8)	32	GND
33	TDM Highway 7 (CT_D7)	34	TDM Highway 6 (CT_D6)
35	TDM Highway 5 (CT_D5)	36	TDM Highway 4 (CT_D4)
37	GND	38	TDM Highway 3 (CT_D3)
39	TDM Highway 2 (CT_D2)	40	TDM Highway 1 (CT_D1)
41	TDM Highway 0 (CT_D0)	42	GND
43	Frame Sync from “A” Clock Master (/CT_FRAME_A)	44	GND
45	Bit Clock from “A” Clock Master (CT_C8_A)	46	GND
47	Secondary Network Timing Reference (CT_NETREF)	48	GND
49	Redundant Frame Sync from “B” Clock Master (/CT_FRAME_B)	50	GND
51	Redundant Bit Clock from “B” Clock Master (CT_C8_B)	52	GND
53	Message Channel (CT_MC)	54	GND
55	Compatibility Frame Pulse (/FR_COMP)	56	GND
57	SCbus System Clock (SCLK)	58	GND

TABLE 3. Thor-2-PCI H.100 Pin Assignments

Pin	Signal	Pin	Signal
59	SCbus System Clock time two (SCLKx2)	60	GND
61	MVIP-90 bit clock (C2)	62	GND
63	MVIP-90 bit clock time two (/C4)	64	GND
65	H-MVIP 16 Mhz Clock (/C16+)	66	H-MVIP 16 Mhz Clock /C16-
67	GND	68	RESERVED

For more information on the H.100 bus, please contact the Enterprise Computer Telephony Forum, ECTF, ***http://www.ectf.org*** .

6.1.3 Centronics Network Interfaces

The back panel of Thor-2-PCI contains a Centronics connector with 50 contacts. The Centronics connector provides the following interfaces:

- 2 T1/E1 Line Interfaces
- 4 Analog Interfaces for Handsets
- 2 External Synchronization Clock Inputs

Thor-2-PCI is delivered with a telco-type connector cable (SCSI Cable) and a Harmonica module which converts from Centronics connector to 8 RJ-11 connectors. The Harmonica module allows the connection of T1/E1 lines, handsets, and external synchronization clocks to Thor-2-PCI using RJ-11 connectors (See Figure 3).

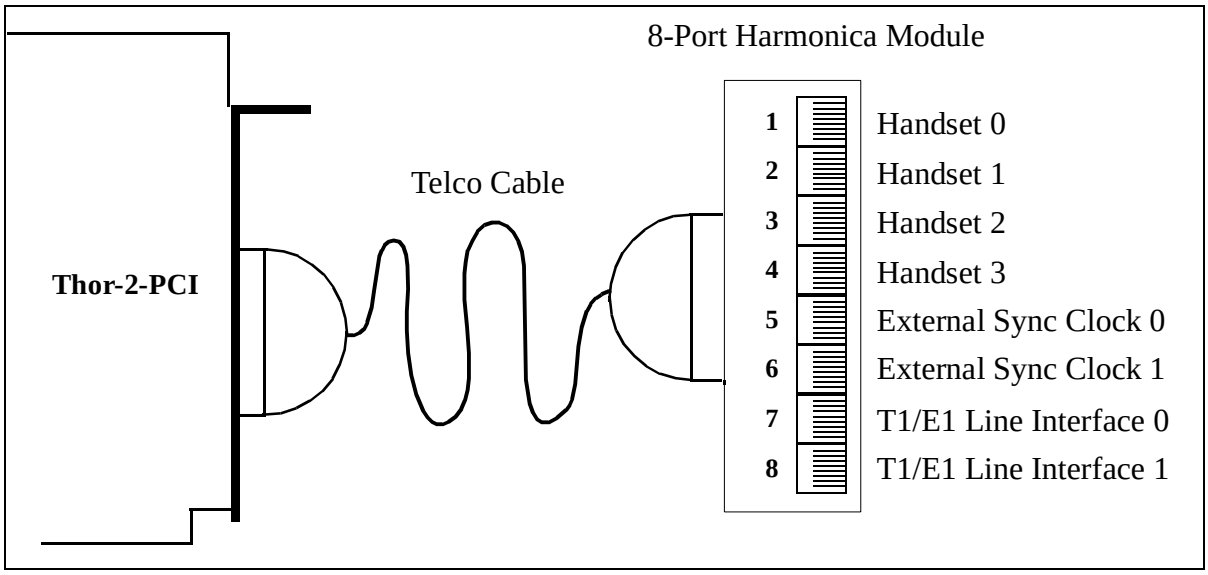

Figure 3. Thor-2-PCI Harmonica Module

Although Thor-2-PCI is delivered with the RJ-45 / RJ-11 Harmonica module, the modular structure of Thor-2-PCI allows it to be adapted for other types of connectors as well. For example, if the application requires BNC or Bantam type connectors, the Harmonica module can be replaced with another type of adapter which converts from Centronics to BNC or Bantam type connectors. The pin-outs of the Centronics and the RJ-11 connectors are documented in Figure 4 and in Table 4.

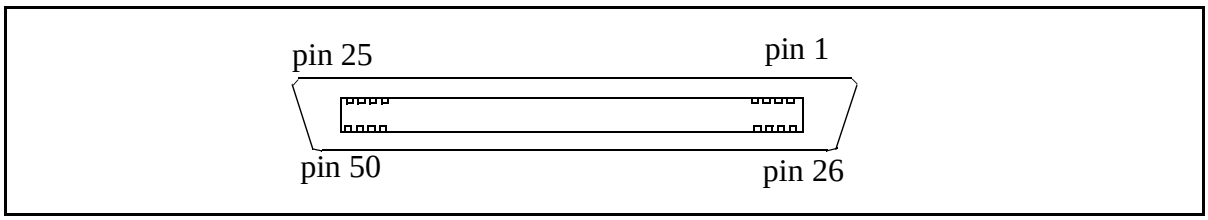

Figure 4. Thor-2-PCI Centronics Connector.

TABLE 4. Thor-2-PCI Centronics Connector Pin Assignments

Pin	Signal	Pin	Signal
1	Codec-0, Speaker (-)	26	Codec-0, Speaker (+)
2	Codec-0, Handset Microphone (+)	27	Codec-0, Handset Microphone Ground
3	Reserved	28	Reserved
4	Codec-1, Speaker (-)	29	Codec-1, Speaker (+)
5	Codec-1, Handset Microphone (+)	30	Codec-1, Handset Microphone Ground
6	Reserved	31	Reserved
7	Codec-2, Speaker (-)	32	Codec-2, Speaker (+)
8	Codec-2, Handset Microphone (+)	33	Codec-2, Handset Microphone Ground
9	Reserved	34	Reserved
10	Codec-3, Speaker (-)	35	Codec-3, Speaker (+)
11	Codec-3, Handset Microphone (+)	36	Codec-3, Handset Microphone Ground
12	Reserved	37	Reserved
13	External Sync Clock In 0 (Connected together with pin 32)	38	External Sync Clock In 0 (Connected together with pin 7)
14	Ground	39	Ground
15	Reserved	40	Reserved
16	External Sync Clock In 1 (Connected together with pin 35)	41	External Sync Clock In 1 (Connected together with pin 10)
17	Ground	42	Ground
18	Reserved	43	Reserved
19	Line Interface 0, Transmit Line (tip)	44	Line Interface 0, Transmit Line (ring)

TABLE 4. Thor-2-PCI Centronics Connector Pin Assignments

Pin	Signal	Pin	Signal
20	Line Interface 0, Receive Line (ring)	45	Line Interface 0, Receive Line (tip)
21	Reserved	46	Reserved
22	Line Interface 1, Transmit Line (tip)	47	Line Interface 1, Transmit Line (ring)
23	Line Interface 1, Receive Line (ring)	48	Line Interface 1, Receive Line (tip)
24	Reserved	49	Reserved
25	Reserved	50	Reserved

There are two types of Thor-2-PCI harmonicas:

- RJ-11 T1/E1 connectors (HMA-1047-1)
- RJ-45 T1/E1 connectors (HMA-1047-2)

The RJ-11 pin-outs in the HMA-1047-1 Harmonica module for the 4-wire T1/E1 line interfaces are shown in Figure 5.

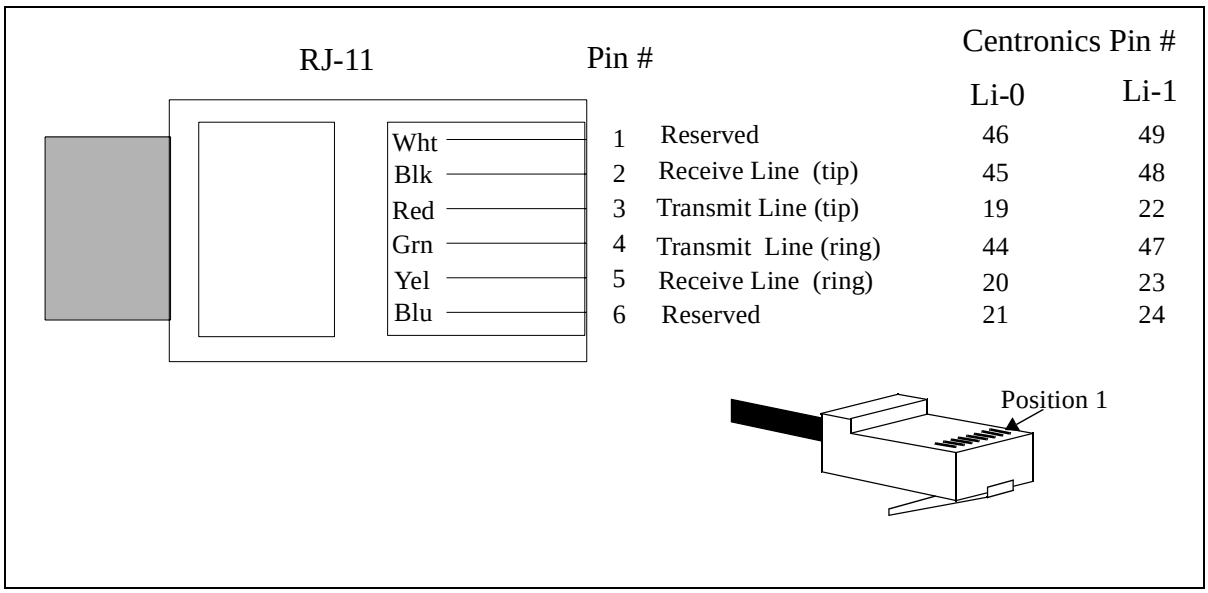

Figure 5. RJ-11 Connector for the T1 or E1 Interface (HMA-1047-1).

The RJ-45 pin-outs in the HMA-1047-2 Harmonica module for the 4-wire T1/E1 line interfaces are shown in Figure 6.

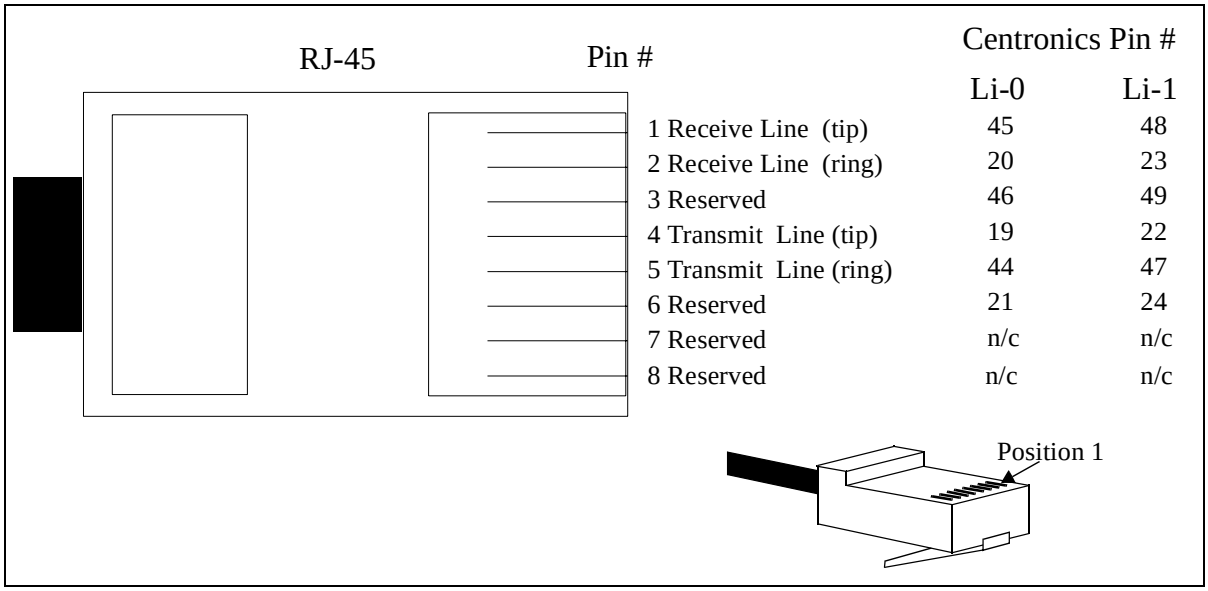

Figure 6. RJ-45 Connector for the T1 or E1 Interface (HMA-1047-2).

Two 8 kHz external synchronization clocks can be connected to the Harmonica as well. The synchronization clock RJ-11 pin out is shown in Figure 7.

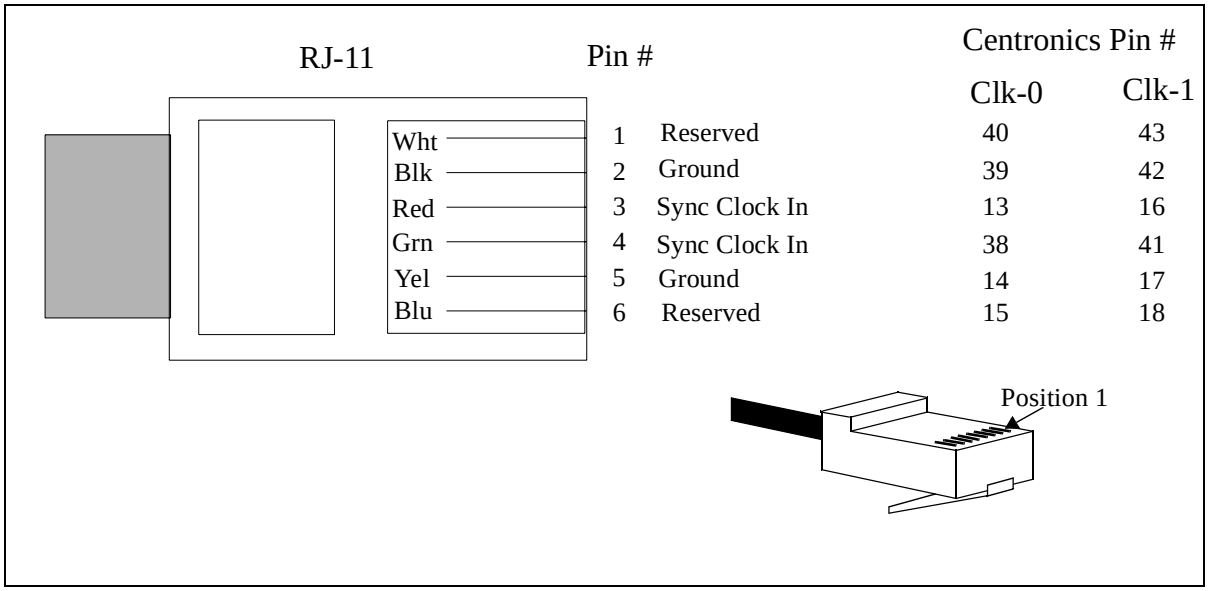

Figure 7. RJ-11 Connector for the External Synchronization Clock.

Note that the synchronization clock in can be connected to either pin 3 or pin 4 (the pins are connected together internally) on the RJ-11. This allows the user to make a

cable where the clock is simply connected to one of the leads on the inner pair without worrying about the wires in the inner pair possibly getting swapped.

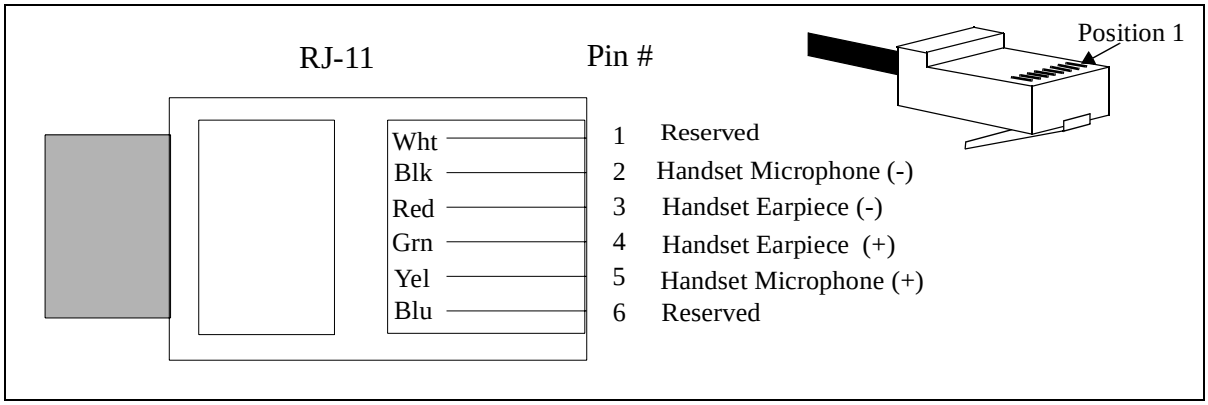

Figure 8. RJ-11 Connector for the Handsets.

6.1.3.1 Monitor Configuration

The Thor-2-PCI board can be used to monitor one active E1/T1 span. One pair of the active E1/T1 span connects to the receiver pins of E1T1 device#0 on Thor-2-PC.I The other pair of the active E1/T1 span connects to the receiver pins of E1T1 device#1 on Thor-2-PCI. These connections are illustrated in Figure 9. This figure shows the connection points directly to the Centronix connector, but it is also possible to connect via the harmonica using the receiver pins of the E1T1 Line interface port 0 and port 1 (see Figure 3 and Figure 6).

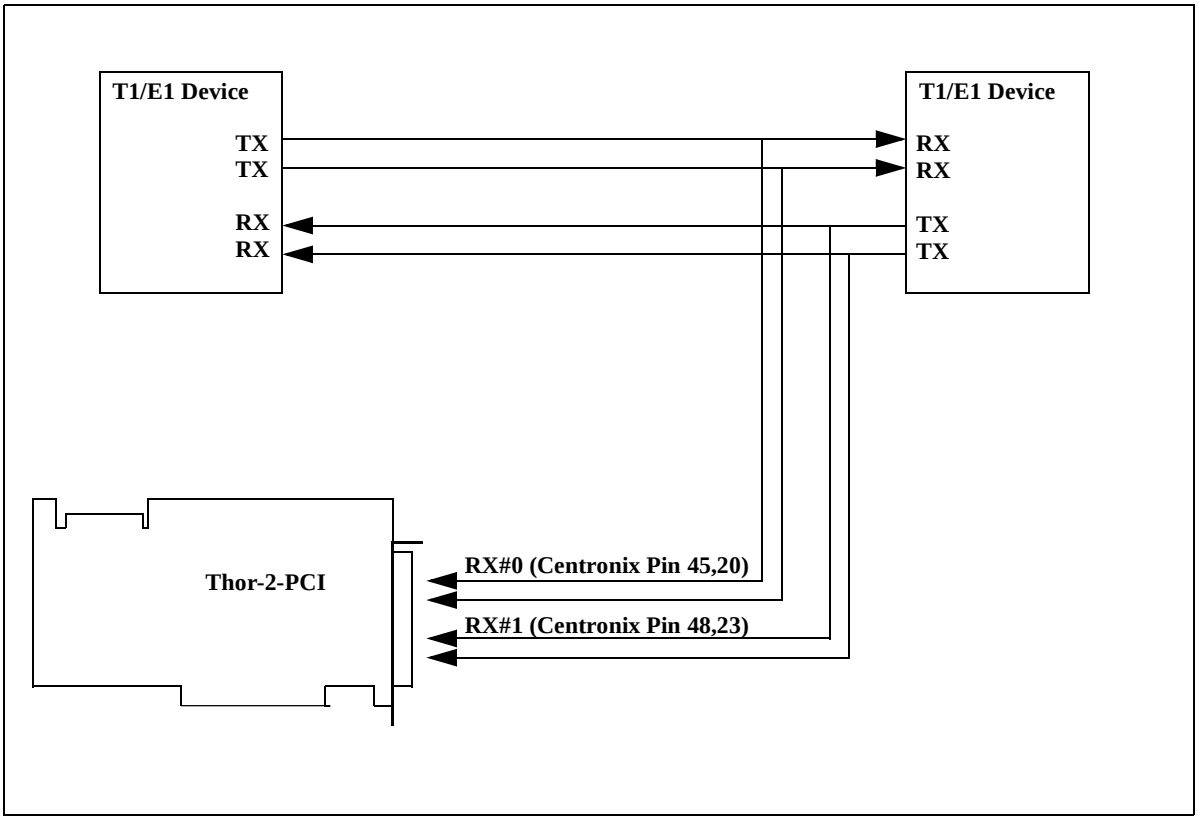

Figure 9. Using Thor-2-PCI to monitor an active E1/T1 span.

6.1.4 OTX ASM Interface

The Thor-2-PCI board contains an OTX ASM (Application Specific Module) Interface (Reference Designators BJ5 and BJ6). The ASM Interface can be used to attach a daughter board modules to the Thor-2-PCI board. The ASM daughter boards can add functionality, such as DSP or HDLC resources.

6.1.5 JTAG Interface

The JTAG port (reference designator BJ3) are used for:

- Board Testing
- Programming of Complex Programmable Logical Devices (CPLDs)
- Connecting the DSP emulator board for DSP Software Development.

For more information on how to use the JTAG port and the DSP emulator, please refer to *"Programmer's Guide for OTX DSP Application Development,"* Odin Document # 1412-1-SAA-1004-1.

6.2 Data Architecture

Internally, Thor-2-PCI utilizes serial TDM (Time-Division Multiplexed) data streams for transfer of data or voice. The internal serial TDM data streams are called “Highways.” External interfaces are called spans.

The serial highways provide data paths between physical devices as shown in Figure 10. If the physical device connects to more than one highway, the device specific highway port number is also shown in Figure 10.

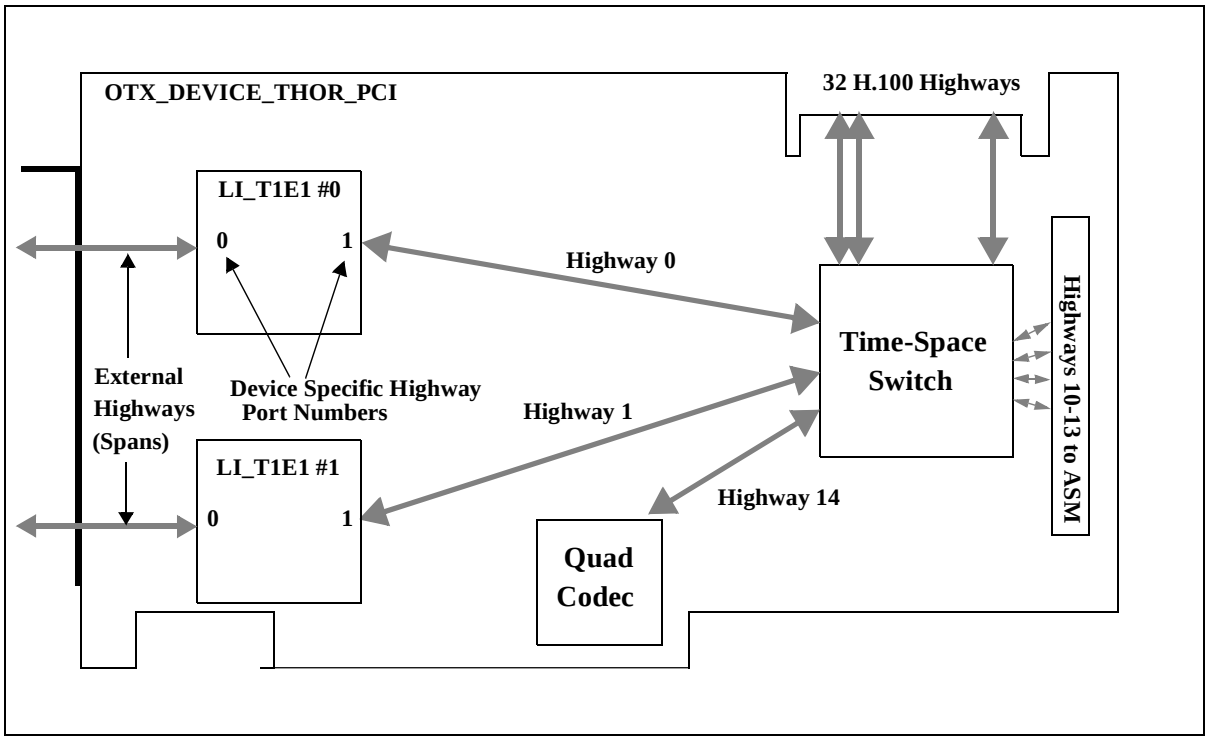

Figure 10. Thor-2-PCI Highway Connections.

The Thor-2-PCI internal highways are configured to operate at 2.048 Mbit/s, each containing 32 8-bit time-slots. The data rate of one time-slot is 64 kbit/s. Table 5 lists the internal highways used on Thor-2-PCI boards.

TABLE 5. Thor-2-PCI Highway Connections

Highway #	Connecting Time-Space Switch to
0	T1/E1 Line Interface #0
1	T1/E1 Line Interface #0
2-9	Reserved
10-13	ASM Daughter Board

TABLE 5. Thor-2-PCI Highway Connections

Highway #	Connecting Time-Space Switch to
14	Quad Codec
15	Reserved

The time-space switch in non-blocking and allows any internal time-slot on any internal highway to be switched to any other highway/time-slot. The cross-connections are software programmable and automatically taken care of by the OTX driver.

In addition, the Thor-2-PCI contains external several highways:

- 2 Highways mapped to the T1/E1 spans
- 32 H.100 Highways

The Thor-2-PCI time-space also provides support multicasting and messaging. In multicasting mode any input channel can be cross-connected to multiple output channels. For example, an incoming Li time slot can be both switched to an outgoing H.100 Highway and it can also be switched to the Codec or ASM board.

In the messaging mode, the time-space switch can be instructed to send a constant byte on any time slot. Once activated, every byte on the specified time slot will contain the same value. The generation of constant byte does not consume any processing capacity. The constant byte feature is useful in, for example, verification of a through connection or in Bit Error Rate (BER) testing.

6.3 Control Architecture

The host PC can control the physical devices on the Thor-2-PCI board through the PCI bus. The Thor-2-PCI control architecture is illustrated in Figure 11.

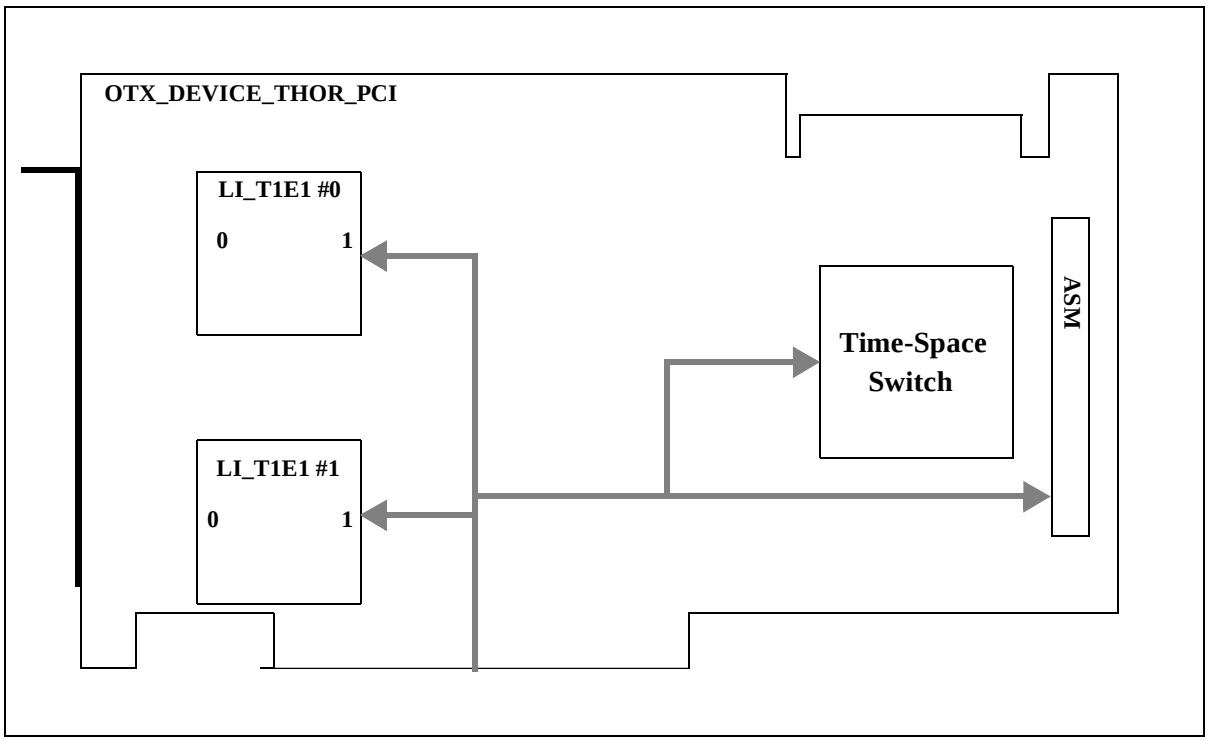

Figure 11. Thor-2-PCI Control Architecture.

6.4 Clock Architecture

On the Thor-2-PCI board all the internal TDM data highways and the all the devices processing TDM data are synchronized to one clock reference. The clock reference can be derived from multiple sources and then switched to all the devices. The clocking sources supported by Thor-2-PCI are illustrated in Figure 12 and listed in Table 6.

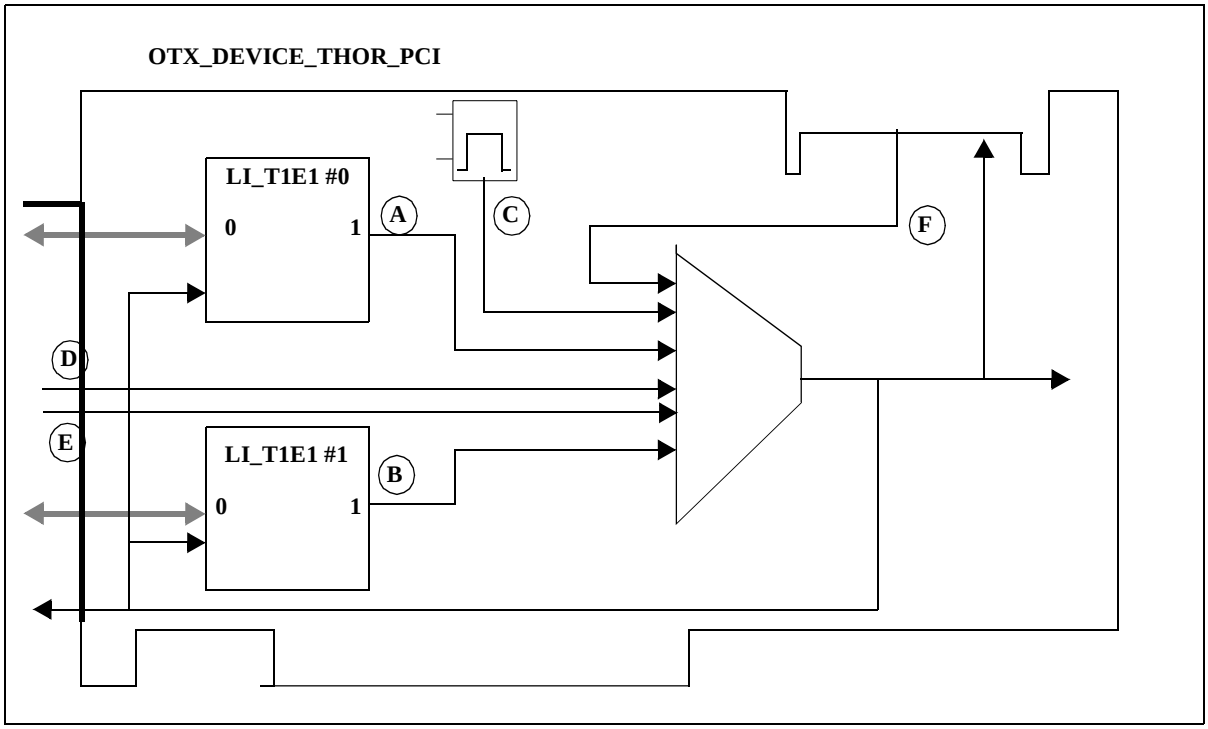

Figure 12. Thor-2-PCI Clock Architecture Overview.

TABLE 6. Thor-2-PCI Clocking Sources.

Clock Source	Description	'clkSource' parameter for OtxBrdSetClocks(), OTX HW Driver
A	Clock extracted from the incoming T1/E1 span 0 (LI-0).	OTX_CLOCK_SOURCE_LOCAL_0
B	Clock extracted from the incoming T1/E1 span 1 (LI-1).	OTX_CLOCK_SOURCE_LOCAL_1
C	On-board free running oscillator.	OTX_CLOCK_SOURCE_INTERNAL
D	External 4.096MHz clock from Centronix connector (External Clock 0)	OTX_CLOCK_SOURCE_LOCAL_4
E	External 4.096MHz clock from Centronix connector (External Clock 1)	OTX_CLOCK_SOURCE_LOCAL_5
F	H.100 Reference Clock	OTX_CLOCK_SOURCE_A_CLOCKS, OTX_CLOCK_SOURCE_B_CLOCKS

In the event that the clocking source is lost, Thor-2-PCI will automatically switch to a backup clocking source. For example, if clocking is derived from an incoming T1/E1 span, and the span experiences Loss of Signal (LOS), the clocking source is automatically switched to the other T1/E1 span. If the other span loses signal as well, then Thor-2 will switch to free-running mode and the clocking will be derived from the on-board oscillator. If the H.100 clocks or the external clocks are used as the clocking source and the clocking is lost, Thor-2-PCI will switch into free-running mode and use the on-board oscillator.

It is important to understand that the difference between the clocks on the external T1/E1 spans and the internal clocks. When the Thor-2-PCI clocking is derived from one incoming T1/E1 span, the external T1/E1 span and the internal highways on-board are completely synchronized. In that case, the other T1/E1 span is not necessarily in synchronization with the internal highways. To compensate for that, Thor-2-PCI implements an elastic receive buffer with a size of 64x8 bits.The elastic store is used to adapt the clock rates between the T1/E1 clock and the Thor-2-PCI system clock, to compensate for input wonder and jitter, and to align the received frame with the internal highway frame. However, the elastic buffer may eventually over- or underflow and a slip condition may occur. When a positive or negative slip occurs, Thor-2-PCI will discard one received layer-1 frame to free space in the elastic receive buffer and to continue forwarding the data from incoming T1/E1 span to the internal highway. The slip condition will cause a one 8-bit data sample to be discarded on all of the timeslots.

The occurrence of slips is normal in telephone network. A loss of data sample in a voice data is insignificant cannot be detected by human ear. Loss of one data byte in a data transmission is typically detected with Cyclic Redundancy Checks (CRC). A loss of a data byte due to a slip is typically corrected by the data link protocol requesting a retransmission of the corrupted packet.

6.5 Logical Subsystems

The logical subsystem view describes the logical design subsystems within the Thor-2-PCI adapter. Each subsystem can comprise hardware, firmware, and driver or on-board processor software. The Thor-2-PCI consists of two subsystems:

1. Line Interface Subsystem
2. Switching Subsystem
3. Codec Subsystem

6.5.1 Line Interface Subsystem

The Line Interface subsystem is responsible for interfacing the Thor-2-PCI card with the external T1/E1 links. The subsystem provides the connectors, terminating resistors, transformers, and overvoltage protection.

6.5.1.1 Line Configurations

The thor-2-PCI line interfaces support several different line codes:

- HDB3 - High Density Bipolar 3
- B8ZS - Bipolar 8 Zero Substitution
- AMI - Alternate Mark Inversion
- AMI with NZC

For the T1 operation mode, the following framing formats can be used:

- F4 - 4-frame multiframe
- F12 - 12 frame multiframe
- ESF - Extended Superframe
- F72 - 72 frame multiframe

For the E1 operation mode, Thor-2-PCI supports the following framing formats:

- Doubleframe
- CRC multiframe

6.5.1.2 Fault Monitoring

The line interface subsystem supports fault and performance monitoring. The transceiver subsystem detects and reports the following alarms in the receive streams:

- Framing errors
- Cyclic Redundancy Check (CRC) errors
- Code violations
- Loss of frame alignment
- Loss of Signal (LOS)
- Alarm Indication Signal (AIS)
- E bit errors (E1 only)
- Slip
- Remote Alarm Indication (RAI, Yellow Alarm)

The line interface subsystems also supports the transmitting of the following alarms towards the remote end:

- Alarm Indication Signal (AIS)
- Remote Alarm Indication (RAI, Yellow alarm)
- Auxiliary Pattern (AUXP)

6.5.1.3 Loopbacks

The line interface subsystem implements a remote loopback for line testing. In the remote loopback mode, the clock and data recovered from the line inputs are routed back to the line outputs through the analog transmitter.

6.5.2 Switching Subsystem

The switching subsystem provides a time-space switch for the switching of any incoming time/slot to any outgoing time slot. This subsystem is also responsible for delivering and switching of the on-board clock signals. The switching subsystem has already been covered in Chapter 6.2: "Data Architecture" and Chapter 6.4: "Clock Architecture".

6.5.3 Codec Subsystem

The Thor-2-PCI board contains four codecs allowing the user to listen in on any 4 internal time-slots. The codecs convert four digital Pulse Code Modulated (PCM) time-slots into analog electrical signals. The analog signals from the codecs can then be connected to standard telephone handsets through connectors 5 - 8 in the Harmonica.

The Thor-2-PCI codecs support both A-law and u-law for the Analog-to-Digital and Digital-to-Analog conversions. The conversion law to be used can be selected by software.

Codec #0 is permanently connected to time-slot 1 (0 count) on the Internal Highway #14. Codecs 1 - 3 are connected to time-slots 2 - 4, respectively. The time-space switch can be used to cross-connect the codecs into any incoming or outgoing time-slot in the Line Interface, ASM, or H.100 Highways.

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