Odin TeleSystems Inc.

Sleipnir-1-PC104-Plus
Technical Description

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1 Abstract

This document provides a technical description of Odin TeleSystems' Sleipnir-1-PC104-Plus adapter card. This presentation is targeted to systems integrators and application developers who are developing telecommunications systems and/or software applications using the Sleipnir-1-PC104-Plus platform. The purpose of this document is to provide the needed information about the hardware to allow software developers to efficiently integrate Sleipnir-1-PC104-Plus into their overall system under design.

For information on how to develop host applications utilizing the OTX Hardware Device Driver Application Programming Interface (API), please refer to the "Programmer's Guide for OTX Hardware API" document (Odin TeleSystems Inc. document number 1411-1-SAA-1006-1). For information on how to develop custom DSP applications, please refer to "Programmer's Guide for OTX C54x DSP Software Development Kit" (Odin document number 1412-1-SAA-1007-1). And finally, for help on how to install the Sleipnir-1-PC104-Plus card and the OTX Device Driver Software, please refer to the Installation Guide for OTX PCMCIA Adapters (Odin TeleSystems Inc. document number 1512-1-HCA-1003-1).

2 Sleipnir-1-PC104-Plus Overview

Sleipnir-1-PC104-Plus is a single span T1/E1/J1 adapter for the PC104 Plus bus. The Sleipnir-1-PC104-Plus is a member of the Odin Telecom frameworX (OTX) product family. It is supported by the OTX device driver and by the OTX Hardware Application Programming Interface (API). It is populated with one Texas Instruments TMS320VC5510 400 Mips DSP and 16MB external memory. Equipped with the appropriate OTX software modules, Sleipnir-1-PCI-Plus can be utilized in a variety of T1/E1, Integrated Services Digital Network (ISDN), Frame Relay, and Signaling System #7 (SS#7) applications.

- The Sleipnir-1-PC104-Plus supports one T1/J1 or E1 interface at the speeds of 1.544 Mbps and 2.048 Mbps, respectively. The same board supports both T1/J1 and E1. Sleipnir-1-PC104-Plus supports all popular frame formats and line coding.

3 Physical specifications

Sleipnir-1-PC104-Plus is a standard size PC104 board.

4 Data Architecture

Internally, Sleipnir-1-PC104-Plus utilizes serial TDM (Time-Division Multiplexed) data streams for transfer of data or voice. The internal serial TDM data streams are called "Highways." The external interface is referred to as "span".

The serial highways provide data paths between physical devices as shown in the figure below.
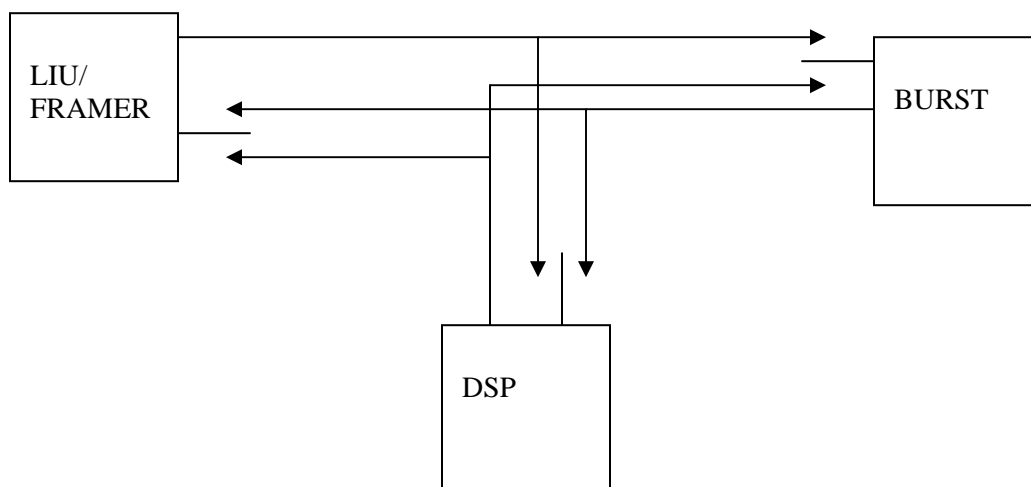
5 PCM Highways

The Sleipnir-1-PC104-Plus utilizes 2 Mbit/sec PCM highways for data routing. When the optional DSP is installed, the DSP can process data from ether the incoming data stream or from the host by way of DMA transfer. The DSP can supply data to ether the outgoing data stream or the host by way of DMA transfer.

6 API Supported Physical Devices

6.1 Board Devices

The Sleipnir-1-PC104-Plusconfiguration and status registers are accessible by API calls. The board devices include the serial to parallel converters and the DMA controller. The application can read or write the data directly from the Sleipnir-1-PC104-Plus buffers, or have the DMA controller place the data in the host memory and notify the application when data is available.

6.2 T1/E1 Line Interface Device

The Sleipnir-1-PC104-Plus Line Interface device (LIU) is fully supported by API calls to configure the interface for the required functionality. There is full access to all device registers for monitoring or diagnostics. For more details on the OTX Hardware API please refer to the *"Programmer's Guide for OTX Hardware API"* (Odin document number 1412-1-SAA-1006-1).

6.3 DSP

The optional DSP on the Sleipnir-1-PC104-Plus can be used to run Odin provided standard DSP applications or they can be used to run user developed custom applications. The Sleipnir-1-PC104-Plus telecom configuration is delivered with a number of Odin's Signal Processing Module (SPM). These SPMs, or DSP application packages, provides supports for many common telecom applications; such as tone detection and generation, FSK detection, and HDLC sending and receiving.

For more information on custom DSP application development, please refer to *"Programmer's Guide for OTX C54x DSP Software Development Kit"* (Odin document number 1412-1-SAA-1007-1).

7 Line Interface Functionality

7.1 Line Configurations

The Sleipnir-1-PC104-Plus line interfaces support several different line codes:

- HDB3 - High Density Bipolar 3

- B8ZS - Bipolar 8 Zero Substitution

- AMI - Alternate Mark Inversion

- AMI with NZC

For the T1 operation mode, the following framing formats can be used:

- F4 - 4-frame multiframe

- F12 - 12 frame multiframe (D3/D4, Superframe)

- ESF - Extended Superframe

- F72 - 72 frame multiframe (SLC96 mode)

For the E1 operation mode, Sleipnir-1-PC104-Plus supports the following framing formats:

- Doubleframe

- CRC multiframe

7.2 Fault Monitoring

The line interface subsystem supports fault and performance monitoring. The transceiver subsystem detects and reports the following alarms in the receive streams:

- Framing errors

- Cyclic Redundancy Check (CRC) errors

- Code violations

- Loss of frame alignment

- Loss of Signal (LOS)

- Alarm Indication Signal (AIS)

- E bit errors (E1 only)

- Slip

- Remote Alarm Indication (RAI, Yellow Alarm)

The line interface subsystem also supports the transmitting of the following alarms towards the remote end:

- Alarm Indication Signal (AIS)

- Remote Alarm Indication (RAI, Yellow alarm)

- Auxiliary Pattern (AUXP)

7.3 Loop Back

The line interface subsystem implements a remote loop back for line testing. In the remote loop back mode, the clock and data recovered from the line inputs are routed back to the line outputs through the analog transmitter.

8 Testing features

The Sleipnir-1-PC104-PlusTelecom configuration offers a variety of features to facilitate low-level T1/E1/J1 testing:

- Full access to F, Y, Si, and Sa bits in E1 mode

- Full access to FS/DL-bits in T1 mode (including support for the DL-channel protocol according to T1.403-1989 ANSI or to AT&T TR54016 specification)

- Programmable line build-out in T1/J1 mode

- Transparent mode

- Programmable transmit pulse shape and receive input threshold

- Insertion and detection of single alarms (e.g. Code Violation, Framing Errors, etc)

- Support for generation and detection of Loop codes

- Support for channel loopback

- Support for PRBS (BERT patterns)

9 PCI Bus

The Sleipnir-1-PC104-Plus board is compliant with the PC104 Plus local bus specification. It is a universal interface, supporting both 3.3 volt and 5 volt signaling. The Sleipnir-1-PC104-Plus supports 32 bits at 33 MHz and can be both Slave and Master.

10 T1 / E1 Interface Connector Options

The Sleipnir-1-PC104-Plus board can be populated with either a RJ45 connector or a 4-pin Molex connector for the T1/J1 or E1 span. The RJ45 connector is the industry standard connector for T1/J1 and E1 spans, however it does not meet the height restrictions for a PC104 board. Therefore, the lower height Molex connector is offered as another connector option.

10.1 RJ45 Connector Option

The pinout for the RJ45 connector (J10) is described in the figure below:

RJ-45   Position #

Position #	
1	Receive (RX) (Tip)
2	Receive (RX) (Ring)
3	
4	Transmit (TX) (Tip)
5	Transmit (TX) (Ring)
6	
7	
8	

Position 1
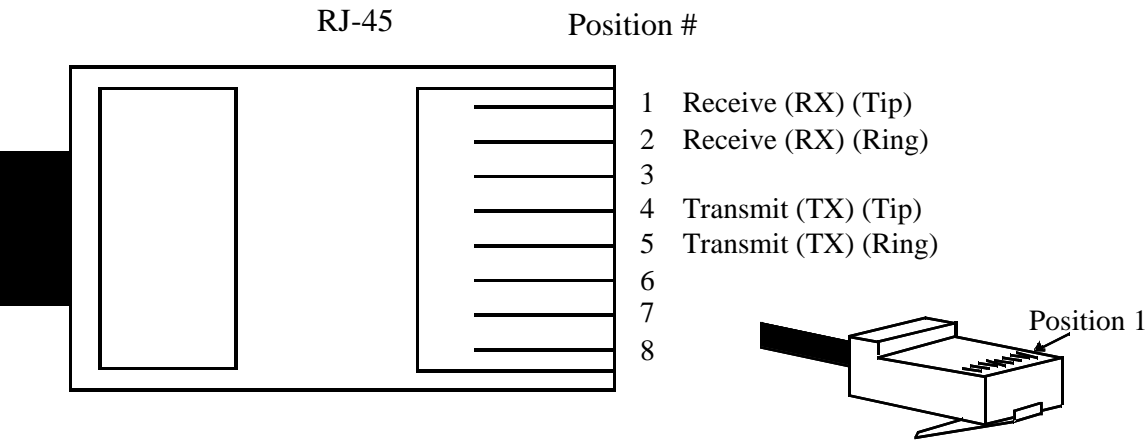
10.2 Molex Connector Option

The pinout for the lower height 4-pin Molex connector is described in Table 1 below:

Table 1 - T1/E1 Connector Pinout

Pin #	Function
1	Receive tip
2	Receive ring
3	Transmit tip
4	Transmit ring

11 Board ID Configuration

Each board on the PC-104 bus must have a unique board ID. The board ID on the Sleipnir-1-PC104-Plus board is configured via the S1 and S2 dipswitches. Please see Table 2 below:

Table 2 - Board ID Configuration

	ID 0	ID 1	ID 2	ID 3	Reserved (Odin)
S1-1	On	Off	Off	Off	Off
S1-2	On	Off	Off	Off	On
S1-3	On	Off	Off	Off	On
S1-4	On	Off	Off	Off	On
S1-5	On	Off	Off	Off	On
S1-6	Off	On	Off	Off	Off
S1-7	Off	On	Off	Off	Off
S1-8	Off	On	Off	Off	Off
S1-9	Off	On	Off	Off	Off
S1-10	Off	On	Off	Off	Off
S2-1	Off	Off	On	Off	Off
S2-2	Off	Off	On	Off	Off
S2-3	Off	Off	On	Off	Off

	ID 0	ID 1	ID 2	ID 3	Reserved (Odin)
S2-4	Off	Off	On	Off	Off
S2-5	Off	Off	On	Off	Off
S2-6	Off	Off	Off	On	Off
S2-7	Off	Off	Off	On	Off
S2-8	Off	Off	Off	On	Off
S2-9	Off	Off	Off	On	Off
S2-10	Off	Off	Off	On	On

12 Clocks

On the Sleipnir-1-PC104-Plus board, all the internal TDM data highways and the all the devices processing TDM data are synchronized to one clock reference. The clock reference can be derived from multiple sources and then routed to all the devices. The following clocking sources are supported by Sleipnir-1-PCI:

- OTX_CLOCK_SOURCE_INTERNAL - On-board free running oscillator
- OTX_CLOCK_SOURCE_LOCAL_0 - Clock extracted from the incoming T1/E1/J1 span 0 (LI0)
- OTX_CLOCK_SOURCE_LOCAL_2 - External 2.048 MHz clock (J9 connector)

The J8 connector can be used to output the Sleipnir-1-PC104-Plus clock reference (2.048 MHz) to another device or equipment. Please see Table 3.

Table 3 - Clock Reference Input

Pin	
1	Reference clock Input (2 MHz)
2	Ground

The J9 connector supplies the currently used clock to an external device. Please see Table 4 below:

Table 4 - Reference Clock Output

Pin	
1	Reference clock Output (2 MHz)

2	Ground

13 JTAG

The JTAG port (reference designator J4) is used for Board Testing, programming of The FPGA PROMS, and Connecting the DSP emulator board for DSP Software Development. Please see Table 5 below:

Table 5 - JTAG Chains

Chain	Parts
TMS0	PROM
TMS1	LI0
TMS2	FPGA,PLX
TMS3	DSP0

To connect the Texas Instruments' Code Composer debugger to the Sleipnir-1-PC104-Plus boards, you need to use the Hermod-JTAG Code Composer Debug Probe, Odin product number HMA-1057-1. Connect Hermod-JTAG to the J4 connector on the OTX PCI adapter. The Code Composer emulator pod can then be connected to the 2x11 pin header on the Hermod-JTAG board.

14 Indicators

The Sleipnir-1-PC104-Plus has four LED indicators visible from the side of the board. One of the LED is controlled by the DSP (using the C55X_SET_LED0_OFF and C55X_SET_LED0_ON macros in the OTX C55x DSP SDK), while the other three LEDs have control bits in the FPGA and are associated with the LIU.

The location and function of the four LEDs are shown in the figure below:

Li0 ALARM ○ ○ Li0 FRM ERR

Dsp0 LED0 ○ ○ Li0 LOS/ACT
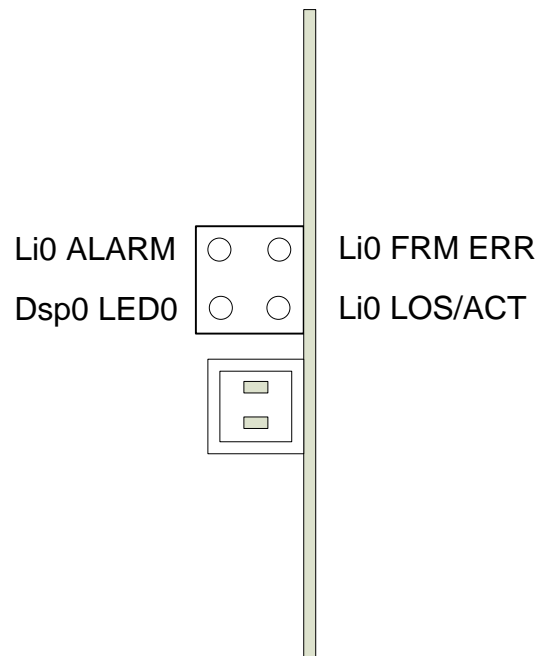
There is also a smaller surface mount LED which is populated directory on the PCB. This LED is controlled by the DSP (using the C55X_SET_LED2_OFF and C55X_SET_LED2_ON macros in the OTX C55x DSP SDK, and are typically used as "heartbeat" LEDs indicating that a DSP program is running. D101 is the LED for DSP0.

The LOS/ACT LED can have three states. Please see Table 6:

Table 6 - LOS/ACT LED

Color	Indicating
Blinking Red	Driver is not yet loaded
Steady Green	Signal (voltage) is present on the T1/E1 span
Steady Red	LOS (Loss Of Signal)

The FRM ERR LED can have the following four states. Please see Table 7:

Table 7 - FRM ERR LED

Color	Indicating
Blinking Red	Frame Error
Steady Red	Frame Error and Multi-Frame Error

Color	Indicating
Blinking Green	Error Count
Blinking Yellow	Multi-Frame Error

The ALARM LED can have three states. Please see Table 8:

Table 8 - ALARM LED

Color	Indicating
Blinking Red	Blue Alarm
Blinking Green	Yellow Alarm and Blue Alarm
Blinking Yellow	Yellow Alarm

15 Power

The Sleipnir-1-PC104-Plus operates from 3.3 Volt or 5V power supplied from the host PC. Power consumption is TBD.

16 Certifications

Final certifications are TBD. The Sleipnir-1-PC104-Plus will be designed with the following list of planned certifications:

- FCC Part 15 (CFR47, Part 15, Subpart B)

- FCC Part 68

- CE EMC (EN61326-1 Class B Equipment, AS/NZS 2064 Class B Limits)

- Safety EN60950 and UL60950

17 Reference documents

The following documents provide further detailed information related to the Sleipnir-1-PC104-Plus board:

- Programmer's Guide for OTX Hardware Driver (Odin document # 1412-1-SAA-1006-1)

- Programmer's Guide for OTX C54x DSP Software Development Kit (Odin document number 1412-1-SAA-1007-1)

18 Glossary

OTX – Odin Telecom FrameworX

DSP – Digital Signal Processor (optional device on Sleipnir-1-PC104-Plus)

SDK – Software Development Kit (supplied with the Sleipnir-1-PC104-Plus with a DSP installed)

API – Application Programmer Interface

CPU – Central Processing Unit. Refers to the host PC in this document.

EEPROM – Electrically Erasable Programmable Read Only Memory.

FPGA – Field Programmable Gate Array.

LED – Light Emitting Diode

LS – Least Significant

MS – Most Significant