



Thor-2-PCI-Plus Technical Description

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Table of Contents

1	Abstract	5
2	Thor-2-PCI-Plus Overview	6
3	Physical specifications	7
4	Data Architecture	8
5	PCM Highways	10
6	API Supported Physical Devices	11
6.1	Board Devices.....	11
6.2	T1/E1 Line Interface Device	11
6.3	ASM	11
7	Line Interface Functionality	12
7.1	Line Configurations.....	12
7.2	Fault Monitoring	12
7.3	Loop Back.....	13
8	Testing features.....	14
9	External Interfaces	14
9.1	PCI Bus.....	14
9.2	T1 / E1 Interface Connections	15
9.3	Clocks.....	18
9.4	JTAG	18



10 Indicators..... 19

11 Power 19

12 Certifications..... 19

13 Reference documents..... 19

14 Glossary 21

15 Support Information 21



1 Abstract

This document provides a technical description of Odin TeleSystems' Thor-2-PCI-Plus adapter card. This presentation is targeted to systems integrators and application developers who are developing telecommunications systems and/or software applications using the Thor-2-PCI-Plus platform. The purpose of this document is to provide the needed information about the hardware to allow software developers to efficiently integrate Thor-2-PCI-Plus into their overall system under design.

For information on how to develop host applications utilizing the OTX Hardware Device Driver Application Programming Interface (API), please refer to the "Programmer's Guide for OTX Hardware API" document (Odin TeleSystems Inc. document number 1411-1-SAA-1006-1). For information on how to develop custom DSP applications, please refer to "Programmer's Guide for OTX C54x DSP Software Development Kit" (Odin document number 1412-1-SAA-1007-1). And finally, for help on how to install the Thor-2-PCI-Plus card and the OTX Device Driver Software, please refer to the Installation Guide for OTX PCMCIA Adapters (Odin TeleSystems Inc. document number 1512-1-HCA-1003-1).



2 Thor-2-PCI-Plus Overview

Thor-2-PCI-Plus is multi-purpose T1/E1 interface adapter. The Thor-2-PCI-Plus card allows Personal Computers (PCs) and other systems with a PCI bus to be interfaced with T1/E1 links.

Thor-2-PCI-Plus is a member of the Odin Telecom frameworkX (OTX+) product family. Thor-2-PCI-Plus is supported by the OTX device driver and by the OTX Hardware Application Programming Interface (API). Equipped with the appropriate OTX software modules, Thor-2-PCI-Plus can be utilized in a variety of T1/E1, Integrated Services Digital Network (ISDN), Frame Relay, and Signaling System #7 (SS#7) applications.

The Thor-2-PCI-Plus supports two (2) T1 or E1 interfaces at the speeds of 1.544 Mbps and 2.048 Mbps, respectively. Throughout the document the T1/E1 interfaces are referred to as Line Interfaces (LIs). The same board supports both T1 and E1. The operation mode as well as the line terminating impedance of 75 ohms or 100 ohms are software switchable. The card also supports a high-impedance mode with external 20db amplifier for monitoring. Consequently, the Thor-2-PCI-Plus card can be used to terminate two (2) T1/E1 links or to monitor one (1) link.

The Thor-2-PCI-Plus provides H.100 Computer Telephony Bus. The H.100 bus comprises of thirty-two (32) 2, 4, or 8 Mbit/s Time-Division Multiplexed (TDM) highways for board-to-board communication. On the Thor-2-PCI-Plus board the H.100 highways are connected to a non-blocking time-space switch. The time-space switch allows 512 time-slots to be switched between H.100 highways and the local highways. 1024 time-slots can be switched locally between on-board devices. The H.100 bus is backwards compatible with the MVIP bus and the SCBus.

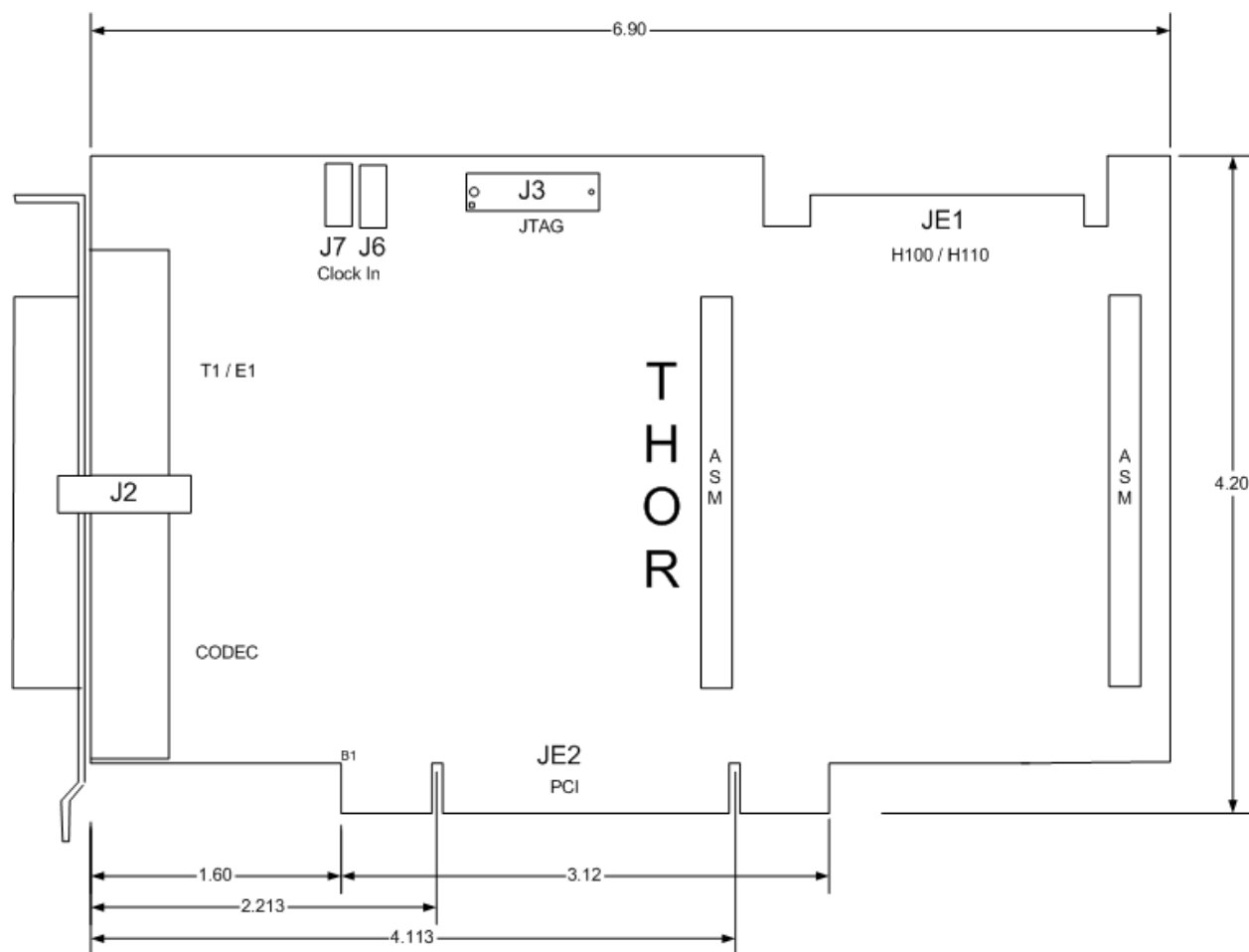
The Thor-2-PCI-Plus board also contains an OTX Application Specific Module (ASM) socket. The ASM interface can be used to add daughter boards providing additional resources. For example, Thor-2-PCI-Plus can be augmented with Vidar-55x4-ASM providing 4 TI TMS320C5510 Digital Signal Processors (DSPs). By loading and running different programs in these DSPs, the Thor-2-PCI-Plus adapter can support a variety of different telecom functions, such as tone detection and generation, HDLC sending and receiving, voice encoding and decoding, etc.

Finally, Thor-2-PCI-Plus contains four (4) codecs. The codecs perform Analog-to-Digital (A/D) and Digital-to-Analog (D/A) conversions. Both the A-law and the u-law are supported. The codecs can be switched to any time-slots on the board. Standard handsets can be connected to the codecs to provide phone functionality.



3 Physical specifications

Thor-2-PCI-Plus is a half-length PCI board.



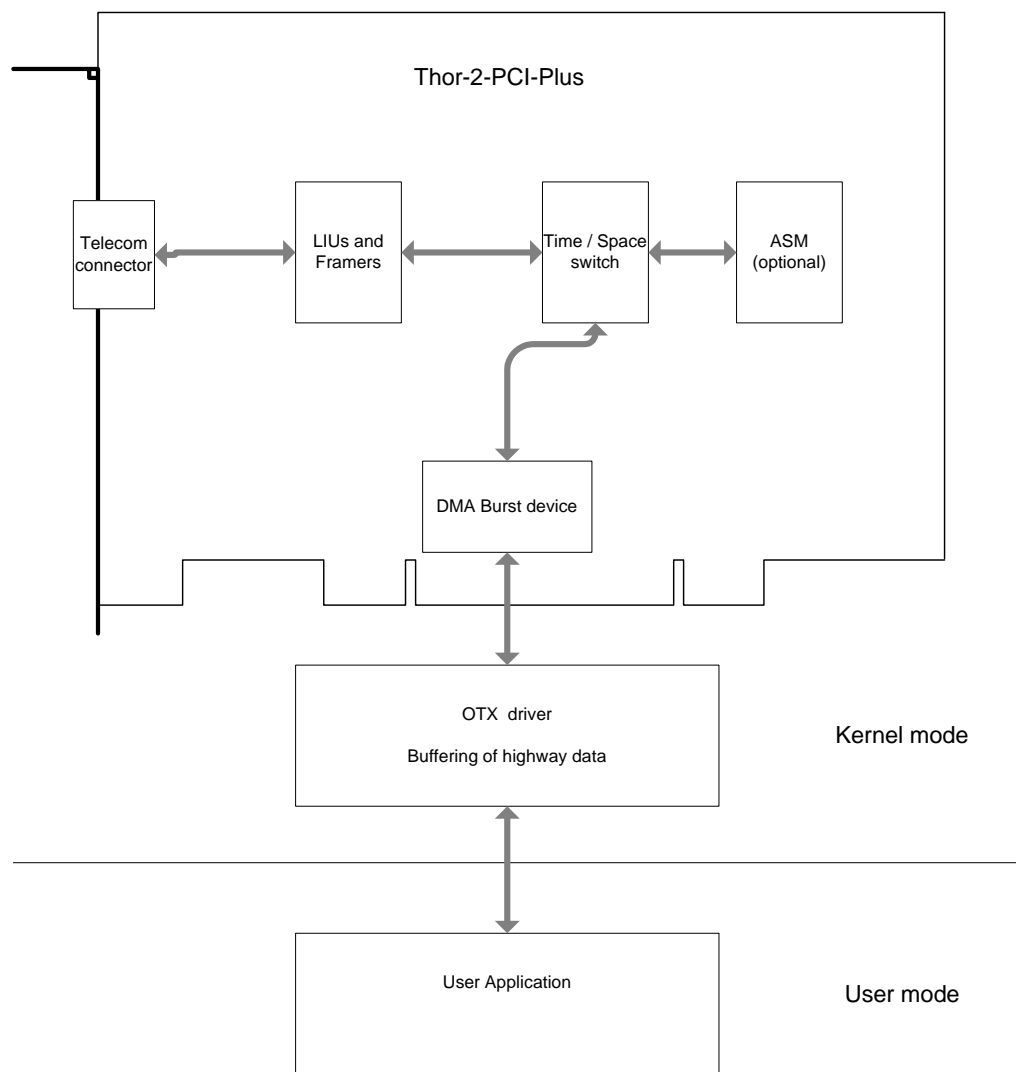
Thor-2-PCI Plus PCB
Mechanical



4 Data Architecture

Internally, Thor-2-PCI-Plus utilizes serial TDM (Time-Division Multiplexed) data streams for transfer of data or voice. The internal serial TDM data streams are called “Highways.” The external interface is referred to as “span”.

The serial highways provide data paths between physical devices as shown in the figure below.





5 PCM Highways

The Thor-2-PCI-Plus internal highways are configured to operate at either 2, 4, or 8 Mbit/s, each containing 32, 64 or 128 8-bit time-slots, respectively. The data rate of one time-slot is 64 kbit/s. The Table below lists the internal highways used on Thor-2-PCI-Plus boards.

Highway #	Connecting Time-Space Switch to
0,1	2.048 Mbits/s Highway connecting to LI#0, LI#1
4,5	2.048 Mbits/s Highway connecting to DMA
7	2.048 Mbits/s Highway connecting to quad CODEC
8-11	2.048 Mbits/s Highway connecting to the ASM

The time-space switch is non-blocking and allows any internal time-slot on any internal highway to be switched to any other highway/time-slot. The cross-connections are software programmable and automatically taken care of by the OTX driver.

In addition, the Thor-2-PCI-Plus contains 32 H.100 Highways:

The Thor-2-PCI-Plus time-space also provides support multicasting and messaging. In multicasting mode any input channel can be cross-connected to multiple output channels. For example, an incoming Li time slot can be both switched to an outgoing H.100 Highway and it can also be switched to the ASM board.

In the messaging mode, the time-space switch can be instructed to send a constant byte on any time slot. Once activated, every byte on the specified time slot will contain the same value. The generation of constant byte does not consume any processing capacity. The constant byte feature is useful in, for example, verification of a through connection or in Bit Error Rate (BER) testing.



6 API Supported Physical Devices

6.1 Board Devices

The Thor-2-PCI-Plus configuration and status registers are accessible by API calls. The board devices include the serial to parallel converters and the DMA controller. The application can read or write the data directly from the Thor-2-PCI-Plus buffers, or have the DMA controller place the data in the host memory and notify the application when data is available. The Time / Space switch registers are also directly accessible by API calls.

6.2 T1/E1 Line Interface Device

The Thor-2-PCI-Plus Line Interface devices are fully supported by API calls to configure the interface for the required functionality. There is full access to all device registers for monitoring or diagnostics.

6.3 ASM

The optional DSPs on the Thor-2-PCI-Plus ASM module can be used to run Odin provided standard DSP applications or they can be used to run user developed custom applications. The Thor-2-PCI-Plus with its ASM is delivered with a number of Odin's Signal Processing Module (SPM). These SPMs, or DSP application packages, provides supports for many common telecom applications; such as tone detection and generation, FSK detection, and HDLC sending and receiving.

For more information on custom DSP application development, please refer to "*Programmer's Guide for OTX C54x DSP Software Development Kit*" (Odin document number 1412-1-SAA-1007-1)



7 Line Interface Functionality

7.1 Line Configurations

The Thor-2-PCI-Plus line interfaces support several different line codes:

- HDB3 - High Density Bipolar 3
- B8ZS - Bipolar 8 Zero Substitution
- AMI - Alternate Mark Inversion
- AMI with NZC

For the T1 operation mode, the following framing formats can be used:

- F4 - 4-frame multiframe
- F12 - 12 frame multiframe (D3/D4, Superframe)
- ESF - Extended Superframe
- F72 - 72 frame multiframe (SLC96 mode)

For the E1 operation mode, Thor-2-PCI-Plus supports the following framing formats:

- Doubleframe
- CRC multiframe

7.2 Fault Monitoring

The line interface subsystem supports fault and performance monitoring. The transceiver subsystem detects and reports the following alarms in the receive streams:

- Framing errors
- Cyclic Redundancy Check (CRC) errors
- Code violations
- Loss of frame alignment



- Loss of Signal (LOS)
- Alarm Indication Signal (AIS)
- E bit errors (E1 only)
- Slip
- Remote Alarm Indication (RAI, Yellow Alarm)

The line interface subsystems also supports the transmitting of the following alarms towards the remote end:

- Alarm Indication Signal (AIS)
- Remote Alarm Indication (RAI, Yellow alarm)
- Auxiliary Pattern (AUXP)

7.3 Loop Back

The line interface subsystem implements a remote loop back for line testing. In the remote loop back mode, the clock and data recovered from the line inputs are routed back to the line outputs through the analog transmitter.



8 Testing features

The Thor-2-PCI-Plus Telecom configuration offers a variety of features to facilitate low-level T1/E1/J1 testing:

- Full access to F, Y, Si, and Sa bits in E1 mode
- Full access to FS/DL-bits in T1 mode (including support for the DL-channel protocol according to T1.403-1989 ANSI or to AT&T TR54016 specification)
- Programmable line build-out in T1/J1 mode
- Transparent mode
- Programmable transmit pulse shape and receive input threshold
- Insertion and detection of single alarms (e.g. Code Violation, Framing Errors, etc)
- Support for generation and detection of Loop codes
- Support for channel loopback
- Support for PRBS (BERT patterns)

9 External Interfaces

9.1 PCI Bus

The Thor-2-PCI-Plus board is compliant with the PCI 2.1 local bus specification. It is a universal interface, supporting both 3.3 volt and 5 volt signaling. The Thor-2-PCI-Plus supports 32 bits at 33 MHz and can be both Slave and Master.



9.2 T1 / E1 Interface Connections

The back panel of Thor-2-PCI-Plus contains a Centronics connector with 50 contacts. The Centronics connector provides the following interfaces:

- 2 T1/E1 4-wire Line Interfaces
- 4 Analog Interfaces for Handsets

Figure 2 below lists the interface connections.

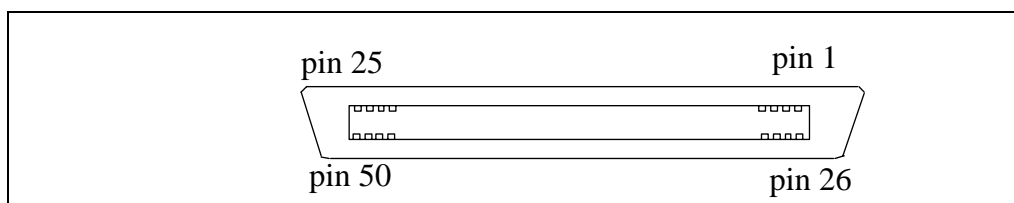


Figure 2. Centronics connector.

**Table 2 T1 /E1 Interface connections, Centronics connector**

Pin	Signal	Pin	Signal
1	Handset 0 Speaker -	26	Handset 0 Speaker +
2	Handset 0 Microphone +	27	Handset 0 Microphone -
3	No connection	28	No connection
4	Handset 1 Speaker -	29	Handset 1 Speaker +
5	Handset 1 Microphone +	30	Handset 1 Microphone -
6	No connection	31	No connection
7	Handset 2 Speaker -	32	Handset 2 Speaker +
8	Handset 2 Microphone +	33	Handset 2 Microphone -
9	No connection	34	No connection
10	Handset 3 Speaker -	35	Handset 3 Speaker +
11	Handset 3 Microphone +	36	Handset 3 Microphone -
12	No connection	37	No connection
13	No connection	38	No connection
14	No connection	39	No connection
15	No connection	40	No connection
16	No connection	41	No connection
17	No connection	42	No connection
18	No connection	43	No connection
19	Span 0 Transmit Tip	44	Span 0 Transmit Ring
20	Span 0 Receive Ring	45	Span 0 Receive Tip
21	No connection	46	No connection
22	Span 1 Transmit Tip	47	Span 1 Transmit Ring
23	Span 1 Receive Ring	48	Span 1 Receive Tip
24	No connection	49	No connection
25	No connection	50	No connection



Thor-2-PCI-Plus is delivered with a telco-type connector cable (SCSI Cable) and a Harmonica module which converts from Centronics connector to 2 RJ-45 connectors and 6 RJ-11. The Harmonica module allows the connection of T1/E1 lines and handsets to Thor-2-PCI-Plus using RJ-45 and RJ-11 connectors. The RJ45 T1/E1 interface connections are diagramed below. (See Figure 3).

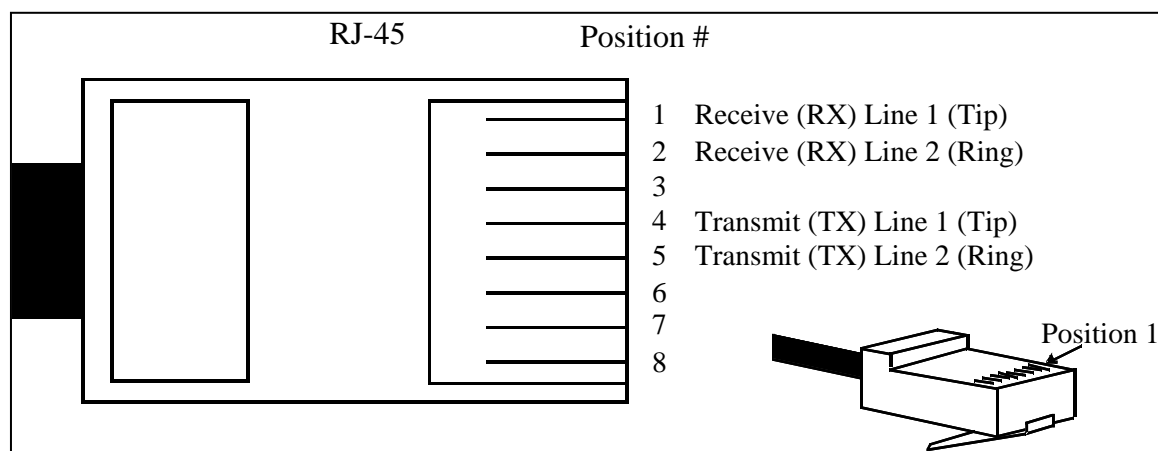


Figure 3. T1/E1 connections.

The RJ-11 Handset interface connections are diagramed below (See Figure 4).

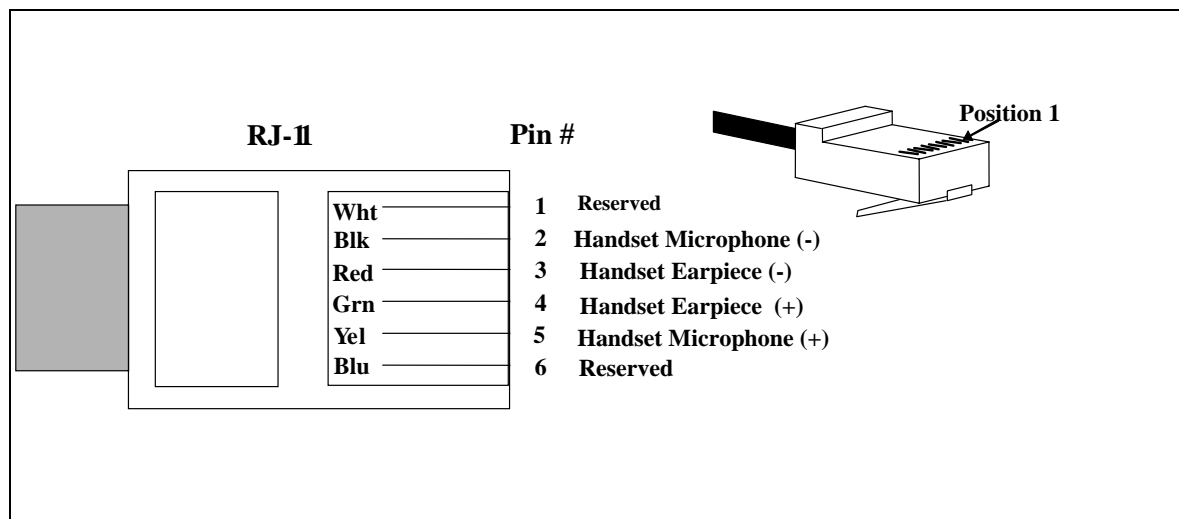


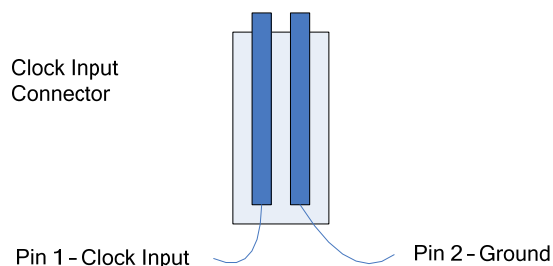
Figure 4. Handset connections.

9.3 Clocks

On the Thor-2-PCI-Plus board, all the internal TDM data highways and the all the devices processing TDM data are synchronized to one clock reference. The clock reference can be derived from multiple sources and then routed to all the devices. The following clocking sources are supported by Thor-2-PCI-Plus:

- OTX_CLOCK_SOURCE_LOCAL_0 - Clock extracted from the incoming Li0 T1/E1/J1 span
- OTX_CLOCK_SOURCE_LOCAL_1 - Clock extracted from the incoming Li1 T1/E1/J1 span
- OTX_CLOCK_SOURCE_INTERNAL - On-board free running oscillator
- OTX_CLOCK_SOURCE_EXTERNAL - The clocks are synchronized to an externally supplied 8kHz clock signal (3.3V - 5V) on connector J6.
- OTX_CLOCK_SOURCE_EXTERNAL_SECONDARY - The clocks are synchronized to an externally supplied 8kHz clock signal (3.3V - 5V) on connector J7.

The locations of the External Clock Input connectors (J6 and J7) are shown in Chapter 3. The pinout of these connectors is shown in the figure below:



9.4 JTAG

The JTAG port (reference designator J3) are used for Board Testing, programming of The FPGA PROMS, and Connecting the DSP emulator board for DSP Software Development.

Table. JTAG Chains

Chain	Parts
TMS0	PROM
TMS1	LIU_0, LIU_1, PCI,T-S_SW
TMS2	ASM



TMS3	ASM
TMS4	FPGA

10 Indicators

The Thor-2-PCI-Plus has two red LED indicators (D18 and D17) located in the upper left hand corner. Each LED is connected to the RPB pin of the E1/T1 devices. D18 is connected to Li0, and D17 is connected Li1. The RPB pin can be programmed to output various E1/T1 status information. Please contact Odin Support for further information of how to program these LED indicators.

11 Power

The Thor-2-PCI-Plus operates from 3.3 Volt and 5 volt power supplied from the host PC. Power consumption is TBD.

12 Certifications

Final certifications are TBD. The following is a list of planned certifications:

- FCC Part 15 (CFR47, Part 15, Subpart B)
- FCC Part 68
- CE EMC (EN61326-1 Class B Equipment, AS/NZS 2064 Class B Limits)
- Safety EN60950 and UL60950

13 Reference documents

The following documents provide further detailed information related to the Thor-2-PCI-Plus board:

- Programmer's Guide for OTX Hardware Driver (Odin document # 1412-1-SAA-1006-1)
- Installation Guide for OTX PCI Adapters (Odin document number 1512-1-HCA-1001-1)



- Programmer's Guide for OTX C54x DSP Software Development Kit (Odin document number 1412-1-SAA-1007-1)



14 Glossary

OTX – Odin Telecom FrameworkX

DSP – Digital Signal Processor (optional device on Thor-2-PCI-Plus)

SDK – Software Development Kit (supplied with the Thor-2-PCI-Plus Telecom configuration)

API – Application Programmer Interface

CPU – Central Processing Unit. Refers to the host PC in this document.

EEPROM – Electrically Erasable Programmable Read Only Memory.

FPGA – Field Programmable Gate Array.

LED – Light Emitting Diode

LS – Least Significant

MS – Most Significant

15 Support Information

For more information on this product, please contact:

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