Odin TeleSystems Inc.

Technical Description for Thor-2, Rev. 1.0

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1. Table of Contents

2. Abstract

This document provides a technical description of Odin TeleSystems' Thor-2 adapter card. This presentation is targeted to designers who are developing applications for the Thor-2 platform. The document concentrates on describing the main technical capabilities of the Thor-2 board. For information on how to use these capabilities under software control, please refer to the *Thor Application Programming Interface (API) Reference Guide* (Odin TeleSystems Inc. document number 1211-1-SDA-1001-1). For more information on how to install and configure the Thor-2 board, please refer to the *Thor-2 User Guide* (Odin TeleSystems Inc. document number 1412-1-HAA-1004-1).

3. Introduction to Thor-2

Odin TeleSystems' Thor-2 board is a T1/E1 Integrated Services Digital Network (ISDN) and Frame Relay ISA interface card for Personal Computers. The intended use of the Thor board is in ISDN Primary Rate (PRI), Frame Relay, and Signaling System #7 (SS#7) test equipment and subsystems.

A PC equipped with the Thor-2 board can be connected directly to a T1 or E1 interface carrying ISDN Primary Rate, Frame Relay, or SS7 traffic. The Thor board utilizes ISDN Primary Rate transceivers which can be switched to operate in T1 (1.544 Mbps) or E1 (2.048 Mbps) rates compliant to ANSI T1.408 and ITU-T G.703, G.704 specifications, respectively. In this document the transceivers are called "Line Interfaces." The Thor-2 board contains two of these line interfaces: Abbreviated Li-0 and Li-1.

Internally, Thor-2 utilizes serial data streams for data transfer. The internal serial data streams are called "Highways." On the Thor-2 board a highway is always a 2.048 Mbit/s bi-directional bit stream. One highway consists of 32 channels (8-bit timeslots), each having a data rate of 64 Kbit/s. All together, the Thor-2 board contains 12 separate internal highways and 384 channels.

All the internal highways are connected to a time-space switch. The 384x384 time-space switch allows any channel on any highway to be cross-connected to any other channel on any other highway. Two of the highways (64 channels) originate from the line interfaces. These highways are called "Li Highways." Eight of the highways are connected to the Multi Vendor Integration Protocol (MVIP) interface. These highways are called "MVIP Highways." One of the highways, the "Aux Highway," is connected to the auxiliary devices (Codecs and DTMF transceivers). And finally, the last internal highway is connected to the High Level Data Link Controller (HDLC). This highway is called "Control Highway."

All the internal highways are synchronized to one clock reference. The clock source can be selected with software from one of the following alternatives: Either of the incoming T1/E1 spans, MVIP bus master clock signal, MVIP bus secondary clock signal, External clocking reference, or On-board Oscillator.

The Thor-2 board supports digital data and voice communications. It can send and receive data as data streams or as data packets. The packetizing is performed by the on-board HDLC Controller. The HDLC controller sends and receives data through “Pipes.” A pipe is a bit-stream with a data rate between 8 Kbit/s and 2.048Mbit/s. A pipe is a configured entity and it is overlaid onto the internal highways. A pipe can constitute a single channel on the board or it can be a superchannel of any number of time slots, which do not have to be consecutive in a highway. Or alternatively, a pipe can be configured as a lower speed subchannel within a time-slot. Up to 32 different pipes can be established with the combined maximum data rate of 2.048 Mbit/s. One end of a pipe always terminates at the HDLC controller while the other end of the pipe can be switched to a T1/E1 span or to the MVIP interface.

The data sent and received in the pipes is stored in the shared memory. The data from the shared memory is accessible by the host processor via the ISA bus or by the on-board processor.

For voice applications the Thor-2 board also includes two Codecs and two Dual Tone Multi Frequency (DTMF) transceivers. The Codecs perform Analog-to-Digital (A/D) and Digital-to-Analog (D/A) conversions. Both the A-law and the u-law are supported. The codecs can be switched to any time-slots on the board. Standard handsets can be connected to the codecs to provide full digital phone functionality. The DTMF transceivers can be used to send and receive DTMF tones and to recognize call progress tones. The transmitted frequencies are programmable with software.

Up to four Thor-2 boards can be placed into one PC. These boards can be connected together within the PC chassis using the MVIP interface. The MVIP interface provides a standardized external bus containing eight bi-directional 2.048 Mbit/s serial data streams. The MVIP interface makes it possible to cross-connect any time-slot from any Thor-2 board with any other time-slot on any other Thor-2 board or to any other MVIP compliant extension board within the PC chassis. The MVIP interface also facilitates sharing of resources. For example, all of the boards can share and utilize the HDLC controller, codecs, or DTMF transceivers from any other board within the MVIP bus.

The Thor-2 board contains an on-board microprocessor: Intel 386 EX. Within this document the on-board processor is called the “Local Processing Unit,” or “LPU.” The PC’s main processor is called the “Central Processing Unit,” “CPU,” or simply the “Host.” The Thor-2 board can be operated as an active card under LPU control or as a passive card under CPU control.

For storage Thor-2 utilizes standard Single Inline Memory Modules (SIMMs). The board can be equipped with 1 MByte, 2 MBytes, or 8 MBytes of memory. The board also contains 512 KBytes of Flash memory which can be used for persistent storage.

4. System Overview

The Thor-2 board consists of the following subsystems:

1. Line Interface Subsystem
2. Transceiver Subsystem
3. Signaling Subsystem
4. Switching Subsystem
5. Processor Subsystem
6. Software Driver Subsystem

The Thor-2 subsystems are illustrated in Figure 1 on page 9. The different subsystems are introduced in the following subchapters and are described in more detail in the subsequent chapters.

4.1 Line Interface Subsystem

The Line Interface subsystem is responsible for interfacing with the T1/E1 network. The subsystem provides the connectors, terminating resistors, transformers, and over-voltage protection.

4.2 Transceiver Subsystem

The transceiver subsystem implements the send and receive line interface functions. These functions include data and clock recovery, as well as local and remote diagnostics loops. The subsystem is also responsible for frame alignment and synthesis, line coding, error checking, as well as insertion and extraction of alarms and facility signaling.

4.3 Signaling Subsystem

The signaling subsystem is responsible for the management of High-Level Data Link Control (HDLC) signaling channels within the transmit and receive frames. The signaling subsystem also contains Codecs implementing the phone functionality and DTMF transceivers for inband tone signaling (sending and receiving).

4.4 Switching Subsystem

The switching subsystem provides a time-space switch for the switching of any incoming time/slot to any outgoing time slot. This subsystem is also responsible for delivering and switching of the on-board clock signals.

4.5 Processor Subsystem

The processor subsystem consists of the on-board processor and on-board memory; Dynamic Random Access Memory (DRAM) and Flash. The processor subsystem also contains the processor buses.

4.6 Software Driver Subsystem

The software driver subsystem consists of the CPU and the LPU software. The CPU software contains the Thor-2 driver that allows the host processor to communicate with the board. The LPU software contains the boot-strap routine and the monitor (operating system) for the on-board processor.

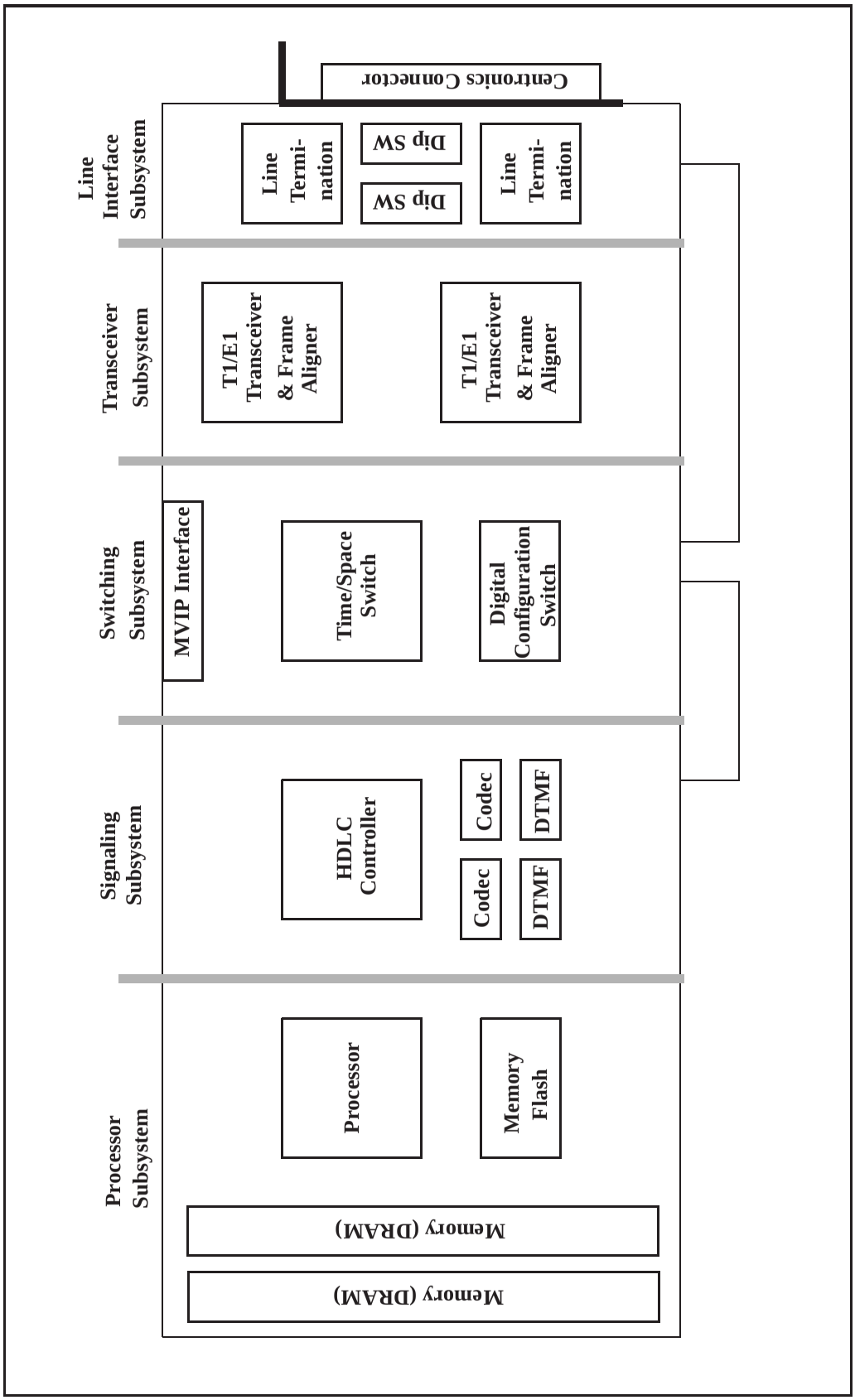

Figure 1. Thor-2 Subsytems

5. Line Interface Subsystem

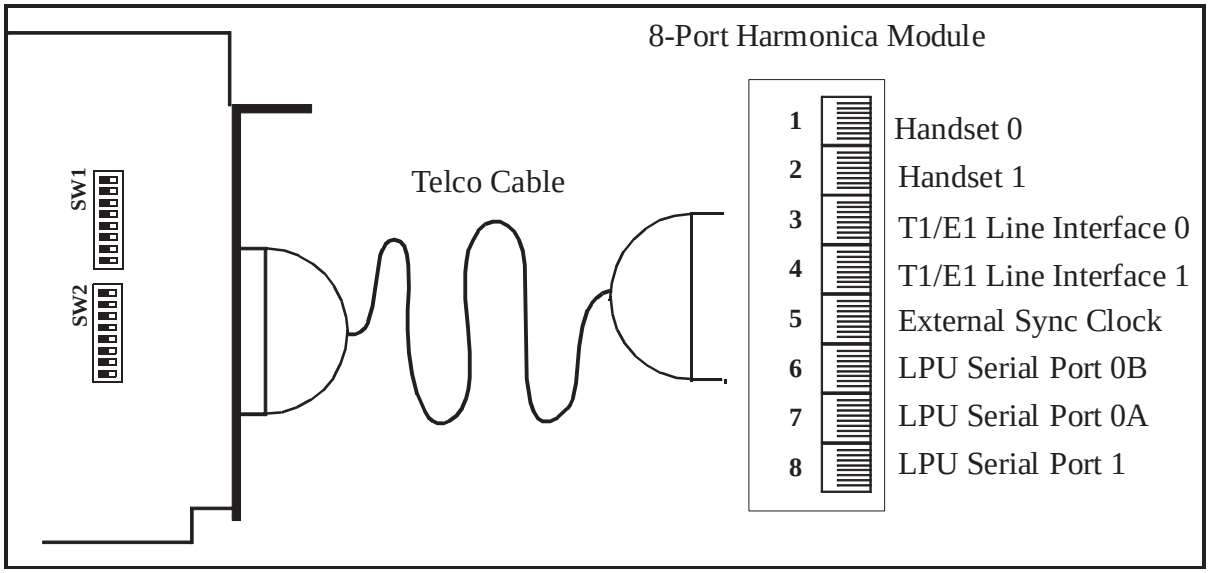

Figure 2. Overview of the Line Interface Subsystem

The line interface subsystem interfaces with the T1/E1 network and with the auxiliary devices through the Thor-2 back panel. The back panel contains a Centronics connector with 50 contacts. Thor-2 is delivered with a telco-type connector cable and a Harmonica module which converts from Centronics connector to 8 RJ-11 connectors. The Harmonica module allows the connection of T1/E1 lines, handsets, speakers, external synchronization clocks, and serial lines to Thor-2 using RJ-11 connectors (See Figure 2 on page 10).

Although Thor-2 is delivered with the RJ-11 Harmonica module, the modular structure of Thor-2 allows it to be adapted for other types of connectors as well. For example, if the application requires BNC or Bantam type connectors, the Harmonica module can be replaced with another type of adapter which converts from Centronics to BNC or Bantam type connectors. The pin-outs of the Centronics and the RJ-11 connectors are documented in Figure 3 on page 11 and Table 1 on page 11. For detailed documentation on the pin-outs of the RJ-11 connectors in the Harmonica, please refer to the *Thor-2 User Guide*.

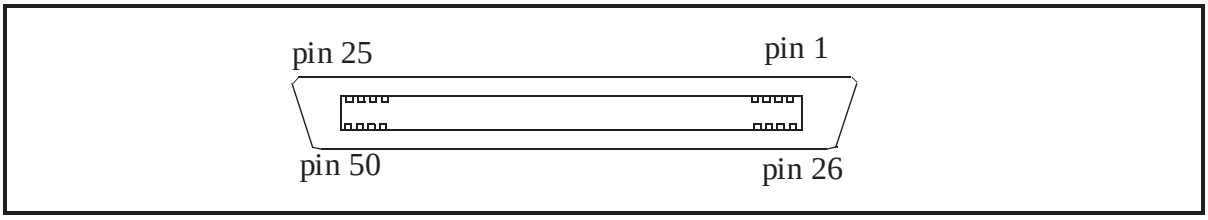

Figure 3. Thor-2 Centronics Connector

TABLE 1. Thor-2 Centronics Connector Pin Assignments

Pin	Signal	Pin	Signal
1	Codec-0, Handset Earpiece (-)	26	Codec-0, Handset Earpiece (+)
2	Codec-0, Handset Microphone (+)	27	Codec-0, Handset Microphone (-)
3	Codec-0, Speaker (+)	28	Codec-1, Speaker (-)
4	Codec-1, Handset Earpiece (-)	29	Codec-1, Handset Earpiece (+)
5	Codec-1, Handset Microphone (+)	30	Codec-1, Handset Microphone (-)
6	Codec-1, Speaker (+)	31	Codec-0, Speaker (-)
7	Line Interface 0, Transmit Line (tip)	32	Line Interface 0, Transmit Line (ring)
8	Line Interface 0, Receive Line (ring)	33	Line Interface 0, Receive Line (tip)
9	Reserved	34	Reserved
10	Line Interface 1, Transmit Line (tip)	35	Line Interface 1, Transmit Line (ring)
11	Line Interface 1, Receive Line (ring)	36	Line Interface 1, Receive Line (tip)
12	Reserved	37	Reserved
13	External Synch clock 1.544 or 2.048 MHz	38	External Synch Clock, 8 kHz
14	Ground	39	Ground
15	Reserved	40	Reserved
16	LPU Com0, Data Terminal Ready (DTR)	41	LPU Com0, Data Set Ready (DSR)
17	LPU Com0, Data Carrier Detected (DCD)	42	LPU Com0, Ring Indicator (RI)
18	Reserved	43	Ground
19	LPU Com0, Transmit Data (TXD)	44	LPU Com0, Receive Data (RXD)
20	LPU Com0, Clear to Send (CTS)	45	LPU Com0, Request to Send (RTS)
21	Reserved	46	Ground
22	LPU Com1, Transmit Data (TXD)	47	LPU Com1, Receive Data (RXD)
23	Reserved	48	Reserved
24	Reserved	49	Ground
25	Reserved	50	Reserved

The line interface subsystem also contains the terminating resistors for line termination. Different characteristics impedance for the T1/E1 electrical interface can be set with dip switches on the board. The possible line terminations are summarized in Table 2 on page 12.

TABLE 2. Possible Thor-2 Line Terminations

Application	Characteristic Impedance
DS1	100 Ohms
T1	100 Ohms
E1	120 Ohms
E1	75 Ohms
Monitor (T1 or E1)	High

6. Transceiver Subsystem

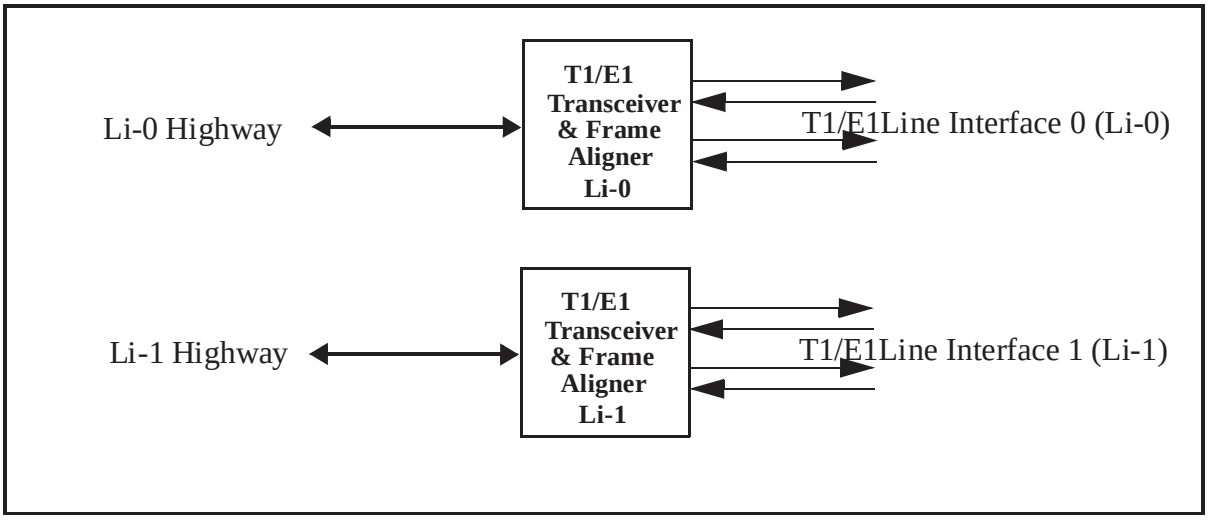

Figure 4. Overview of the Transceiver Subsystem

The transceiver subsystem of Thor-2 provides the analog receive and transmit circuitry for E1 and DSX-1 (T1) signals. It also converts the T1/E1 signals into 2,048 Kbit/s internal Li Highways.

6.1 Line Configurations

The transceiver subsystem of Thor-2 supports several different line codes:

- HDB3 - High Density Bipolar 3
- B8ZS - Bipolar 8 Zero Substitution
- AMI - Alternate Mark Inversion
- AMI with NZC

For the T1 operation mode, the following framing formats can be used:

- F4 - 4-frame multiframe
- F12 - 12 frame multiframe
- ESF - Extended Superframe
- F72 - 72 frame multiframe

For the E1 operation mode, Thor-2 supports the following framing formats:

- Doubleframe
- CRC multiframe

6.2 Fault Monitoring

The transceiver subsystem supports fault and performance monitoring. The transceiver subsystem detects and reports the following alarms in the receive streams:

- Framing errors
- Cyclic Redundancy Check (CRC) errors
- Code violations
- Loss of frame alignment
- Loss of Signal (LOS)
- Alarm Indication Signal (AIS)
- E bit errors (E1 only)
- Slip
- Remote Alarm Indication (RAI, Yellow Alarm)

The transceiver subsystems also supports the transmitting of the following alarms towards the remote end:

- Alarm Indication Signal (AIS)
- Remote Alarm Indication (RAI, Yellow alarm)
- Auxiliary Pattern (AUXP)

6.3 Loopbacks

The transceiver subsystem implements a remote loopback for line testing. In the remote loopback mode, the clock and data recovered from the line inputs are routed back to the line outputs through the analog transmitter.

7. Switching Subsystem

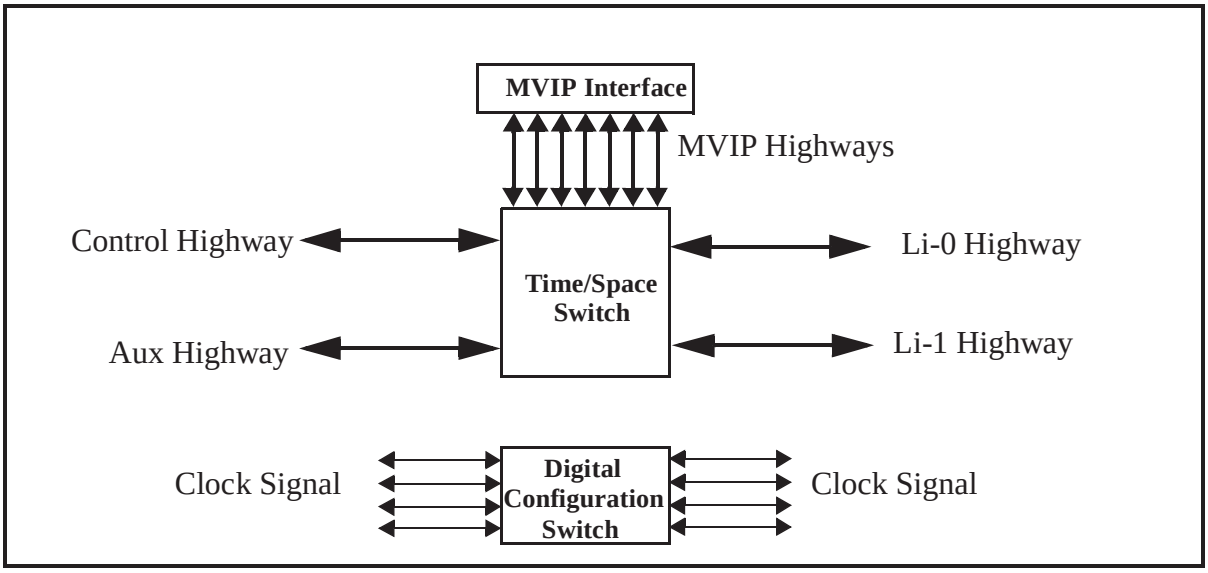

Figure 5. Overview of the Switching Subsystem

The Switching subsystem of Thor-2 consists of two different switching functions. The time-space switch is used to switch the data transmitted on the internal highways. In addition, Thor-2 utilizes a digital configuration switch which is used to switch the clocking source for the board. The two different types of switching, the data switching and the clock switching are discussed in more detail in the following subchapters.

7.1 Data Switching

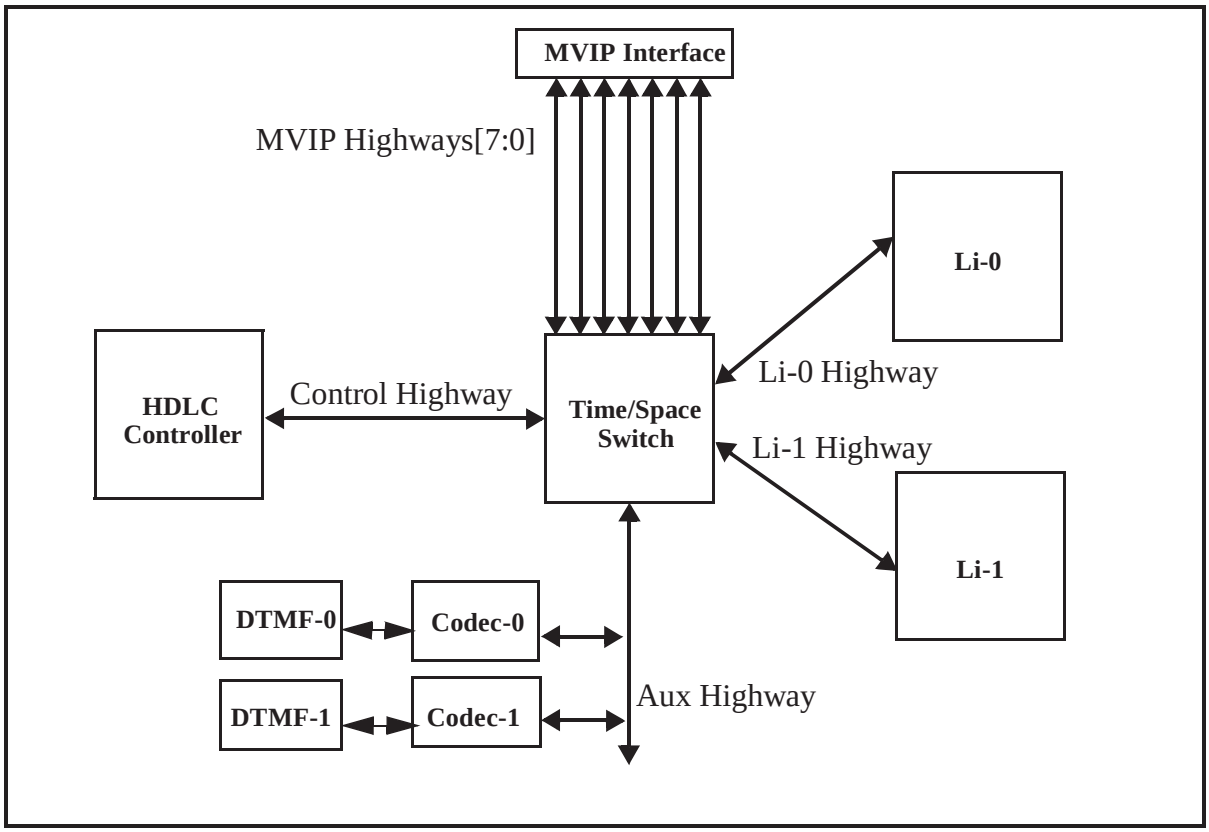

Figure 6. Thor-2 Data Switching Architecture.

Internally, the Thor-2 board transfers user data using serial data streams or “Highways.” Each highway is a 2.048 Mbit/s bi-directional bit stream containing 32 channels (8-bit time-slots). The data rate of one channel is 64 Kbit/s. As shown in Figure 6 on page 16, Thor-2 has 12 separate highways: 2 Li Highways, 8 MVIP Highways, the Auxiliary (Aux) Highway, and the Control Highway. All of the highways are connected to the time-space switch. The time-space switch has a 384x384 channel capacity and provides switching of data from any input channel to any output channel. The cross-connections are software programmable.

The Thor-2 time-space also supports multicasting and messaging. In multicasting any input channel can be cross-connected to multiple output channels. For example, an incoming Li time slot can be both switched to an outgoing MVIP Highway and it can also be switched to the Aux Highway for the monitoring of DTMF tones.

In the messaging mode, the time-space switch can be instructed to send a constant byte on any time slot. Once activated, every byte on the specified time slot will contain the same value. The generation of constant byte does not consume any processing capacity from the CPU or the LPU. The constant byte feature is useful in, for example,

verification of a through connection or in Bit Error Rate (BER) testing.

7.2 Clock Switching

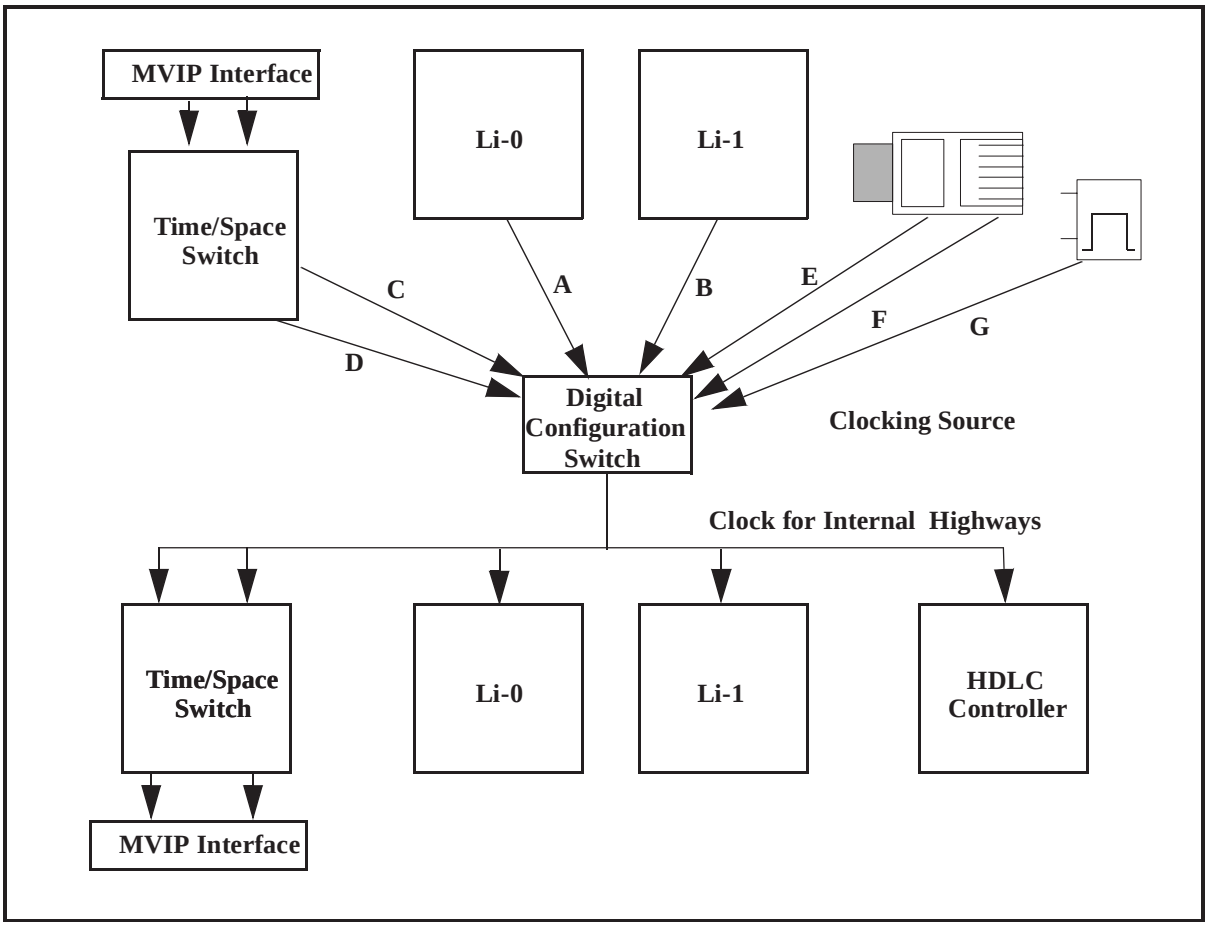

Figure 7. Thor-2 Clock Switching Architecture

As explained in the previous chapter, data on the Thor-2 board is transmitted using internal highways. All of the internal highways are connected to the time-space switch (See Figure 6 on page 16). Consequently, all of the devices on the Thor-2 that are connected to the data highways must be synchronized to the same clocking source. The clocking for the internal highways can be derived from multiple sources and the source to be used can be selected by software. The possible clocking sources are listed in Table 3 on page 18.

TABLE 3. Thor-2 Clocking Sources

Clock Source	Description
A	8 kHz frame clock extracted from the incoming T1/E1 span 0.
B	8 kHz frame clock extracted from the incoming T1/E1 span 1.
C	MVIP bus 8 kHz framing clock
D	MVIP bus 8 kHz secondary clock
E	External 8 kHz framing clock (Connector 6 in the Harmonica)
F	External 2 Mhz bit clock (Connector 6 in the Harmonica)
G	On-board oscillator

In the event that the clocking source is lost, Thor-2 will automatically switch to a backup clocking source. For example, if clocking is derived from an incoming T1/E1 span, and the span experiences Loss of Signal (LOS), the clocking source is automatically switched to the other T1/E1 span. If the other span loses signal as well, then Thor-2 will switch to free-running mode and the clocking will be derived from the on-board oscillator. If the MVIP clocks or the external clocks are used as the clocking source and the clocking is lost, Thor-2 will switch into free-running mode and use the on-board oscillator.

It is important to understand that the difference between the clocks on the external T1/E1 spans and the internal clocks. When the Thor-2 clocking is derived from one incoming T1/E1 span, the external T1/E1 span and the internal highways on-board are completely synchronized. In that case, the other T1/E1 span is not necessarily in synchronization with the internal highways. To compensate for that, Thor-2 implements an elastic receive buffer with a size of 64x8 bits.The elastic store is used to adapt the clock rates between the T1/E1 clock and the Thor-2 system clock, to compensate for input wonder and jitter, and to align the received frame with the internal highway frame. However, the elastic buffer may eventually over- or underflow and a slip condition may occur. When a positive or negative slip occurs, Thor-2 will discard one received layer-1 frame to free space in the elastic receive buffer and to continue forwarding the data from incoming T1/E1 span to the internal highway. The slip condition will cause a one 8-bit data sample to be discarded on all of the time-slots.

7.3 MVIP

Thor-2 supports the Multi-vendor Integration Protocol (MVIP) standard. The MVIP bus is a multiplexed digital telephony highway designed to carry telephone traffic between circuit boards within one PC chassis. The MVIP bus has the capacity of 256 full-duplex 64 kbit/s channels. The channels are combined into 8 2.048 Mbit/s serial data streams. The 8 bi-directional serial streams are carried over 16 physical lines. Within the PC chassis the data streams are passed from card to card using a 40 pin ribbon cable and mass termination connectors on each card.

The MVIP connector is illustrated in Figure 8 on page 19 and the pin-out is listed in Table 1 on page 11.

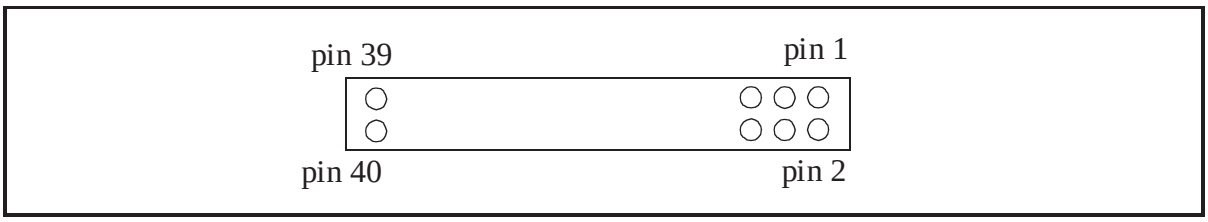

Figure 8. Thor-2 MVIP Connector.

TABLE 4. Thor-2 MVIP Connector Pin Assignments

Pin	Signal	Pin	Signal
1	Reserved	2	Reserved
3	Reserved	4	Reserved
5	Reserved	6	Reserved
7	Digital Stream Out 0 (DSo0)	8	Digital Stream In 0 (DSi0)
9	Digital Stream Out 1 (DSo1)	10	Digital Stream In 1 (DSi1)
11	Digital Stream Out 2 (DSo2)	12	Digital Stream In 2 (DSi2)
13	Digital Stream Out 3 (DSo3)	14	Digital Stream In 3 (DSi3)
15	Digital Stream Out 4 (DSo4)	16	Digital Stream In 4 (DSi4)
17	Digital Stream Out 5 (DSo5)	18	Digital Stream In 5 (DSi5)
19	Digital Stream Out 6 (DSo6)	20	Digital Stream In 6 (DSi6)
21	Digital Stream Out 7 (DSo7)	22	Digital Stream In 7 (DSi7)
23	Reserved	24	Reserved
25	Reserved	26	Reserved
27	Reserved	28	Reserved
29	Reserved	30	Ground
31	/C4	32	Ground
33	/F0	34	Ground
35	C2	36	Ground
37	SEC8K	38	Ground
39	Reserved	40	Reserved

8. Signaling Subsystem

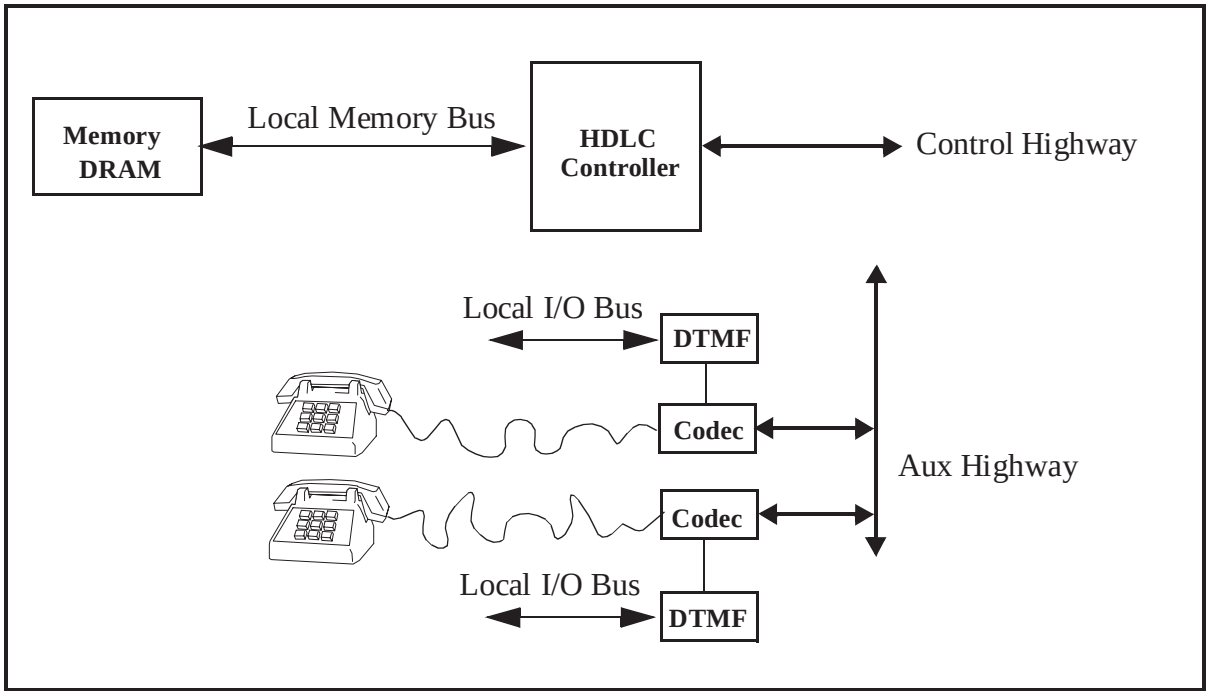

Figure 9. Overview of The Signaling Subsystem

The Thor-2 signalling subsystem consists of a High Level Data Link Controller (HDLC), two codecs, and two DTMF Transceivers.

8.1 HDLC Controller

Thor-2 utilizes a 32-channel HDLC controller. As shown in Figure 9 on page 20, the HDLC controller is connected to the Control Highway and to the local memory bus. The HDLC controller allows data streams and packets to be sent and received by the CPU or by the LPU. The received data is copied into the on-board Random Access Memory (RAM), from where it can be copied into the PC memory or to the hard-disk by the CPU. The data to be sent is first copied into the on-board memory by the LPU or the CPU after which the data can be sent by the HDLC controller.

The HDLC controller sends and receives data through “pipes.” A pipe is a bit-stream with a data rate between 8 Kbit/s and 2.048Mbit/s. A pipe is a configured entity and it is overlaid on to the internal highways. A pipe can constitute a single channel on the board or it can be a superchannel of any number of time slots, which do not have to be consecutive in a highway. What this means in practise is, that the whole highway can be configured as one 2.048 Mbit/s pipe, or any number of time slots (less than 32) and in any order can be configured as a pipe. A pipe can also be a configured as a lower speed subchannel within a time-slot. For example, bit 7 in time-slot 13 can be config-

ured as a 8 kbit/s pipe, and HDLC signalling or a data stream can be sent and received over that pipe. The time-space switch can then be used to connect the time-slots related to a specified pipe to an external T1/E1 span or to MVIP highway. Pipes can also be set up to support the standard ISDN H0, H11, and H12 channels. Up to 32 different pipes can be established with the combined maximum data rate of 2.048 Mbit/s. For more information on how to setup and use the pipes, please refer to the *Thor API Reference Guide*.

The Thor-2 HDLC controller can be operated in a transparent or HDLC protocol mode. In the transparent mode, the data stream is sent and received over a specified pipe without any modifications to the data. In the HDLC protocol mode, the Thor-2 HDLC controller detects and generates the HDLC opening and closing flags as well and checks and generates the Cyclic Redundancy Check (CRC). The CRC can be configured as 16 or 32 bits long. The Thor-2 HDLC also supports shared opening and closing flags. This is important as some protocols, e.g. SS#7, assume that the closing flag of an HDLC frame is also an opening flag of the next frame. The Thor-2 HDLC controller can also be operated in transparent CRC mode, where the CRC is not removed by the Controller from the received frames and is not supplied by the HDLC controller for the frames to be sent. The HDLC controller also supports channel inversion.

The maximum frame length supported by the Thor-2 board is 8192 bytes. Thor-2 will detect and report the following error conditions: aborted frame, too long frame, and too short frame (shorter than flags + CRC).

The Thor-2 HDLC Controller operation modes are summarized in detail in Table 5 on page 22.

TABLE 5. Summary of Thor-2 HDLC Controller Operation Modes

Mode	Functionality
HDLC	• Automatic flag detection and transmission • Support for shared opening and closing flags • Generation of '1's or flags for interframe-time-fill. Detection of inter-frame-time-fill change. • Zero bit insertion • Flag stuffing and flag adjustment for rate adaptation. • CRC generation and checking (16 or 32 bits) • Support for transparent CRC operation • Error detection (abort, long frame, CRC error, 2 categories of short frames, non-octet frame content)
Transparent Mode A (TMA)	• Slot synchronous transparent transmission and reception without a frame structure. • Bit overwrite with fill and mask flags. • Flag stuffing, flag detection, and flag generation.
Transparent Mode B (TMB)	• Transparent transmission and reception using frames delimited by 0x00 flags. • Support for shared opening and closing flags. • Flag stuffing, flag detection, and flag generation. • Error detection (non octet frame content, short frame, long frame)
Transparent Mode R (TMR)	• Transparent transmission and reception using the GSM 08.60 framing. • Automatic 0x0000 flag generation and detection. • Support for 40, 39.5, and 40.5 octet frames. • Error detection (non octet frame content, short frame, long frame)

8.2 Codec

The Thor-2 board contains two codecs implementing two digital phones. The codecs convert two digital Pulse Code Modulated (PCM) channels into analog electrical signals. The analog signals from the codecs can then be connected to standard telephone handsets through connectors #1 and #2 in the Harmonica. The codecs also provide speaker interfaces which are available in the above mentioned connectors.

The Thor-2 codecs support both A-law and u-law for the Analog-to-Digital and Digital-to-Analog conversions. The conversion law to be used can be selected by software. Transmit, receive, and side-tone gains are programmable with software as well. The codecs can also be used to generate DTMF and single tone frequencies. The generated frequencies are again fully programmable.

Codec-0 is permanently connected to time-slot 2 (0 count) on the Aux Highway and Codec-1 is connected to time-slot 3. The time-space switch can be used to cross-connect the codecs into any incoming or outgoing time-slot in the Li and MVIP Highways.

8.3 DTMF Transceiver

The Thor-2 board also contains two Dual Tone Multi Frequency (DTMF) transceivers. The transceivers consist of high performance DTMF receivers and DTMF generators which employ a burst counter to synthesize precise tone bursts and pauses. The DTMF transceivers can also be operated in a call progress mode, where frequencies within the selected pass bands can be detected.

9. Processor Subsystem

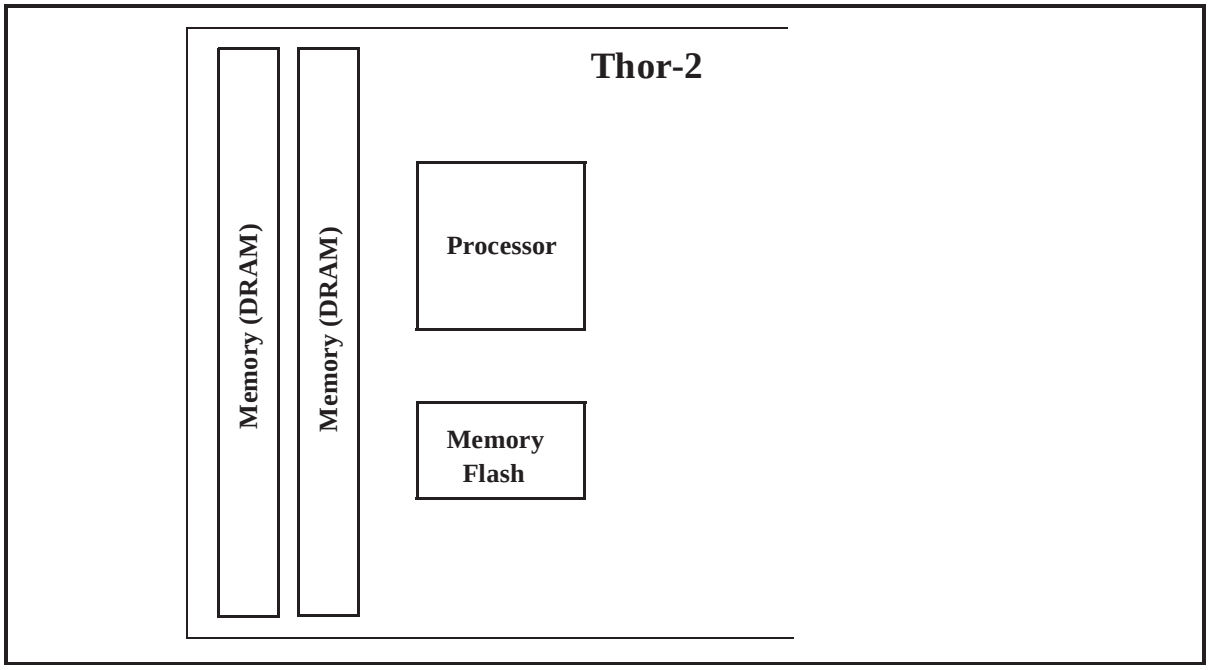

Figure 10. Overview of the Processor Subsystem

The Thor-2 processor subsystem consists of the on-board processor, the on-board Random Access Memory (RAM), the flash memory, and the local buses.

9.1 Processor

The Thor-2 on-board processor (the LPU) is an Intel 386EX. The Intel 386EX microprocessor is a fully static, 32-bit processor optimized for embedded applications. It integrates many commonly used DOS-type peripherals and it has a 32-bit programming architecture compatible with the large software base of Intel386 processors. On the Thor-2 board the 386EX is operated at 16 Mhz.

Besides its processing power, the 386 EX provides several additional resources for Thor-2. The LPU contains an Asynchronous Serial I/O (SIO) unit which implement a Universal Asynchronous Receiver/Transmitter (UART). The LPU implements two full-duplex, asynchronous serial channels (Com-0 and Com-1). The SIO converts serial data characters received from a peripheral device or modem to parallel data and converts parallel data characters received from the LPU to serial data. The serial channels are completely programmable and they are available in connectors #6, #7 and #8 in the Harmonica. The modem control signals are also available for Com-0.

9.2 Memory

The Thor-2 board contains two types of memory: Dynamic Random Access Memory (DRAM) and Flash.

The maximum number of memory that can be addressed on board by the LPU and the CPU is 64 MBytes. The DRAM is located in the beginning of the local memory map (low addresses) and the flash is located at the end of the local memory map (high addresses) as illustrated in Figure 11 on page 25.

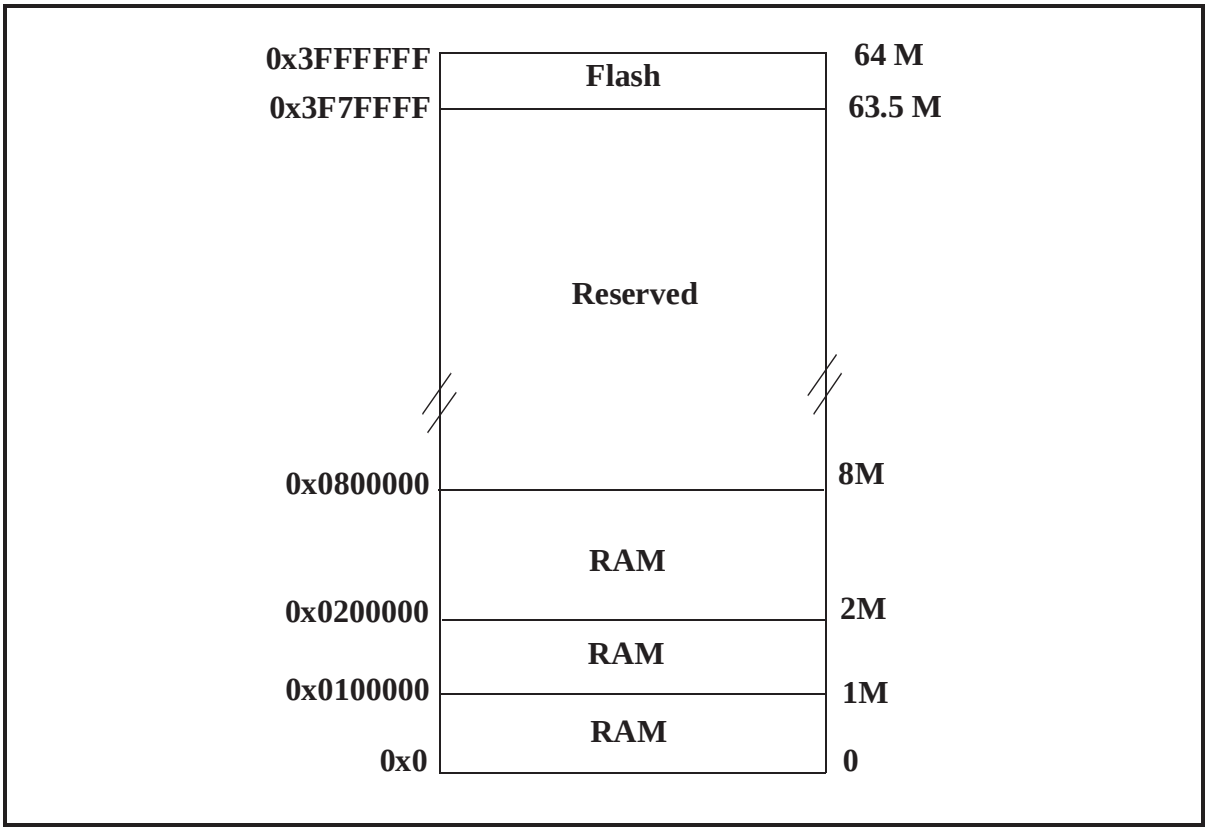

Figure 11. Thor-2 On-Board Memory Map

9.2.1 DRAM Memory

The Thor-2 board utilizes 30-pin DRAM Single Inline Memory Modules (or SIMMs). Thor-2 contains two 30-pin SIMM connectors. Consequently, the board can be equipped with 1 MByte (2 x 512 KByte SIMMs), with 2 MBytes (2 x 1 MByte SIMMs), or with 8 MBytes (2 x 4 MByte SIMMs) of memory. The internal architecture of the Thor-2 board is 16-bits wide, each SIMM containing 8 bits (or one SIMM containing the odd addresses and the other SIMM the even addresses). Please note that both of the SIMMs must be present for the Thor-2 board to operate, and that the SIMMs must be of the same size and speed. The access time of the used memory

should be 70 ns or less. The DRAM is used to store the LPU programs and data as well as receive and transmit buffers for the HDLC controller.

The LPU can execute the Odin TeleSystems proprietary operating system (Monitor) or ROM-DOS^{TM} 6.22 embedded operating system. The DRAM memory mapping is different in those two cases. The memory mapping for Odin LPU Monitor is described in Figure 12 on page 26 and the memory mapping for LPU ROM-DOS is described in Figure 13 on page 27.

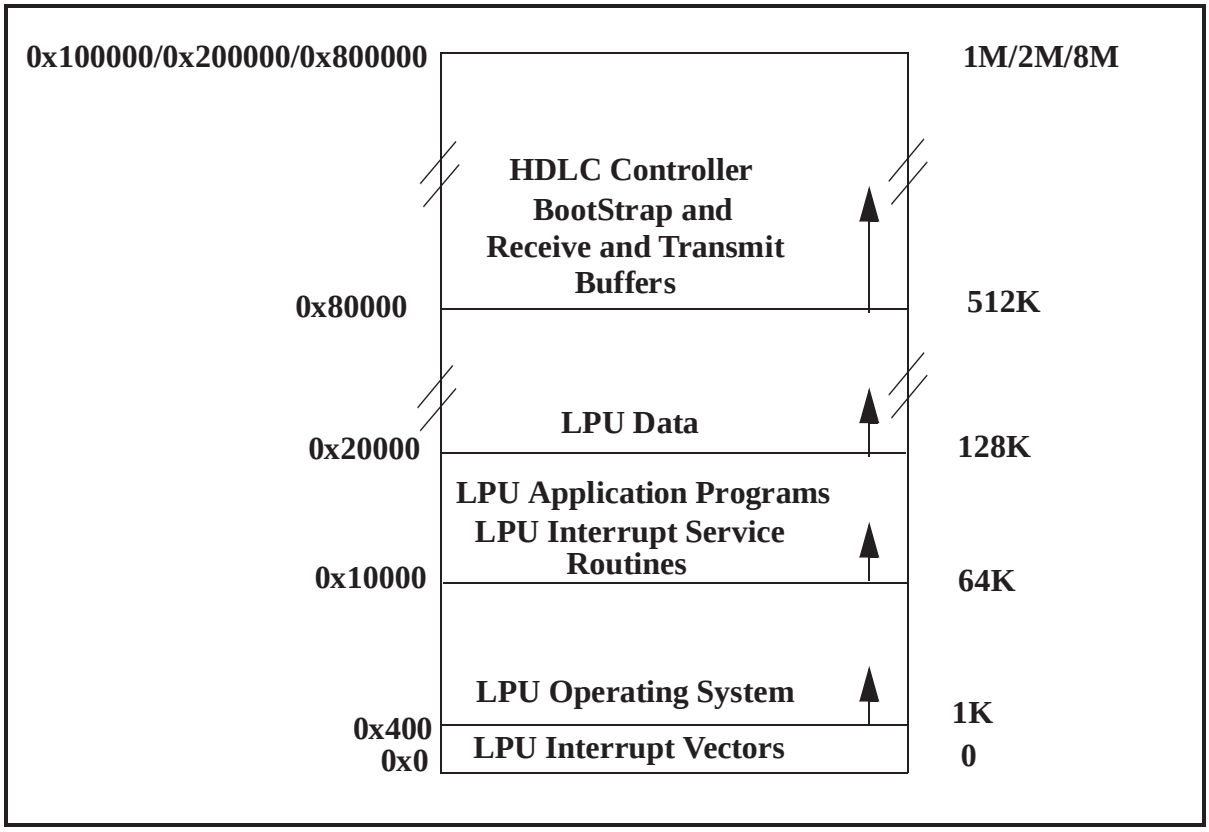

Figure 12. Thor-2 DRAM Memory Map when LPU is running the Odin Proprietary Monitor

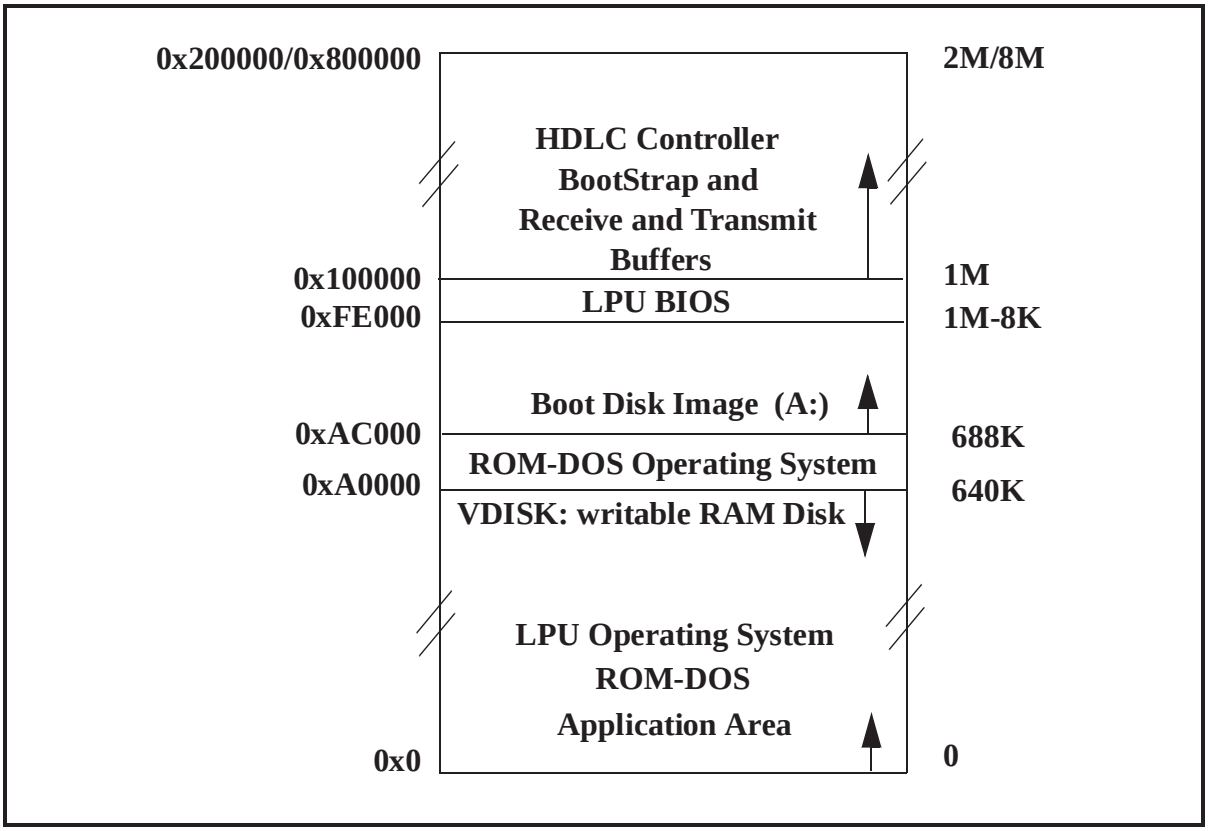

Figure 13. Thor-2 DRAM Memory Map when LPU is running ROM-DOS

9.2.2 Flash Memory

Thor-2 also contains 512 KBytes of flash memory for persistent storage. The Thor-2 flash contains 11 Sectors: seven 64 KByte sectors, one 32 KByte sector, one 16 KByte sectors and two 8 KByte sectors. Any address can be read individually, but a writing to an address requires that the entire sector will be rewritten. The flash can be reprogrammed 100,000 times.

The Thor-2 flash is used to store the LPU Operating System, the LPU boot disk image as well as the Thor-2 configuration and maintenance data. For more information on the persistent Thor-2 configuration data, please refer to the *Thor-2 User Guide*. Nine of the sectors are used by Thor-2 and two are available for general purpose use by the application programs. The sector locations are shown in Figure 14 on page 28.

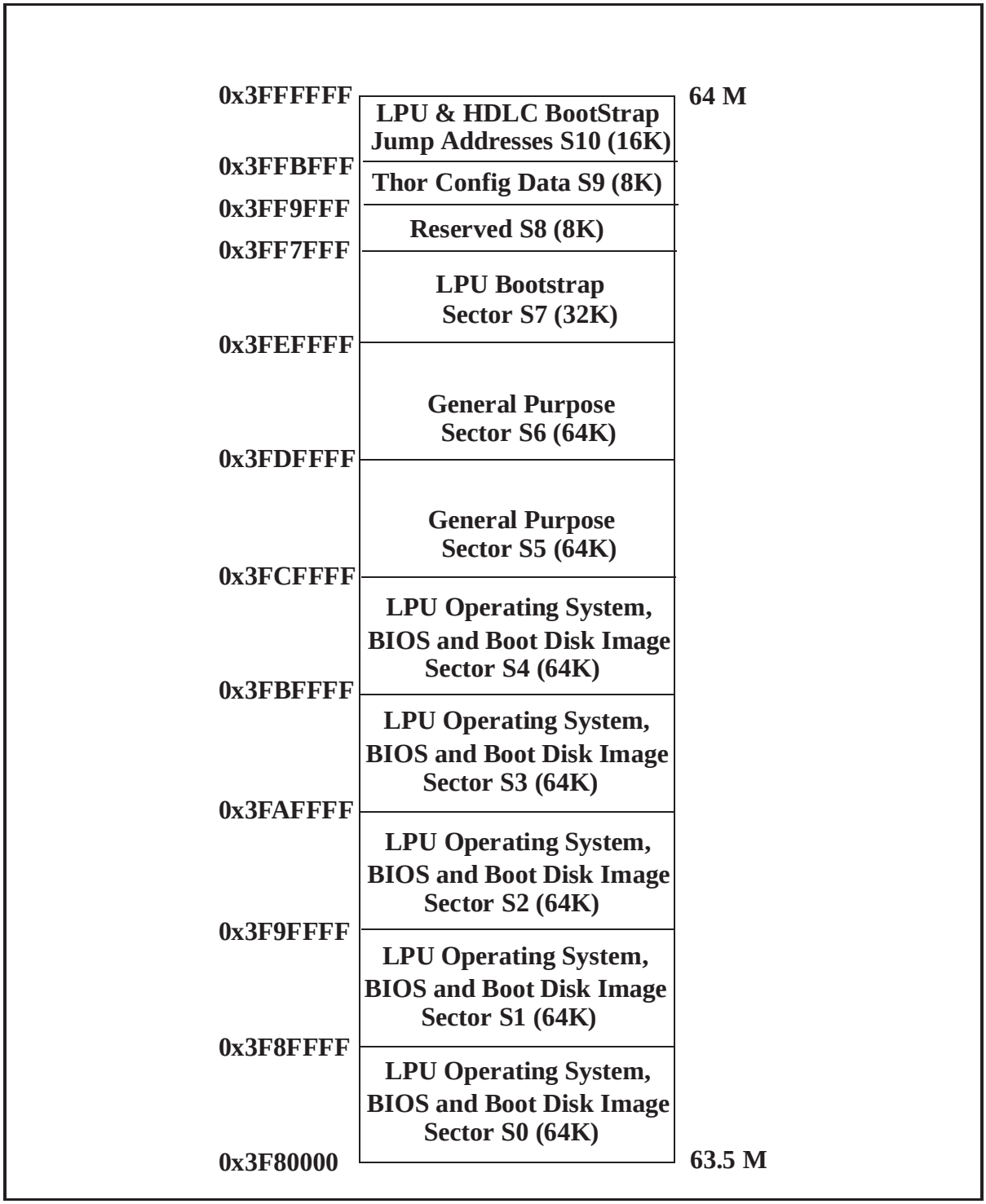

Figure 14. Thor-2 Flash Memory Map

9.3 Control Architecture

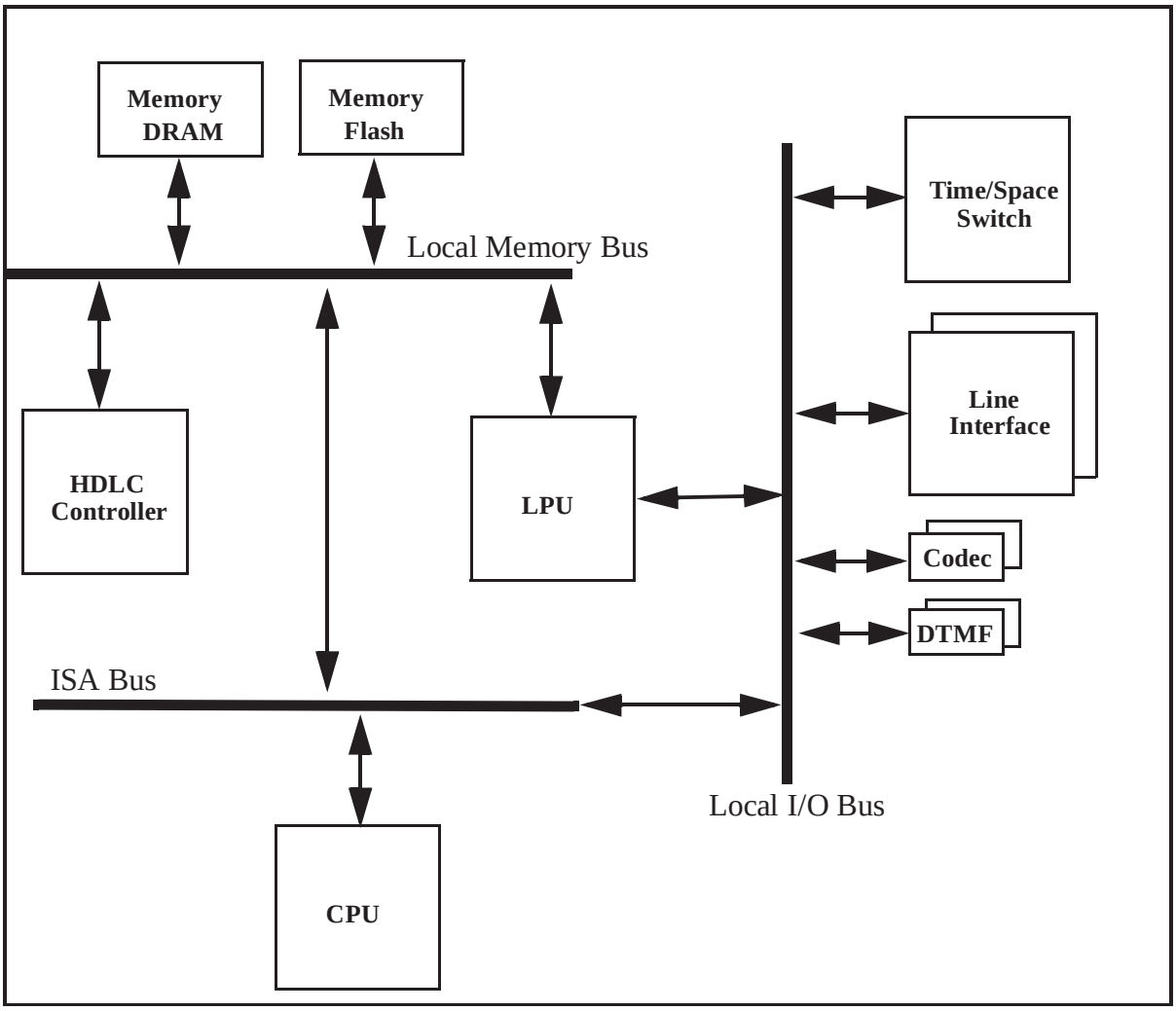

Figure 15. Overview of the Thor-2 Control Architecture

The Thor-2 processor subsystem also contains the control buses. Thor-2 interfaces to the ISA bus and includes two local control buses on-board: The local memory bus and the local I/O bus. The local memory bus is used to access the on-board RAM and flash. The local I/O bus is used to access the I/O-mapped devices: the Line Interfaces, the Time-space Switch, the Codecs, and the DTMF Transceivers. The Thor-2 bus architecture is illustrated in Figure 15 on page 29.

The on-board memory can be accessed by the CPU, the LPU, or the HDLC controller. The devices connected to the Local I/O bus can be controlled by the CPU or by the LPU. The Thor-2 control architecture facilitates parallel processing; For example, the HDLC controller can access the memory over the local memory bus at the same time as the CPU is communicating with a device connected to the Local I/O-bus.

Due to its flexible control architecture, Thor-2 can operate as an active or passive board. The Thor-2 board can be run autonomously under the LPU control without any intervention from the CPU. Or alternatively, the board can be operated under CPU control with the LPU halted.

10. Software Driver Subsystem

The software driver subsystem consists of the LPU boot-up software, LPU Operating System (Odin proprietary monitor or ROM-DOS^{TM}), Thor-2 utility programs, and the driver that allows the host processor to communicate with the board.

The LPU operating system is preloaded into the Flash.

The Thor-2 board is delivered with two utility programs:

- *T2Boot.exe*
  - Loads the configuration data into the Field Programmable Gate Arrays (FPGAs).
  - Boots up the on-board processor for Odin Monitor or ROM-DOS.
  - Loads a new boot disk image into the flash.
  - Performs diagnostics on the board.
- *T2Config.exe* - Stores the T1/E1 configuration parameters persistently in to the flash memory.

For more information on the utility programs *T2Boot.exe* and *T2Config.exe*, please refer to the *Thor-2 User Guide*.

The Thor-2 DOS driver is a C library which can be linked to the C or C++ application. The driver consists of header files containing the macro definitions, type definitions, and function declarations and of the linkable libraries.

The Thor-2 Windows 95 driver is a Virtual Device Driver (VxD) which provides the functionality for Windows 95 applications to talk with the Thor-2 Board.

For more information on the Thor-2 Driver, please refer to the *Thor Application Programming Interface (API) Reference Guide*.

11. Host Control Interface

The Thor-2 communicates with the Host PC over the Industry Standard Architecture (ISA) bus. The Thor-2 board is both memory and I/O mapped, and the CPU can perform both memory and I/O accesses towards Thor-2. Thor-2 communicates towards the CPU by using ISA bus interrupts (IRQs). The memory and I/O mapping of Thor-2 is discussed in detail in the following chapters.

11.1 Memory Mapping

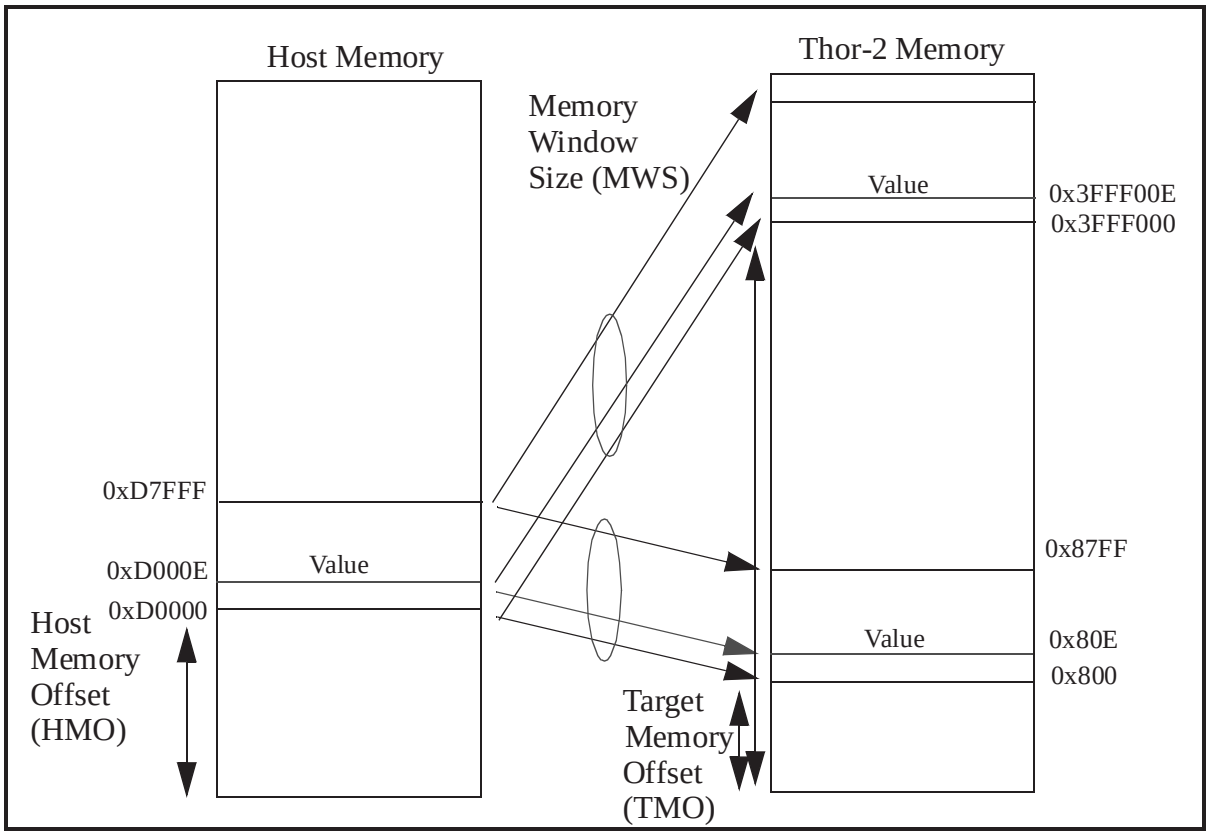

Figure 16. The Sliding Memory Window (See also Figure 17 on page 33)

The on-board memory is accessed by the host via a memory window. An area in the host memory must be reserved for the Thor-2 access. The window within the host memory is mapped on the on-board memory. The mapping can be changed dynamically allowing a small host memory address window to be used to access the whole on-board memory area. The sliding memory window concept is illustrated in Figure 16 on page 32.

The host processor can set up the memory window by writing to three registers on the Thor-2 board. First, the Host Memory Offset (HMO) register is set to point to the

starting address of the memory window. In a DOS application, the memory offset would typically be in the upper memory area between 640K and 1M; for example, 0xD0000. In other operating systems with flat memory model, the host memory offset can be set at any point within the memory.

The size of the memory window is set up in the Memory Window Size (MWS) register. With DOS applications a typical window size is 32 KBytes. The minimum allowed window size is 1 KBytes and the maximum is 16 MBytes.

Lastly, the host must set the Target Memory Offset (TMO) register to map the reserved memory area into the on-board memory. The value in this register sets the lower boundary of the memory window in the on-board memory. An example of the memory mapping is shown in Figure 17 on page 33.

```
Host Memory Offset: 0xD0000 (832k)
Memory Window Size: 0x7FFF (32)K
Thor-2 Memory area in Host Memory: 0xD0000 - 0xD7FFF

Target Memory Offset: 0x800 (2k)

Host memory access to host address: 0xD000E
=> Accesses on-board RAM memory at address: 0x80E

or
Target Memory Offset: 0x3FFF000

Host memory access to host address: 0xD000E
=> Accesses Flash memory at address: 0x3FFF00E
```

Figure 17. Thor-2 Memory Mapping Example

The sliding window addressing scheme can be summarized by the following formula:

```
Target Address = (Host Address - Host Offset) + Target Offset
```

Figure 18. The Address Calculation Formula

The HMO, MWS, and TMO registers used in setting up the memory mapping are discussed in more detail in Chapter 11.2.2: "Direct Access I/O-Registers".

11.2 I/O Mapping

Thor-2 also requires I/O address space. Thor-2 utilizes two types of I/O access: direct and indirect. The direct access I/O registers are mapped directly into the host I/O address space. The indirect access I/O registers are accessed through a sliding I/O window similar to the sliding memory window explained in the previous chapter.

11.2.1 Setting the I/O Base Address for Direct Access I/O Registers

Thor-2 contains 16 registers mapped directly into the host I/O address space. The base address for these registers are set using the Dip Switch SW4 on the Thor-2 board. The I/O-base can be placed at 16 byte boundaries (addressed dividable by 16) within the host I/O address space: 0 - 1K.

Up to 4 Thor-2 boards can be placed in one PC. Each board must have a unique board number which is set using the switches 7 and 8 in SW4 on Thor-2. Table 6 summarizes the switch SW4 settings for the board number.

TABLE 6. SW4 Board number settings

Board #	S7	S8
0	On	On
1	Off	On
2	On	Off
3	Off	Off

Switches 1-6 are used to set the I/O base address for the direct access I/O registers. Switch 1 maps to address 4 in the I/O address, Switch 2 to address 5, and so on. Switch 6 maps to the most significant bit of the I/O-address, bit 9. Table 7 shows some example settings for some commonly used I/O base address settings. Note that dip switch position “On” corresponds to value “0” and position “Off” to value “1”.

TABLE 7. Examples of SW4 I/O base address settings

IO Base Address	S6-S1 value	S1	S2	S3	S4	S5	S6
0220H	22H = 100010B	On	Off	On	On	On	Off
0240H	24H = 100100B	On	On	Off	On	On	Off
0280H	28H = 101000B	On	On	On	Off	On	Off
02A0H	2AH = 101010B	On	Off	On	Off	On	Off
0300H	30H = 110000B	On	On	On	On	Off	Off

TABLE 7. Examples of SW4 I/O base address settings

IO Base Address	S6-S1 value	S1	S2	S3	S4	S5	S6
0320H	32H = 110010B	On	Off	On	On	Off	Off
0340H	34H = 110100B	On	On	Off	On	Off	Off

11.2.2 Direct Access I/O-Registers

The direct access I/O-Registers are summarized in Table 8 on page 35.

TABLE 8. Direct Access I/O-Registers

Address	Register	R/W	Bits	Description
I/O-base	Host Memory Offset (HMO)	W	16	Determine the starting address of the host memory assigned to Thor-2.
I/O-base + 2	Memory Window Size (MWS)	W	16	Sets the size of the memory window in host memory assigned to Thor-2.
I/O-base + 4	Target Memory Offset (TMO)	W	16	Determines the offset in the target memory where the host memory window is mapped.
I/O-base + 6	Host I/O Offset (HIO)	W	8	Set the starting address in the host I/O-base for the I/0 window used to communicate with the devices on the local I/O bus.
I/O-base + 7	I/O Window Size (IWS)	W	8	Sets the size of the I/O-address space window in host assigned for Thor-2 local I/O-bus access.
I/O-base + 8	Target I/O Offset (TIO)	W	8	Determines the offset in the Local I/O-bus where the I/O window is mapped.
I/O-base + 9	CPU Interrupt Mask (CIM)	W	7	Mask for disallowing device interrupts towards the Host
I/O-base + 9	CPU Pending Interrupt (CPI)	R	7	Source of HOST interrupts
I/O-base + 10	LPU Interrupt Mask (LIM)	W	7	Mask for disallowing device interrupts towards the LPU.
I/O-base + 11	IRQ Select/Action Request (ISAR)	W	8	Selects the interrupt used for host: IRQ 3, 4, 5, 7, 10, 11, 12, or 15. Generates action requests towards the Munich.
I/O-base + 12	Reset Request A (RRA)	W	8	Reset up to 8 devices.
I/O-base + 13	Reset Request B (RRB)	W	8	Reset up to 8 devices.
I/O-base + 14	FPGA Load (FL)	W	6	Load the configuration data to two on-board FPGA's.
I/O-base + 14	FPGA Status (FS)	R	2	Allow the reading back of the FPGA status pins' levels.

TABLE 8. Direct Access I/O-Registers

Address	Register	R/W	Bits	Description
I/O-base + 15	Board Control (BC)	W	8	General Purpose register for control outputs.
I/O-base + 15	Board Status (BST)	R	8	General Purpose Register for reading in status inputs.

11.2.2.1 Host Memory Offset (HMO) Register

The HMO Register contains bits [23:8] of the starting address of the host memory reserved for Thor-2. The window can be placed at 256 byte boundaries (Addresses dividable by 2^8=256).

11.2.2.2 Memory Window Size (MWS) Register

The MWS register contains a mask which determines the size of the sliding memory window. The 8 least significant address bits are not masked, so the minimum window size is (2^8=) 256 bytes. For the minimum window size, the register should be set to 0xFFFF. By setting 0's to the least significant bit positions, the size of the window can be increased, each bit increasing the window size two-fold. E.g., value 0xFFFC in the MWS register yields a window size of (2^2=) 4 x 256 = 1024 bytes and value 0xFFF0 a window size (2^4=) 16 x 256 = 4096 bytes. The maximum window size (register value 0x0000) is (2^{16}=) 65536 x 256 = 16 MBytes.

Since the minimum resolution of the target offset (TMO register) is 1024 bytes, the minimum practical window size is 1024 bytes (1 KByte) as well (MWS register value 0xFFFC). A smaller than 1 KByte sliding window can be used, but in that case some of the on-board memory will not be accessible by the host.

11.2.2.3 Target Memory Offset (TMO) Register

The TMO register contains bits [25:10] of the offset to the local memory bus. The value of the TMO register is added to the address within the sliding address window (host address - host offset) to determine the actual on-board address of the Memory location being accessed. The resolution of the target offset is 1024 bytes (1 KByte).

11.2.2.4 Host I/O Offset (HIO) Register

The HIO Register contains bits [9:2] of the starting address of the host I/O-address space reserved for Thor-2. The window can be placed at even addresses at 4 byte intervals (2^2 bits). The I/O address window must be placed within the first 1 kilobyte of the I/O-address space.

11.2.2.5 I/O Window Size (IWS) Register

The IWS register contains a mask which determines the size of the sliding I/O address window. The two least significant address bits are not masked, so the minimum window size is (2^2=) 4 bytes. For the minimum window size, the register should be set to 0xFF. By setting 0's to the least significant bit positions, the size of the window can be increased, each bit increasing the window size two-fold.. E.g. Value 0xFE in the IWS register yields a window size of (2^1=) 2 x 4 = 8 bytes and value 0xF0 a window size (2^4=) 16 x 4 = 64 bytes. The maximum window size (register value 0x00) is (2^8=) 256 x 4 = 1 KByte.

11.2.2.6 Target I/O Offset (TIO) Register

The TIO register contains bits [9:2] of the offset to the local memory bus. The value of the TIO register is added to the address within the sliding address window (host address - host offset) to determine the actual on-board address of the I/O-register being accessed. The resolution of the target offset is 4 bytes.

11.2.2.7 CPU Interrupt Mask (CIM) Register

The CIM register can be used to mask interrupts from the Thor-2 devices. Clearing the register masks all the device interrupts and setting the register enables them. The bits in the CIM register are described in Table 9 on page 37 .

TABLE 9. CIM Bit Description

Bit	Function
0	0: Mask Interrupts from the HDLC Controller 1: Allow Interrupts
1	0: Mask Interrupts from Li0 1: Allow Interrupts
2	0: Mask Interrupts from Li1 1: Allow Interrupts
3	0: Mask Interrupts from the Time-Space Switch 1: Allow Interrupts
4	0: Mask Interrupts from DTMF Transceiver 0 1: Allow Interrupts
5	0: Mask Interrupts from DTMF Transceiver 1 1: Allow Interrupts
6	0: Mask Interrupts from the LPU 1: Allow Interrupts

11.2.2.8 CPU Pending Interrupt (CPI) Register

The CPI register contains information on pending interrupts towards the CPU. The CPI register bits are described in Table 15 on page 40.

TABLE 10. CPI Bit Description

Bit	Function
0	1: Interrupt pending from the HDLC Controller 0: No interrupt pending
1	1: Interrupt pending from Li0 0: No interrupt pending
2	1: Interrupt pending from Li1 0: No interrupt pending
3	1: Interrupt pending from the Time-Space Switch 0: No interrupt pending
4	1: Interrupt pending from DTMF Transceiver 0 0: No interrupt pending
5	1: Interrupt pending from DTMF Transceiver 1 0: No interrupt pending
6	1: Interrupt pending from the LPU 0: No interrupt pending

11.2.2.9 LPU Interrupt Mask (LIM) Register

The LIM register can be used to mask interrupts from the Thor-2 devices towards the LPU. Clearing the register masks all the device interrupts and setting the register enables them. The bits in the LIM register are described in Table 11 on page 38.

TABLE 11. LIM Bit Description

Bit	Function
0	0: Mask Interrupts from the CPU 1: Allow Interrupts
1	0: Mask Interrupts from the HDLC Controller 1: Allow Interrupts
2	0: Mask Interrupts from Li0 1: Allow Interrupts
3	0: Mask Interrupts from Li1 1: Allow Interrupts
4	0: Mask Interrupts from the Time-Space Switch 1: Allow Interrupts

TABLE 11. LIM Bit Description

Bit	Function
5	0: Mask Interrupts from DTMF Transceiver 0 1: Allow Interrupts
6	0: Mask Interrupts from DTMF Transceiver 1 1: Allow Interrupts

11.2.2.10 IRQ Select/Action Request (ISAR) Register

The ISAR Register is used to select the ISA bus IRQ used by the Thor-2 (See Table 13). It can also be used by the CPU to interrupt the LPU, send action request to the HDLC Controller, disable all the interrupts, perform self-test on the LPU, and float the LPU.

TABLE 12. ISAR Bit Description

Bit	Function
0	ISA IRQ Address 0
1	ISA IRQ Address 1
2	ISA IRQ Address 2
3	1: Generate Interrupt towards the LPU 0: No action
4	1: Generate Action Request towards the HDLC Controller. 0: No action
5	1: Disable all the interrupts towards the CPU 0: No action
6	1: Perform self-test on the LPU 0: No action
7	1: Disconnect (Float) the LPU from the local buses 0: No action

TABLE 13. ISAR[2:0] - to ISA IRQ Mapping

ISAR2	ISAR1	ISAR0	IRQ
0	0	0	IRQ3
0	0	1	IRQ4
0	1	0	IRQ5
0	1	1	IRQ7
1	0	0	IRQ10

TABLE 13. ISAR[2:0] - to ISA IRQ Mapping

ISAR2	ISAR1	ISAR0	IRQ
1	0	1	IRQ11
1	1	0	IRQ12
1	1	1	IRQ15

11.2.2.11 Reset Request A (RRA) Register

By writing ‘1’s to this register, the host can reset the devices listed in Table 14 on page 40. It should be noted that the Reset input for the devices will be kept asserted as long as the register holds a ‘1’ at the corresponding bit position. To resume normal operation of a device, a ‘0’ must be placed in to the Reset Request Register.

TABLE 14. RRA bit description

Bit	Function
0	Reset the LPU
1	Reset Li0
2	Reset Li1
3	Reset the Time-Space Switch
4	Reset HDLC Controller
5	Reset Codec-0
6	Reset Codec-1
7	Reset the Flash Memory

11.2.2.12 Board Status (BST) Register

The BST register can be used to read the status of various Codec and LPU watchdogs and LPU general purpose I/O-pins.

TABLE 15. BST Bit Description

Bit	Function
0	Codec-0 Watchdog
1	Codec-1 Watchdog
2	LPU Watchdog
3	LPU, General purpose pin P1#2
4	LPU, General purpose pin P1#3
5	LPU, General purpose pin P1#4

TABLE 15. BST Bit Description

Bit	Function
6	Reserved
7	Reserved

11.2.2.13 Other Registers

The Reset Request B (RRB) Register, the FPGA Load (FL) Register, the FPGA Status (FS) Register, and the Board Control (BC) Register are reserved for Odin internal use. These registers are not available to the application developer.

11.2.3 Indirect Access I/O-Registers

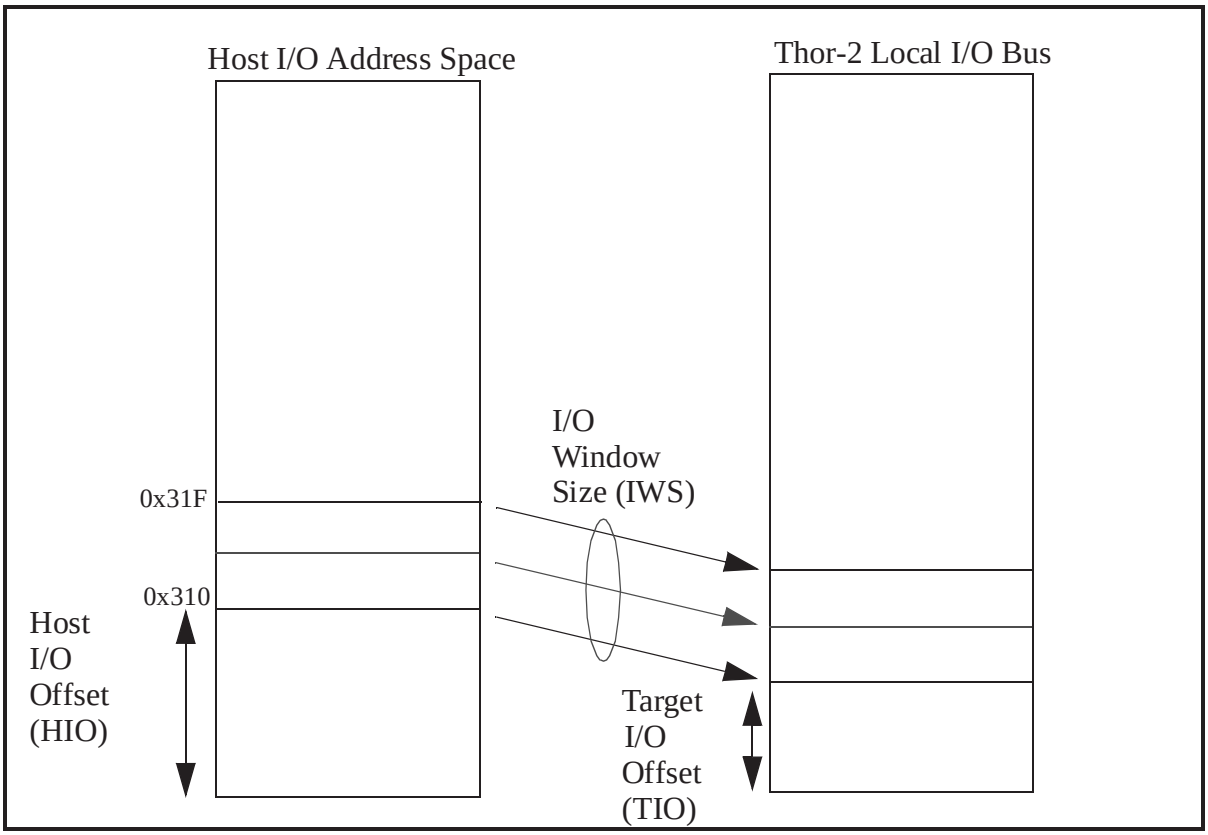

Figure 19. The Sliding I/O Window.

In addition to the 16 direct access I/O registers, the Thor-2 devices on the local I/O-bus contain a large number of I/O-registers. These registers are accessed through a sliding I/O-window. The I/O sliding window is illustrated in Figure 19 on page 41. The sliding I/O window operates based on the same principle as the sliding memory

window. For explanation on the concept, please refer to Chapter 11.1: "Memory Mapping".

11.2.3.1 Local I/O Bus Address Mapping

The I/O-devices in the local I/O-bus are mapped to the address space according to Table 16 on page 42.

TABLE 16. Mapping of I/O-devices on the local I/O bus

Device	Device Address Range	Offset	Local I/O Bus Address Range	R/W	Data Bits	Description
Li-0	0-127	0x100	0x100-0x17F	R/W	8	Line Interface #0 Registers
Li-1	0-127	0x180	0x180-0x1FF	R/W	8	Line Interface #1 Registers
TSS	0-3	0x200	0x200-0x203	R/W	8	Time-Space Switch Registers
DTMF-0	0-1	0x204	0x204-0x205	R/W	4	DTMF Transceiver #0 Registers
DTMF-1	0-1	0x208	0x208-0x209	R/W	4	DTMF Transceiver #1 Registers
Codec-0	0	0x20D	0x20C	R/W	3	Codec #0 Serial Data Interface
Codec-1	0	0x210	0x210	R/W	3	Codec #1 Serial Data Interface

11.3 Host Interrupt

The Thor-2 board communicates towards the host PC via an Interrupt. The used IRQ line can be selected with software from the following set: IRQ3, IRQ4, IRQ5, IRQ7, IRQ10,. IRQ11, IRQ12, and IRQ15. The used IRQ is selected by writing to the ISAR Register (See Table 13 on page 39). If several Thor-2 boards are installed in one PC, they can share the same IRQ line.

12. Thor-2 Specifications

PC Bus Interface:	Industry Standard Architecture (ISA)
Physical Dimensions:	4.5” x 13.3” x 0.062” Inches
Power Requirements:	+5 V (DC) +- 5%, 2.5 A
Operating Temperature:	0 ^{o} C - 35 ^{o}C

13. Standards Compliance

Thor-2 complies to the following standards:

13.1 Interfaces

ITU-T I.431 1544 kbit/s (T1) and 2048 kbit/s (E1)

13.2 E1 Interface

ITU-T G.703

ITU-T G.704

13.3 Jitter

ITU-T I.431

ITU-T G.703

AT&T TR 62411

13.4 Loss of Signal Indication

ITU-T G.775

ANSI T1.403

13.5 Error Checking

ITU-T G.706

13.6 Codecs

ITU-T G.711

ITU-T G.714

13.7 MVIP

MVIP-90 Standard, Release 1.1

Doc. No. 1111-1-HAA-1004-1
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