OctalFALC™

Octal E1/T1/J1 Framer and Line Interface Component for Long- and Short-Haul Applications

PEF 22558 E, Version 1.1

Wireline Communications

Never stop thinking.

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PEF 22558 E, Octal E1/T1/J1 Framer and Line Interface Component for Long- and Short-Haul Applications

Revision History: 2005-04-12, Rev. 2.0

Previous Version:

Page	Subjects (major changes since last revision)
24	Pin RES has no internal pull up resistor
53	Pin MCLK has an internal pull up resistor
25	Pin IM1 has an internal pull down resistor
58	Pins XDI(1:8) have internal pull up resisitors
337, 548	Reset values of registers TXP(1:8) are 38hex, see TXP1_E or TXP1_T
111, 112	Recommended pulse shaper programming values changed, see Table 25 and Table 26
84	Acknowledge frame structure of the SCI interface, description reworked, see Figure 10
165	Bit robbing idle functionality in F72 mode together with serial CAS, see Chapter 5.3.3
97	Receiver sensitivity in E1 mode, see Chapter 3.6.1, Chapter 3.6.2 and Chapter 13.3
RFIFO2L_E	Receive FIFO registers RFIFO(1:3)(H,L) have reset values ´xx_H´, see RFIFO2L_E for example
CMR6_E, CMR6_T	Ordering of TCLK frequencies and register bits CMR6.STF changed
654	FSC timing parameter values, see Figure 119

Trademarks

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

List of Figures

List of Figures

List of Figures

List of Tables

List of Tables

List of Tables

List of Tables

Preface

The OctalFALC™ is an 8 channel E1/T1/J1 Framer And Line interface Component, it is designed to fulfill all required interfacing between 8 analog E1/T1/J1 lines and the digital PCM system highway/H.100 bus.

The digital functions as well as the analog characteristics can be configured either via a flexible microprocessor interface, SPI interface or via an SCI interface.

To enable a seamless transition from QuadFALC® designs to OctalFALC™ applications, a compatibility mode is provided. This mode allows software written for the QuadFALC® to be used with the OctalFALC™ without changes.

The device is delivered inRoHS compliant package PG-LBGA-256 and in non-RoHS compliant package P-LBGA-256.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1**, “Introduction”: Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- **Chapter 2**, “Pin Descriptions”: Lists pin locations with associated signals, categorizes signals according to function, and describe signals.
- **Chapter 3** to **Chapter 5**, “Functional Description”: These chapters describe the functional blocks and principal operation modes, organized into separate sections for E1 and T1/J1 operation
- **Chapter 6** and **Chapter 8**, “E1 Registers” and “T1/J1 Registers”: Gives a detailed description of all implemented registers and how to use them in different applications/configurations.
- **Chapter 9**, “Package Outlines”: Shows the mechanical values of the device packages.
- **Chapter 10**, “Electrical Characteristics”: Specifies maximum ratings, DC and AC characteristics.
- **Chapter 11**,“Operational Description”: Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).
- **Chapter 12**, “Signalling Controller ...”: Describes signaling controller functions for both E1 and T1/J1 operation.
- **Chapter 13**, “Appendix”: Gives an example for over voltage protection and information about application notes and other support.
- **Terminology**: Declares abbreviations used in this document.

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656
ANSI T1.102
ANSI T1.403
AT&T PUB 43802
AT&T PUB 54016
AT&T PUB 62411
ESD Ass. Standard EOS/ESD-5.1-1993
ETSI ETS 300 011
ETIS ETS 300 166
ETSI ETS 300 233
ETSI ETS 300 324
ETSI ETS 300 347
ETSI TBR12
ETSI TBR13
FCC Part68
GR-253-CORE
GR-499-CORE
GR-1089-CORE
H.100
H-MVIP
IEEE 1149.1
ITU-T G.703
ITU-T G.704
ITU-T G.705
ITU-T G.706
ITU-T G.732
ITU-T G.735
ITU-T G.736
ITU-T G.737
ITU-T G.738
ITU-T G.739
ITU.T G.733
ITU-T G.823
ITU-T G.824
ITU-T G.962
ITU-T G.963
ITU-T G.964
ITU-T I.431
ITU-Q.703
JT-G703
JT-G704
JT-G706
JT-G33
JT-I431
MIL-Std. 883D
TR-TSY-000009
UL 1459

1 Introduction

The OctalFALC™ is the latest adition to Infineon's FALC® family of sophisticated E1/T1/J1 Framer And Line interface Components. This monolithic 8 channel device is designed to fulfill all required interfacing between eight analog E1/T1/J1 lines and the digital PCM system highway, H.100/H.110 or H-MVIP bus. Designed to support both long haul and short haul applications, the OctalFALC™ provides support for all standard E1/T1/J1 functions. It includes 3 HDLC controllers per channel which makes particularly suitable for supporting V5.1/V5.2 systems. Support of Signalling System #7 is also included.

The device is supplied in a 17 mm x 17 mm LBGA package, and is designed to minimize the number of external components required, so reducing system costs and board space. RoHS compliant (PG-LBGA-256) and non-RoHS compliant (P-LBGA-256) package versions are available

The OctalFALC™ also includes an integrated analog switch for each channel to allow either 75 Ω operation or 1.1 protection switching to be supported. It operates with a single master clock source and features crystal-less jitter attenuation .

Equipped with a flexible microprocessor interface, a SCI and a SPI interface, it connects to any control processor environment. A standard boundary scan interface is provided to support board level testing. BGA device packaging, minimum number of external components and low power consumption lead to reduced overall system costs.

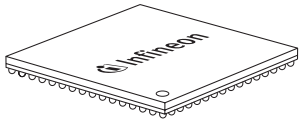
Other members of the FALC® family are the FALC® single channel Framer And Line interface Component and the QuadFALC® four channel Framer and LIU component.

Octal E1/T1/J1 Framer and Line Interface Component for Long- and Short-Haul Applications OctalFALC™

PEF 22558 E

Version 1.1

1.1 Features



P/PG-LBGA-256-1, -2

Line Interface

- High-density, generic interface for all E1/T1/J1 applications
- Eight Analog receive and transmit circuits for long-haul and short-haul applications
- E1 or T1/J1 mode selectable
- Data and clock recovery using an integrated digital phase-locked loop
- Clock generator for jitter-free system/transmit clocks per channel
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) and PUB 62411 are met
- Maximum line attenuation up to -43 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Flexible programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable line build-out for CSU signals according to ANSI T1. 403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22.5 dB (T1/J1)
- Programmable low transmitter output impedances for high transmit return loss and generic E1/T1/J1 applications
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Flexible tristate functions of the digital receive outputs
- Receive line monitor mode
- Integrated analog switch for generic E1/T1/J1 applications to meet termination resistance 75/120Ω for E1, 100Ω for T1 and 110Ω for J1
- Crystal-less wander and jitter attenuation/compensation according to TR 62411, ETS-TBR 12/13, PUB 62411
- Common master clock reference for E1 and T1/J1 with any frequency within 1.02 and 20 MHz
- Power-down function
- Support of automatic protection switching
- Dual-rail or single-rail digital inputs and outputs
- Unipolar NRZ or CMI for interfacing fiber-optical transmission routes
- Selectable line codes (E1: HDB3, AMI/T1: B8ZS, AMI with ZCS)
- Loss-of-signal indication with programmable thresholds according to ITU-T G.775, ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Optional data stream muting upon LOS detection
- Programmable receive slicer threshold
- Local loop, payload loop and remote loop for diagnostic purposes. Automatic payload loop and remote loop switching is possible with In-Band and Out-Band loop codes
- Per channel power-down function

Type	Package
PEF 22558 E	PG-LBGA-256
PEF 22558 E	P-LBGA-256

- Low power device, two power supply voltages: 1.8 V and 3.3 V

Frame Aligner

- Frame alignment/synthesis for 2048 kbit/s according to ITU-T G.704 (E1) and for 1544 kbit/s according to ITU-T G.704 and JT G.704 (T1/J1)
- Programmable frame formats:
  E1: Doubleframe, CRC multiframe (E1)
  T1: 4-frame multiframe (F4,FT), 12-frame multiframe (F12, D3/4), extended superframe (F24, ESF), remote switch mode (F72, SLC96)
- Selectable conditions for recover/loss of frame alignment
- CRC4 to non-CRC4 interworking according to ITU-T G. 706 Annex B (E1)
- Error checking via CRC4 procedures according to ITU-T G. 706 (E1)
- Error checking via CRC6 procedures according to ITU-T G. 706 and JT G.706 (T1/J1)
- Performs synchronization in ESF format according to NTT requirements (J1)
- Alarm and performance monitoring per second 16-bit counter for CRC-errors, framing errors, code violations, error monitoring via E-bit and SA6-bit (E1), errored blocks, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS, remote/yellow alarm,…)
- Remote alarm generation/checking according to ITU JT-G.704 in ESF-format (J1)
- Remote defect indication according to ITU-T G.775
- IDLE code insertion for selectable channels
- Single-bit defect insertion
- Flexible system clock frequency for receiver and transmitter
- Supports programmable system data rates with independent receive/transmit shifts:
  E1: 2.048, 4.096, 8.192 and 16.384 Mbit/s (according to H.100/H.110 bus)
  T1/J1: 2.048, 4.096, 8.192, 16.384 Mbit/s and 1.544, 3.088, 6.176, 12.352 Mbit/s
  with integrated multiplexer and de-multiplexer
- Elastic store for receive and transmit clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Provides different time slot mapping modes
- Supports fractional E1 or T1/J1 access
- Flexible transparent modes
- Programmable In-band loop code detection and generation (TR62411)
- Programmable Out-band loop code (BOM) detection (ANST-T1 403))
- Channel loop back, line loop back or payload loop back capabilities (TR54016)
- Flexible pseudo-random binary sequence generator and monitor
- Clear channel capabilities (T1/J1)
- Loop-timed mode

Signaling Controller

- Three HDLC controllers per channel, attachable either to the line or system side, including 128 byte FIFO buffers, perform Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions
- Supports signaling system #7 delimitation, alignment and error detection according to ITU-Q.703 processing of fill in signaling units, processing of errored signaling units
- ANSI T1.404 bit-oriented messages (BOM) generates periodical performance reports
- CAS/CAS-BR controller with last look capability, enhanced CAS-register or system interface access and freeze signaling indication
- DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016 (T1/J1)
- Flexible DL-bit access for F72 (SLC96) format (T1/J1)
- Generates periodical performance report according to ANSI T1. 403, accessible by microcontroller
- Provides access to serial signaling data streams
- Multiframe synchronization and synthesis according to ITU-T G.732
- Alarm insertion and detection (AIS and LOS in time slot 16)

- Transparent mode
- Scalable FIFO buffers (up to 128 bytes deep) for efficient transfer of data packets
- Time slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode (useful for fractional T1/J1 applications)
- Time-slot 0 Sa8...4-bit handling via FIFOs (E1)
- HDLC access to any Sa-bit combination (E1)

Microprocessor Interface

- Asynchronous 8/16-bit microcontroller bus interface (Intel or Motorola type selectable)
- SPI bus interface
- SCI bus interface
- All registers directly accessible
- Multiplexed and non-multiplexed address bus operations on asynchronous 8/16-bit microprocessor bus interface
- Hard/software reset options
- Extended interrupt capabilities
- One-second timer (internal or external timing reference)

General

- ® compatibility mode enables using of ® programming without changes
- Boundary scan standard IEEE 1149.1
- P-LBGA-256 package; body size 17 mm × 17 mm; ball pitch 1.0 mm or
- Temperature range from -40 to +85 °C
- 1.8 V and 3.3 V power supply
- Typical power consumption 150 mW per channel

Applications

- Wireless basestations
- E1/T1/J1 ATM gateways, multiplexer
- E1/T1/J1 **C**hannel & **D**ata **S**ervice **U**nits (CSU, DSU)
- E1/T1/J1 Internet access equipment
- LAN/WAN router
- ISDN PRI, PABX
- **D**igital **A**ccess **C**rossconnect **S**ystems (DACS)
- SONET/SDH add/drop multiplexer

1.2 Logic Symbol

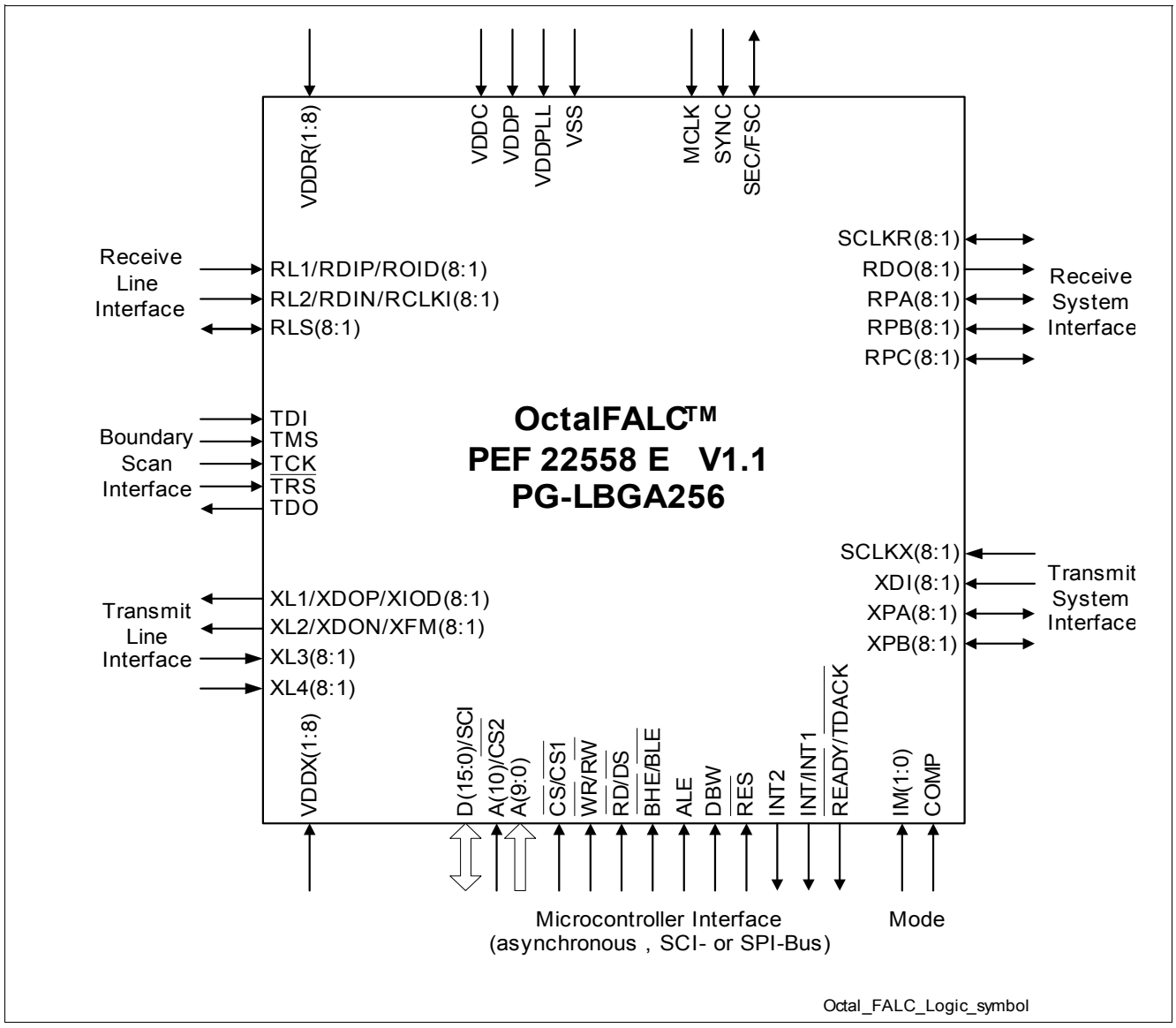


Figure 1 Logic Symbol

1.3 Typical Applications

The figures show a multiple link application for Frame Relay applications using the OctalFALC™ together with the 256-channel HDLC controller MUNICH256 as well as an 8-channel interface to the ATM layer via the IWE8 interworking device..

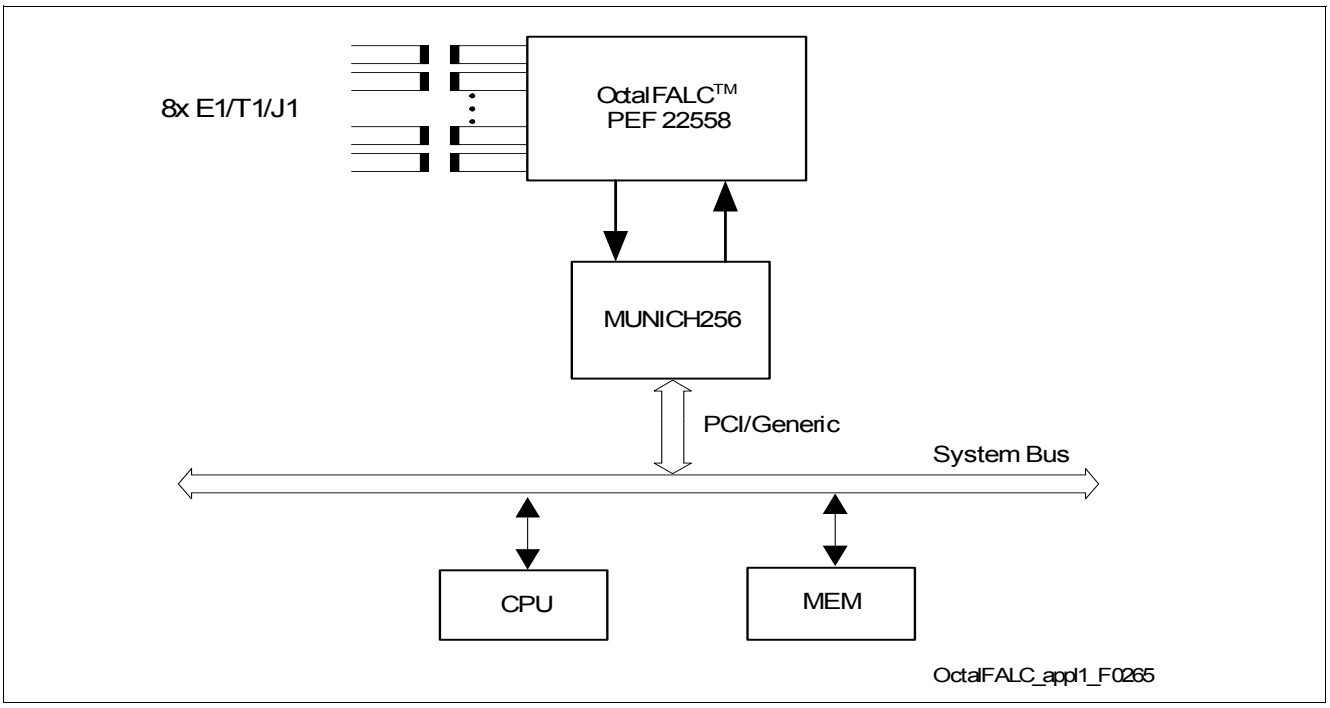


Figure 2 Multiple E1/T1/J1 Link over Frame Relay

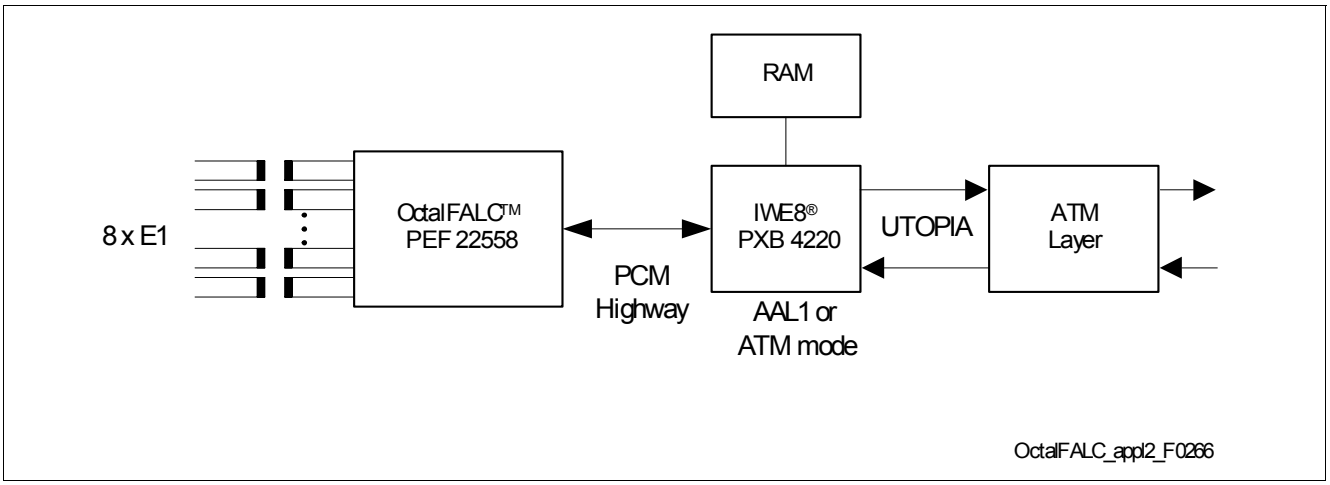


Figure 3 8-Channel E1/T1/J1-Interface to the ATM Layer

2 Pin Descriptions

In this chapter the function and placement of all pins are described.

2.1 Pin Diagram PG-LBGA-256 (top view)

Figure 4 shows the ball layout of the OctalFALC™

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
16	Reserved	XPB8	XPA8	SCLKX8	SCLKR8	RPA7	A0	RD	A3	A9	SCLKX6	SCLKR6	RPC5	SCLKR5	RPA5	Reserved
15	RL27	VSS	XDI8	RPB8	XPB7	RDO7	ALE	WR	A4	A8	RPC6	XPB5	RPB5	RDO5	VSS	RL26
14	RLS27	VSS	XL37	XL17	XPA7	RPB7	READY	INT2	A2	A7	XDI6	XPA5	XL16	XL36	VSS	RLS26
13	RL17	VDDR7	XL47	XL27	RDO8	SCLKR7	SYNC	BHE	A1	A6	RPB6	RPA6	XL26	XL46	VSS	RL16
12	VSS	VSS	VDDX7	VDDX7	RPA8	SCLKX7	SEC	CS	A5	A10	XPA6	SCLKX5	VDDX6	VDDX6	VDDR6	VSS
11	RL18	VDDR8	VSS	XL38	XL18	RPC8	VDDC	INT	VDDP	VDDP	XPB6	XDI5	XL15	XL35	VDDR5	RL15
10	RL28	RLS28	VSS	XL48	XL28	RPC7	VSS	VSS	VSS	VSS	VDDC	RDO6	XL25	XL45	TDO	RLS25
9	VSS	VSS	VDDX8	VDDX8	RPC2	XDI7	VSS	VSS	VSS	VSS	VDDC	TDI	VDDX5	VDDX5	TCK	RL25
8	RL21	COMP	VDDX1	VDDX1	RPB2	SCLKX2	VSS	VSS	VSS	VSS	VDDC	TMS	VDDX4	VDDX4	VSS	VSS
7	RLS21	VDDR1	XL31	XL11	RPC1	XDI2	VSS	VSS	VSS	VSS	XPA3	XL14	XL34	VSS	RLS24	RL24
6	RL11	IM1	XL41	XL21	RPA2	XPB2	VSS	VDDPLL	MCLK	VSS	RDO3	XL24	XL44	TRSQ	VDDR4	RL14
5	VSS	VDDR2	VDDX2	VDDX2	XDI1	XPA2	VDDP	VDDP	VDDP	VDDP	XDI3	RPB4	VDDX3	VDDX3	DBW	VSS
4	RL12	IM0	XL32	XL12	RDO2	D12	VDDC	VDDC	VDDC	SCLKR3	RPA3	RPA4	XL13	XL33	VDDR3	RL13
3	RLS22	RES	XL42	XL22	XPA1	D13	D9	D5	D3	D2	SCLKX3	RDO4	XL23	XL43	VSS	RLS23
2	RL22	VSS	RDO1	RPB1	XPB1	D14	D10	D7	D4	D0	RPB3	XPB3	RPC4	XDI4	VSS	RL23
1	Reserved	RPA1	SCLKR1	SCLKX1	SCLKR2	D15	D11	D8	D6	D1	RPC3	SCLKR4	SCLKX4	XPA4	XPB4	Reserved

Figure 4 Pin Configuration (Ball Layout) PG-LBGA-256

2.2 Pin Definitions and Functions

The following table describes all pins and their functions:

Table 1 I/O Signals

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
Operation Mode Selection and Device Initialization					
	B3	$\overline{\text{RES}}$	I	–	**Hardware Reset** Active low

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	B6	IM1	I	PD	**Interface Mode Selection** $'00_B'$: Asynchronous Intel Bus Mode. $'01_B'$: Asynchronous Motorola Bus Mode $'10_B'$: SPI Bus Slave Mode. $'11_B'$: SCI Bus Slave Mode
	B4	IM0	I	PU	
	B8	COMP	I	PU	**Software Compatibility Mode Selectt** 1_B **QuadFALC® Mode** ("Compatibility Mode") is selected: OctalFALC™ can be used as it consists on two separate "pseudo" QuadFALCs. 0_B **OctalFALC™ Generic Mode**
Asynchronous and Serial Microcontroller Interfaces					
	K12	A10	I	PU	**Address Bus Line 10** MSB of address if COMP = $'0_B'$ and if micro controller mode (Intel, Motorola) is selected
		CS2	I	PU	**Chip Select 2** Low active chip select for second "pseudo" QuadFALC® if COMP = '1' and if micro controller mode (Intel, Motorola) is selected.
	K16	A9	I	PU	**Address Bus Line 9**
	K15	A8	I	PU	**Address Bus Line 8**
	K14	A7	I	PU	**Address Bus Line 7**
	K13	A6	I	PU	**Address Bus Line 6**
	J12	A5	I	PU	**Address Bus Line 5**
		A5	I	PU	**SCI source address bit 5 (MSB)** Only used if SCI interface mode is selected by IM(1:0) = '11b'.
	J15	A4	I	PU	**Address Bus Line 4**
		A4	I	PU	**SCI source address bit 4** Only used if SCI interface mode is selected by IM(1:0) = '11b'.
	J16	A3	I	PU	**Address Bus Line 3**
		A3	I	PU	**SCI source address bit 3** Only used if SCI interface mode is selected by IM(1:0) = '11b'.
	J14	A2	I	PU	**Address Bus Line 2**
		A2	I	PU	**SCI source address bit 2** Only used if SCI interface mode is selected by IM(1:0) = '11b'.
	J13	A1	I	PU	**Address Bus Line 1**
		A1	I	PU	**SCI source address bit 1** Only used if SCI interface mode is selected by IM(1:0) = '11b'.
	G16	A0	I	PU	**Address Bus Line 0**
		A0	I	PU	**SCI source address bit 0 (LSB)** Only used if SCI interface mode is selected by IM(1:0) = '11b'.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	F1	D15	IO	PU	**Data Bus Line 15**
		PLL10	I	PU	**PLL programming bit 10** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	F2	D14	IO	PU	**Data Bus Line 14**
		PLL9	I	PU	**PLL programming bit 9** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	F3	D13	IO	PU	**Data Bus Line 13**
		PLL8	I	PU	**PLL programming bit 8** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	F4	D12	IO	PU	**Data Bus Line 12**
		PLL7	I	PU	**PLL programming bit 7** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
3	G1	D11	IO	PU	**Data Bus Line 11**
		PLL6	I	PU	**PLL programming bit 6** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	G2	D10	IO	PU	**Data Bus Line 10**
		PLL5	I	PU	**PLL programming bit 5** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	G3	D9	IO	PU	**Data Bus Line 9**
		PLL4	I	PU	**PLL programming bit 4** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	H1	D8	IO	PU	**Data Bus Line 8**
		PLL3	I	PU	**PLL programming bit 3** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	H2	D7	IO	PU	**Data Bus Line 7**
		PLL2	I	PU	**PLL programming bit 2** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	J1	D6	IO	PU	**Data Bus Line 6**
		PLL1	I	PU	**PLL programming bit 1** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	H3	D5	IO	PU	**Data Bus Line 5**
		PLL0	I	PU	**PLL programming bit 0** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	J2	D4	IO	PU	**Data Bus Line 4**

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	J3	D3	IO	PU	**Data Bus Line 3**
	K3	D2	IO	PU	**Data Bus Line 2**
		SCI_CLK	I	–	**SCI Bus Clock** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
		SCLK	I	–	**SPI Bus Clock** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
	K1	D1	IO	PU	**Data Bus Line 1**
		SCI_RXD	I	PU	**SCI Bus Serial Data In** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
		SDI	I	PU	**SPI Serial Data In** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
	K2	D0	IO	PU	**Data Bus Line 0**
		SCI_TXD	I	PP or oD	**SCI Bus Serial Data Out** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
		SDO	I	PU	**SPI Bus Serial Data Out** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
	G15	ALE	I	PU	**Address Latch Enable** A high on this line indicates an address on an external multiplexed address/data bus. The address information provided on A(10:0) for COMP= ´0´ or A(9:0) for COMP= ´1´ is internally latched with the falling edge of ALE. This function allows the OctalFALC™ to be connected to a multiplexed address/data bus without the need for external latches. In this case, pins A(7:0) must be connected to the data bus pins externally. In case of demultiplexed mode this pin can be connected directly to VDD or can be left open.
	H16	$\overline{RD}$	I	PU	**Read Enable** Intel bus mode. This signal indicates a read operation. When the OctalFALC™™ is selected via CS, the RD signal enables the bus drivers to output data from an internal register addressed by A(10:0) to the Data Bus.
		$\overline{DS}$	I	PU	**Data Strobe** Motorola bus mode. This pin serves as input to control read/write operations.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	H15	$\overline{WR}$	I	PU	**Write Enable** Intel bus mode. This signal indicates a write operation. When CS is active the OctalFALC™™ loads an internal register with data provided on the data bus.
		$\overline{RW}$	I	PU	**Read/Write Select** Motorola bus mode. This signal distinguishes between read and write operation.
	R5	DBW	I	PU	**Data Bus Width select** Bus interface mode A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{BHE}$/$\overline{BLE}$.
	H13	$\overline{BHE}$	I	PU	**Bus High Enable** Intel bus mode. If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus D(15:8). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open.
		$\overline{BLE}$	I	PU	**Bus Low Enable** Motorola bus mode. If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus D(7:0). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open.
	H12	$\overline{CS}$	I	PU	**Chip Select** Low active chip select if SPI or SCI interface mode is selected or if COMP = ´0_B´ and micro controller mode (Intel, Motorola) is selected.
		$\overline{CS1}$	I	PU	**Chip Select 1** Low active chip select for first "pseudo" QuadFALC® if COMP = ´1_B´ and if micro controller mode (Intel, Motorola) is selected.
	H11	INT	O	–	**Interrupt Request** Interrupt request if COMP = ´0_B´. INT serves as general interrupt request for all interrupt sources. These interrupt sources can be masked via registers IMR(7:0). Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR(7:0). Output characteristics (push-pull active low/high, open drain) are determined by programming register IPC.
		INT1	O	–	**Interrupt Request 1** Interrupt request of first "pseudo" QuadFALC® if COMP = ´1_B´.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	H14	INT2	O	–	**Interrupt Request 2** Interrupt request of second "pseudo" QuadFALC® if COMP = ´1_B´.
	G14	$\overline{\text{READY}}$	O	–	**Data Ready** Only if Intel bus mode is selected. Asynchronous handshake signal to indicate successful read or write cycle.
		$\overline{\text{DTACK}}$	O	–	**Data Acknowledge** Only if Motorola bus mode is selected. Asynchronous handshake signal to indicate successful read or write cycle.
Line Interface Receiver					
	A6	RL1.1	I (analog)	–	**Line Receiver input 1, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP1	I	–	**Receive Data Input Positive, port 1** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID1	I	–	**Receive Optical Interface Data, port 1** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI1 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	A8	RL2.1	I (analog)	–	**Line Receiver input 2, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN1	I	–	**Receive Data Input Negative, port 1** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI1	I	–	**Receive Clock Input, port 1** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI1 is ignored if CMI coding is selected.
	A7	RLS21	IO (analog)	–	**Receive Line Switch, port 1** Connector of the analog switch.
	A4	RL1.2	I (analog)	–	**Line Receiver input 1, port 2** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP2	I	–	**Receive Data Input Positive, port 2** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID2	I	–	**Receive Optical Interface Data, port 2** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	A2	RL2.2	I (analog)	–	**Line Receiver input 2, port 2** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN2	I	–	**Receive Data Input Negative, port 2** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI2	I	–	**Receive Clock Input, port 2** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI2 is ignored if CMI coding is selected.
	A3	RLS22	IO (analog)	–	**Receive Line Switch, port 2** Connector of the analog switch.
	T4	RL1.3	I (analog)	–	**Line Receiver input 1, port 3** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP3	I	–	**Receive Data Input Positive, port 3** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID3	I	–	**Receive Optical Interface Data, port 3** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI3 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	T2	RL2.3	I (analog)	–	**Line Receiver input 2, port 3** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN3	I	–	**Receive Data Input Negative, port 3** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI3	I	–	**Receive Clock Input, port 3** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI3 is ignored if CMI coding is selected.
	T3	RLS23	IO (analog)	–	**Receive Line Switch, port 3** Connector of the analog switch.
	T6	RL1.4	I (analog)	–	**Line Receiver input 1, port 4** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP4	I	–	**Receive Data Input Positive, port 4** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID4	I	–	**Receive Optical Interface Data, port 4** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI4 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	T7	RL2.4	I (analog)	–	**Line Receiver input 2, port 4** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN4	I	–	**Receive Data Input Negative, port 4** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI4	I	–	**Receive Clock Input, port 4** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI4 is ignored if CMI coding is selected.
	R7	RLS24	IO (analog)	–	**Receive Line Switch, port 4** Connector of the analog switch.
	T1T	RL1.5	I (analog)	–	**Line Receiver input 1, port 5** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP5	I	–	**Receive Data Input Positive, port 5** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID5	I	–	**Receive Optical Interface Data, port 5** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI5 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	T9	RL2.5	I (analog)	–	**Line Receiver input 2, port 5** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN5	I	–	**Receive Data Input Negative, port 5** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI5	I	–	**Receive Clock Input, port 5** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI5 is ignored if CMI coding is selected.
	T10	RLS25	IO (analog)	–	**Receive Line Switch, port 5** Connector of the analog switch.
	T13	RL1.6	I (analog)	–	**Line Receiver input 1, port 6** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP6	I	–	**Receive Data Input Positive, port 6** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID6	I	–	**Receive Optical Interface Data, port 6** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI6 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	T15	RL2.6	I (analog)	–	**Line Receiver input 2, port 6** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN6	I	–	**Receive Data Input Negative, port 6** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI6	I	–	**Receive Clock Input, port 6** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI6 is ignored if CMI coding is selected.
	T14	RLS26	IO (analog)	–	**Receive Line Switch, port 6** Connector of the analog switch.
	A13	RL1.7	I (analog)	–	**Line Receiver input 1, port 7** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP7	I	–	**Receive Data Input Positive, port 7** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID7	I	–	**Receive Optical Interface Data, port 7** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI7 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	A15	RL2.7	I (analog)	–	**Line Receiver input 2, port 7** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN7	I	–	**Receive Data Input Negative, port 7** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI7	I	–	**Receive Clock Input, port 7** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI7 is ignored if CMI coding is selected.
	A14	RLS27	IO (analog)	–	**Receive Line Switch, port 7** Connector of the analog switch.
	A11	RL1.8	I (analog)	–	**Line Receiver input 1, port 8** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIP8	I	–	**Receive Data Input Positive, port 8** Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID8	I	–	**Receive Optical Interface Data, port 8** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI8 is required.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	A10	RL2.8	I (analog)	–	**Line Receiver input 2, port 8** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		RDIN8	I	–	**Receive Data Input Negative, port 8** Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI8	I	–	**Receive Clock Input, port 8** Receive clock input for the optical interface if LIM1.DRS is set and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI8 is ignored if CMI coding is selected.
	B10	RLS28	IO (analog)	–	**Receive Line Switch, port 8** Connector of the analog switch.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D7	XL1.1	O (analog)	–	**Transmit Line 1, port 1** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP1	O	–	**Transmit Data Output Positive, port 1** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK1 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID1	O	–	**Transmit Optical Interface Data, port 1** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK1. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D6	XL2.1	O (analog)	–	**Transmit Line 2, port 1** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON1	O	–	**Transmit Data Output Negative, port 1** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK1 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM1	O	–	**Transmit Frame Marker, port 1** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK1. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM1 marker is not valid.
	C7	XL3.1	I (analog)	–	**Transmit Line 3, port 1** Analog transmit input 1.
	C6	XL4.1	I (analog)	–	**Transmit Line 4, port 1** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D4	XL1.2	O (analog)	–	**Transmit Line 1, port 2** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP2	O	–	**Transmit Data Output Positive, port 2** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK2 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID2	O	–	**Transmit Optical Interface Data, port 2** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK2 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D3	XL2.2	O (analog)	–	**Transmit Line 2, port 2** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON2	O	–	**Transmit Data Output Negative, port 2** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK2 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM2	O	–	**Transmit Frame Marker, port 2** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK2. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM2 marker is not valid.
	C4	XL3.2	I (analog)	–	**Transmit Line 3, port 2** Analog transmit input 1.
	C3	XL4.2	I (analog)	–	**Transmit Line 4, port 2** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N4	XL1.3	O (analog)	–	**Transmit Line 1, port 3** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP3	O	–	**Transmit Data Output Positive, port 3** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK3 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID3	O	–	**Transmit Optical Interface Data, port 3** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK3 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N3	XL2.3	O (analog)	–	**Transmit Line 2, port 3** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON3	O	–	**Transmit Data Output Negative, port 3** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK3 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM3	O	–	**Transmit Frame Marker, port 3** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK3. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM3 marker is not valid.
	P4	XL3.3	I (analog)	–	**Transmit Line 3, port 3** Analog transmit input 1.
	P3	XL4.3	I (analog)	–	**Transmit Line 4, port 3** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	M7	XL1.4	O (analog)	–	**Transmit Line 1, port 4** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP4	O	–	**Transmit Data Output Positive, port 4** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK4 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID4	O	–	**Transmit Optical Interface Data, port 4** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK4 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	M6	XL2.4	O (analog)	–	**Transmit Line 2, port 4** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON4	O	–	**Transmit Data Output Negative, port 4** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK4 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM4	O	–	**Transmit Frame Marker, port 4** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK4. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM4 marker is not valid.
	N7	XL3.4	I (analog)	–	**Transmit Line 3, port 4** Analog transmit input 1.
	N6	XL4.4	I (analog)	–	**Transmit Line 4, port 4** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N11	XL1.5	O (analog)	–	**Transmit Line 1, port 5** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP5	O	–	**Transmit Data Output Positive, port 5** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK5 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID5	O	–	**Transmit Optical Interface Data, port 5** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK5 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N10	XL2.5	O (analog)	–	**Transmit Line 2, port 5** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON5	O	–	**Transmit Data Output Negative, port 5** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK5 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM5	O	–	**Transmit Frame Marker, port 5** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK5. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM5 marker is not valid.
	P11	XL3.5	I (analog)	–	**Transmit Line 3, port 5** Analog transmit input 1.
	P10	XL4.5	I (analog)	–	**Transmit Line 4, port 5** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N14	XL1.6	O (analog)	–	**Transmit Line 1, port 6** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP6	O	–	**Transmit Data Output Positive, port 6** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK6 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID6	O	–	**Transmit Optical Interface Data, port 6** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK6 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N13	XL2.6	O (analog)	–	**Transmit Line 2, port 6** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON6	O	–	**Transmit Data Output Negative, port 6** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK6 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM6	O	–	**Transmit Frame Marker, port 6** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK6. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM6 marker is not valid.
	P14	XL3.6	I (analog)	–	**Transmit Line 3, port 6** Analog transmit input 1.
	P13	XL4.6	I (analog)	–	**Transmit Line 4, port 6** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D14	XL1.7	O (analog)	–	**Transmit Line 1, port 7** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP7	O	–	**Transmit Data Output Positive, port 7** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK7 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID7	O	–	**Transmit Optical Interface Data, port 7** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK7 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D13	XL2.7	O (analog)	–	**Transmit Line 2, port 7** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON7	O	–	**Transmit Data Output Negative, port 7** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK7 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM7	O	–	**Transmit Frame Marker, port 7** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK7. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM7 marker is not valid.
	C14	XL3.7	I (analog)	–	**Transmit Line 3, port 7** Analog transmit input 1.
	C13	XL4.7	I (analog)	–	**Transmit Line 4, port 7** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E11	XL1.8	O (analog)	–	**Transmit Line 1, port 8** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP8	O	–	**Transmit Data Output Positive, port 8** This digital output for transmitted dual-rail PCM(+) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked with positive transitions of XCLK8 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XOID8	O	–	**Transmit Optical Interface Data, port 8** Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK8 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E10	XL2.8	O (analog)	–	**Transmit Line 2, port 8** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON8	O	–	**Transmit Data Output Negative, port 8** This digital output for transmitted dual-rail PCM(-) route signals can provide • Half bauded signals with 50% duty cycle (LIM0.XFB = 0) or • Full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data is clocked on positive transitions of XCLK8 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.
		XFM8	O	–	**Transmit Frame Marker, port 8** This digital output marks the first bit of every frame transmitted on port XDOP8. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). Data is clocked on positive transitions of XCLK8. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM8 marker is not valid.
	D11	XL3.8	I (analog)	–	**Transmit Line 3, port 8** Analog transmit input 1.
	D10	XL4.8	I (analog)	–	**Transmit Line 4, port 8** Analog transmit input 2.
Clock Signals					
	J6	MCLK	I	PU	**Master Clock** A reference clock of better than ±32 ppm accuracy in the range of 1.02 to 20 MHz must be provided on this pin. The OctalFALC™ internally derives all necessary clocks from this master (see registers GCM(6:1)).
	G13	SYNC	I	PU	**Clock Synchronization of DCO-R** If a clock is detected on pin SYNC the DCO-R circuitry of the OctalFALC™ synchronizes to this 1.544/2.048 MHz clock (see LIM0.MAS, CMR1.DCS and CMR2.DCF). Additionally, in master mode the OctalFALC™ is able to synchronize to an 8 kHz reference clock (IPC.SSYF = 1). If not connected, an internal pullup transistor ensures high input level.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	G12	SEC	I	PU	**One-Second Timer Input** A pulse with logical high level for at least two 2.048 MHz cycles triggers the internal one-second timer. After reset this pin is configured to be an input. If not connected, an internal pullup transistor ensures high input level (see register GPC1).
		SEC	O	–	**One-Second Timer Output** Activated high every second for two 2.048 MHz clock cycles.
		FSC	O	–	**8 kHz Frame Synchronization** The optionally synchronization pulse is active high or low for one 2.048/1.544 MHz cycle (pulse width = 488 ns for E1and 648 ns or T1/J1).
System Interface Receive					
	C2	RDO1	O	–	**Receive Data Out, port 1** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR1, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR1 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO1 is cleared (driven to low level, not tristate).
	C1	SCLKR1	I/O	PU	**System Clock Receive, port 1** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = ´0´) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = ´1´) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR1 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E4	RDO2	O	–	**Receive Data Out, port 2** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR2, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR2 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO2 is cleared (driven to low level, not tristate).
	E1	SCLKR2	I/O	PU	**System Clock Receive, port 2** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR2 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.
	L6	RDO3	O	–	**Receive Data Out, port 3** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR3, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR3 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO3 is cleared (driven to low level, not tristate).
	K4	SCLKR3	I/O	PU	**System Clock Receive, port 3** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR3 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	M3	RDO4	O	–	**Receive Data Out, port 4** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR4, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR4 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO4 is cleared (driven to low level, not tristate).
	M1	SCLKR4	I/O	PU	**System Clock Receive, port 4** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR4 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.
	P15	RDO5	O	–	**Receive Data Out, port 5** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR5, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR5 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO5 is cleared (driven to low level, not tristate).
	P16	SCLKR5	I/O	PU	**System Clock Receive, port 5** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR5 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	M10	RDO6	O	–	**Receive Data Out, port 6** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR6, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR6 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO6 is cleared (driven to low level, not tristate).
	M16	SCLKR6	I/O	PU	**System Clock Receive, port 6** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR6 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.
	F15	RDO7	O	–	**Receive Data Out, port 7** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR7, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR7 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO7 is cleared (driven to low level, not tristate).
	F13	SCLKR7	I/O	PU	**System Clock Receive, port 7** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR7 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E13	RDO8	O	–	**Receive Data Out, port 8** Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR8, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR8 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO8 is cleared (driven to low level, not tristate).
	E16	SCLKR8	I/O	PU	**System Clock Receive, port 8** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface. If SCLKR8 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output.
System Interface Transmit					
	E5	XDI1	I	PU	**Transmit Data In, port 1** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX1 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX1 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).
	D1	SCLKX1	I	PU	**System Clock Transmit, port 1** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
	F7	XDI2	I	PU	**Transmit Data In, port 2** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX2 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX2 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	F8	SCLKX2	I	PU	**System Clock Transmit, port 2** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
	L5	XDI3	I	PU	**Transmit Data In, port 3** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX3 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX3 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).
	L3	SCLKX3	I	PU	**System Clock Transmit, port 3** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
	P2	XDI4	I	PU	**Transmit Data In, port 4** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX4 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX4 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).
	N1	SCLKX4	I	PU	**System Clock Transmit, port 4** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
	M11	XDI5	I	PU	**Transmit Data In, port 5** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX5 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX5 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	M12	SCLKX5	I	PU	**System Clock Transmit, port 5** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
	L14	XDI6	I	PU	**Transmit Data In, port 6** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX6 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX6 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).
	L16	SCLKX6	I	PU	**System Clock Transmit, port 6** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
	F9	XDI7	I	PU	**Transmit Data In, port 7** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX1 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX1 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).
	F12	SCLKX7	I	PU	**System Clock Transmit, port 7** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
	C15	XDI8	I	PU	**Transmit Data In, port 8** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX8 according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX8 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D16	SCLKX8	I	PU	**System Clock Transmit, port 8** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = ´0´) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = ´1´) in T1/J1 mode.
Multi Function Pins					
	B1	RPA1	I/O	PU/–	**Receive Multifunction Pins A to C, port 1** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions are described below.
	D2	RPB1	I/O	PU/–	
	E7	RPC1	I/O	PU/–	
	B1	RPA1	I	PU	**Synchronous Pulse Receive, port 1** $\overline{SYPR}$, PC(1:3).RPC(3:0) = ´0000_b´ Together with the values of registers RC(1:0) this signal defines the beginning of time slot 0 on system highway port RDO. Only one multifunction port may be selected as $\overline{SYPR}$ input. After reset, $\overline{SYPR}$ of port A is used, the other lines are ignored. In system interface multiplex mode, $\overline{SYPR}$ has to be provided at port RPA1 for four or all eight channels dependent if 4:1 or 8:1 multiplex mode is selected. $\overline{SYPR}$ defines the beginning of the time slot 0 on port RDO/RSIG. The pulse cycle is an integer multiple of 125 µs.
	D2	RPB1	I	PU	
	E7	RPC1	I	PU	
	B1	RPA1	O	–	**Receive Frame Marker (RFM), port 1** PC(1:3).RPC(3:0) = ´0001_b´ **CMR2.IRSP = ´0´** The receive frame marker can be active high for a 2.048 MHz (E1) or 1.544 MHz (T1/J1) period during any bit position of the current frame. It is clocked off with the rising or falling edge of SCLKR or RCLK, depending on SIC3.RESR. Offset programming is done by using registers RC(1:0). **CMR2.IRSP = ´1´** Frame synchronization pulse generated by the DCO-R circuitry internally. This pulse is active low for a 2.048 MHz (E1) or 1.544 MHz (T1/J1) period.
	D2	RPB1	O	–	
	E7	RPC1	O	–	

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	B1	RPA1	O	–	**Receive Multiframe Begin (RMFB), port 1** PC(1:3).RPC(3:0) = ´0010_b´ In E1 mode RMFB marks the beginning of every received multiframe (RDO). Optionally the time slot 16 CAS multiframe begin can be marked (SIC3.CASMF). Active high for one 2.048 MHz period. In T1/J1 mode the function depends on bit XC0.MFBS: **MFBS = ´1´** RMFB marks the beginning of every received multiframe (RDO). **MFBS = ´0´** RMFB marks the beginning of every received superframe. Additional pulses are provided every 12 frames when using ESF/F24 or F72 format.
	D2	RPB1	O	–	
	E7	RPC1	O	–	
	B1	RPA1	O	–	**Receive Signaling Marker (RSIGM), port 1** PC(1:3).RPC(3:0) = ´0011_b´ E1: Marks the time slots which are defined by register RTR(4:1) of every received frame on port RDO. T1/J1: Marks the time slots which are defined by register RTR(4:1) of every received frame on port RDO, if CAS-BR is not used. When using the CAS-BR signaling scheme, the robbed bit of each channel every sixth frames is marked, if CAS-BR is enabled by XC0.BRM = ´1´.
	D2	RPB1	O	–	
	E7	RPC1	O	–	
	B1	RPA1	O	–	**Receive Signaling Data (RSIG), port 1** PC(1:3).RPC(3:0) = ´0100_b´ The received CAS signaling data is sourced by this pin. Time slots on RSIG correlate directly to the time slot assignment on RDO. In 4:1 or 8:1 system interface multiplex mode four or eight received signaing data streams are merged into a single data stream respectively which is transmitted on RPB1 for 8:1 mode or RPB1 and RRB5 for 4:1 mode (bit- or byte-interleaved).
	D2	RPB1	O	–	
	E7	RPC1	O	–	
	B1	RPA1	O	–	**Data Link Bit Receive (DLR), port 1** PC(1:3).RPC(3:0) = ´0101_b´ E1: Marks the Sa(8:4)-bits within the data stream on RDO. The Sa(8:4)-bit positions in time slot 0 of every frame not containing the frame alignment signal are selected by register XC0. T1/J1: Marks the DL-bit position within the data stream on RDO.
	D2	RPB1	O	–	
	E7	RPC1	O	–	
	B1	RPA1	O	–	**Freeze signaling (FREEZE), port 1** PC(1:3).RPC(3:0) = ´0110_b´ The freeze signaling status is set active high by detecting a loss of signal alarm, a loss of CAS frame alignment or a receive slip (positive or negative). It will stay high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.
	D2	RPB1	O	–	
	E7	RPC1	O	–	

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	B1	RPA1	O	–	**Frame Synchronous Pulse (RFSP) , port 1** $\overline{\text{RFSP}}$, PC(1:3).RPC(3:0) = ´0111_b´ Active low framing pulse derived from the received PCM route signal (line side, RCLK). During loss of synchronization (bit FRS0.LFA = ´1´), this pulse is suppressed (not influenced during alarm simulation). Pulse frequency: 8 kHz Pulse width: 488 ns (E1) or 648 ns (T1/J1).
	D2	RPB1	O	–	
	E7	RPC1	O	–	
	B1	RPA1	I	PU	**Receive Line Termination (RLT), port 1** PC(1:3).RPC(3:0) = ´1000_b´.
	D2	RPB1	I	PU	
	E7	RPC1	I	PU	
	B1	RPA1	I	PU	**General Purpose Input (GPI), port 1** PC(1:3).RPC(3:0) = ´1001_b. The pin is set to input. The state of this input is reflected in the register bits MFPI.RPA, MFPI.RPB or MFPI.RPC respectively.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**General Purpose Output High (GPOH), port 1** PC(1:3).RPC(3:0) = ´1010_b´. The pin level is set fix to high level.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**General Purpose Output Low (GPOL), port 1** PC(1:3).RPC(3:0) = ´1011_b´. The pin level is set fix to low level.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**Loss of Signal Indication Output (LOS), port 1** PC(1:3).RPC(3:0) = ´1100_b. The output reflects the Loss of Signal status as readable in FRS0.LOS.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	I	PU	**Receive TDM System Interface Tristate (RTDMT), port 1** PC(1:3).RPC(3:0) = ´1101_b´. Controlling of tristate mode for RDO, RSIG,SCLKR and RFM. The RTDMT value is logically exored with the register bit SIC3.RRTRI.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**Receive Data Output Negative (RDON), port 1** PC(1:3).RPC(3:0) = ´1110_b´. Receive data output negative for dual rail mode on system side (LIM3.DRR = ´1´). Bipolar violation output for single rail mode on system side (LIM3.DRR = ´0´).
	D2	RPB1			
	E7	RPC1			
	B1	RPB1	O	–	**Receive Clock Output (RCLK), port 1** PC(1:3).RPC(3:0) = ´1111_b´. Default setting after reset Receive clock output RCLK. After reset RCLK is configured to be internally pulled up weekly. By setting of PC5.CRP RCLK is an active output. RCLK source and frequency selection is made by CMR1.RS(1:0) if COMP = ´1´ or by CMR4.RS(2:0) if COMP = ´0´.
	D2	RPB1			
	E7	RPC1			

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E6	RPA2	I/O	PU/–	**Receive Multifunction Pins A to C, port 2** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions as described for port 1.
	E8	RPB2			
	E9	RPC2			
	L4	RPA3	I/O	PU/–	**Receive Multifunction Pins A to C, port 3** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions as described for port 1.
	L2	RPB3			
	L1	RPC3			
	M4	RPA4	I/O	PU/–	**Receive Multifunction Pins A to C, port 4** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions as described for port 1.
	M5	RPB4			
	N2	RPC4			

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	R16	RPA5	I/O	PU/–	**Receive Multifunction Pins A to C, port 5** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions as described for port 1.
	N1N	RPB5			
	N1N	RPC5			
	M13	RPA6	I/O	PU/–	**Receive Multifunction Pins A to C, port 6** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions as described for port 1.
	L13	RPB6			
	L15	RPC6			
	F16	RPA7	I/O	PU/–	**Receive Multifunction Pins A to C, port 7** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions as described for port 1.
	F14	RPB7			
	F10	RPC7			

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E12	RPA8	I/O	PU/–	**Receive Multifunction Pins A to C, port 8** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level. The input function must not be selected twice or more. Selectable pin functions as described for port 1.
	D15	RPB8			
	F11	RPC8			
	E3	XPA1	I/O	PU/–	**Transmit Multifunction Pins A and B, port 1** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions are described below.
	E2	XPB1	I/O	PU/–	
	E3	XPA1	I	PU	**Synchronous Pulse Transmit, port 1** $\overline{\text{SYPX}}$, PC(1:2).XPC(3:0) = ´0000_b´ Together with the values of registers XC(0:1) this signal defines the beginning of time slot 0 at system highway port XDI. The pulse cycle is an integer multiple of 125 µs. $\overline{\text{SYPX}}$ must not be used in parallel with XMFS.
	E2	XPB1	I	PU	
	E3	XPA1	I	PU	**Transmit Multiframe Synchronization (XMFS), port 1** PC(1:2).XPC(3:0) = ´0001_b´ This port defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low. XMFS must not be used in parallel with $\overline{\text{SYPX}}$. *Note: A new multiframe position has settled at least one multiframe after pulse XMFS has been supplied.*
	E2	XPB1	I	PU	

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E3	XPA1	I	PU	**Transmit Signaling Data (XSIG), port 1** PC(1:2).XPC(3:0) = ´0010_b´ Input for transmit signaling data received from the signaling highway. Optionally, (SIC3.TTRF = ´1´), sampling of XSIG data is controlled by the active high XSIGM marker. At higher data rates sampling of data is defined by bits SIC2.SICS(2:0).
	E2	XPB1	I	PU	
	E3	XPA1	I	PU	**Transmit Clock (TCLK), port 1** PC(1:2).XPC(3:0) = ´0011_b´ A 2.048/8.192 MHz (E1) or 1.544/6.176 MHz (T1/J1) clock has to be sourced by the system if the internally generated transmit clock (generated by DCO-X) shall not be used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 (E1) or 1.544 MHz (T1/J1).
	E2	XPB1	I	PU	
	E3	XPA1	O	–	**Transmit Multiframe Begin (XMFB), port 1** PC(1:2).XPC(3:0) = ´0100_b´ XMFB marks the beginning of every transmitted multiframe on XDI. The signal is active high for one 2.048 (E1) or 1.544 MHz (T1/J1) period.
	E2	XPB1	O	–	
	E3	XPA1	O	–	**Transmit Signaling Marker (XSIGM), port 1** PC(1:2).XPC(3:0) = ´0101_b´ **E1** Marks the transmit time slots on XDI of every frame which are defined by register TTR(1:4). **T1/J1** Marks the transmit time slots on XDI of every frame which are defined by register TTR(1:4) (if not CAS-BR is used). When using the CAS-BR signaling scheme the robbed bit of each channel in every sixth frame is marked.
	E2	XPB1	O	–	
	E3	XPA1	O	–	**Data Link Bit Transmit (DLX), port 1** PC(1:2).XPC(3:0) = ´0110_b´ **E1** Marks the Sa(8:4)-bits within the data stream on XDI. The Sa(8:4)-bit positions in time slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA8E to XC0.SA4E. **T1/J1** This output provides a 4 kHz signal which marks the DL-bit position within the data stream on XDI (in ESF mode only).
	E2	XPB1	O	–	
	E3	XPA1	O	–	**Transmit Clock (XCLK), port 1** PC(1:2).XPC(3:0) = ´0111_b´ Transmit line clock of 2.048 MHz (E1) or 1.544 MHz (T1/J1) derived from SCLKX/R, RCLK or generated internally by DCO circuitries.
	E2	XPB1	O	–	

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E3	XPA1	I	PU	**Transmit Line Tristate (XLT), port 1** PC(1:2).XPC(3:0) = ´1000_b´ A high level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically ored with register bit XPM2.XLT.
	E2	XPB1	I	PU	
	E3	XPA1	I	PU	**General Purpose Input (GPI), port 1** PC(1:2).XPC(3:0) = ´1001_b. The pin is set to input. The state of this input is reflected in the register bits MFPI.XPA, MFPI.XPB or MFPI.XPC respectively.
	E2	XPB1	I	PU	
	E3	XPA1	O	–	**General Purpose Output High (GPOH), port 1** PC(1:2).XPC(3:0) = ´1010_b´. The pin level is set fix to high level.
	E2	XPB1	O	–	
	E3	XPA1	O	–	**General Purpose Output Low (GPOL), port 1** PC(1:2).XPC(3:0) = ´1011_b´. The pin level is set fix to high level.
	E2	XPB1	O	–	
	E3	XPA1	I	PU	**Transmit Data Input Negative (XDIN), port 1** PC(1:2).XPC(3:0) = ´1101_b. Transmit data input negative for dual rail mode on system side (LIM3.DRX = ´1´).
	E2	XPB1	I	PU	
	E3	XPA1	I	PU	**Transmit Line Tristate, low active, port 1** $\overline{\text{XLT}}$: PC(1:2).XPC(3:0) = ´1110_b´. A low level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically ored with register bit XPM2.XLT.
	E2	XPB1	I	PU	
	F5 F6	XPA2 XPB2	I/O	PU/–	**Transmit Multifunction Pins A and B, port 2** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions as described for port 1.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	L7 M7	XPA3 XPB3	I/O	PU/–	**Transmit Multifunction Pins A and B, port 3** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions as described for port 1.
	P1 R1	XPA4 XPB4	I/O	PU/–	**Transmit Multifunction Pins A and B, port 4** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions as described for port 1.
	M14 M15	XPA5 XPB5	I/O	PU/–	**Transmit Multifunction Pins A and B, port 5** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions as described for port 1.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	L12 L11	XPA6 XPB6	I/O	PU/–	**Transmit Multifunction Pins A and B, port 6** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions as described for port 1.
	E14 E15	XPA7 XPB7	I/O	PU/–	**Transmit Multifunction Pins A and B, port 7** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions as described for port 1.
	C16 B16	XPA8 XPB8	I/O	PU/–	**Transmit Multifunction Pins A and B, port 8** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the OctalFALC™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level. Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel. Selectable pin functions as described for port 1.
Power Supply					
	B7	V_{DDR1}	S	–	**Positive Power Supply** For the analog receiver 1 (3.3 V)
	B5	V_{DDR2}	S	–	**Positive Power Supply** For the analog receiver 2 (3.3 V)

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	R4	V_{DDR3}	S	–	**Positive Power Supply** For the analog receiver 3 (3.3 V)
	R6	V_{DDR4}	S	–	**Positive Power Supply** For the analog receiver 4 (3.3 V)
	R11	V_{DDR5}	S	–	**Positive Power Supply** For the analog receiver 5 (3.3 V)
	R12	V_{DDR6}	S	–	**Positive Power Supply** For the analog receiver 6 (3.3 V)
	B13	V_{DDR7}	S	–	**Positive Power Supply** For the analog receiver 7 (3.3 V)
	B11	V_{DDR8}	S	–	**Positive Power Supply** For the analog receiver 8 (3.3 V)
	C8	V_{DDX1}	S	–	**Positive Power Supply** For the analog transmitter 1
	D8				
	C5	V_{DDX2}	S	–	**Positive Power Supply** For the analog transmitter 2
	D5				
	N5	V_{DDX3}	S	–	**Positive Power Supply** For the analog transmitter 3
	P5				
	N8	V_{DDX4}	S	–	**Positive Power Supply** For the analog transmitter 4
	P8				
	N9	V_{DDX5}	S	–	**Positive Power Supply** For the analog transmitter 5
	P9				
	N12	V_{DDX6}	S	–	**Positive Power Supply** For the analog transmitter 6
	P12				
	C12	V_{DDX7}	S	–	**Positive Power Supply** For the analog transmitter 7
	D12				
	C9	V_{DDX8}	S	–	**Positive Power Supply** For the analog transmitter 8
	D9				
	G4	V_{DDC}	S	–	**Positive Power Supply** For the digital core (1.8 V)
	G11				
	H4				
	J4				
	L8				
	L9				
	L10				
	H6	V_{DDPLL}	S	–	**Positive Power Supply** For the analog PLL

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	G5	V_{DDP}	S	–	**Positive Power Supply** For the digital pads (3.3 V) For correct operation, all V_{DD} pins have to be connected to positive power supply.
	H5				
	J5				
	K5				
	J11				
	K11				

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	A5	V_{SS}	S	–	**Power Ground** Common for all sub circuits (0 V) For correct operation, all V_{SS} pins have to be connected to ground.
	A9				
	A12				
	B2				
	B9				
	B12				
	B14				
	B15				
	C10				
	C11				
	G6				
	G7				
	G8				
	G9				
	G10				
	H7				
	H8				
	H9				
	H10				
	J7				
	J8				
	J9				
	J10				
	K6				
	K7				
	K8				
	K9				
	K10				
	P7				
	R2				
	R3				
	R8				
	R13				
	R14				
	R15				
	T5				
	T8				
	T12				

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
Boundary Scan/Joint Test Access Group (JTAG)					
	P6	$\overline{\text{TRS}}$	I	PD	**Test Reset** For Boundary Scan (active low). If not connected, an internal pullup transistor ensures high input level. If the JTAG boundary scan is not used, this pin must be connected to $\overline{\text{RES}}$ or V_{SS}.
	M9	TDI		PU	**Test Data Input** For Boundary Scan. If not connected an internal pullup transistor ensures high input level.
	M8	TMS			**Test Mode Select** For Boundary Scan. If not connected an internal pullup transistor ensures high input level.
	R9	TCK			**Test Clock** For Boundary Scan. If not connected an internal pullup transistor ensures high input level.
	R10	TDO	O	–	**Test Data Output** For Boundary Scan

Note: oD = open drain output PU = input or input/output comprising an internal pullup device To override the internal pullup by an external pulldown, a resistor value of 22 kΩ is recommended. The pullup devices are activated during reset, this means their state is undefined until the reset signal has been applied. Unused pins containing pullups can be left open.

2.3 Pin Strapping

Some pins are used for selection of functional modes of the OctalFALC™:

Table 2 Overview about the Pin Strapping

PIN	Pin Strapping is used	Pin Strapping Function
COMP	Always	Defines the compatibility mode, see **Chapter 3.1.1**.
IM(1:0)	Always	Defines the used micro controller interface, see **Chapter 3.4**
A(10)	Only in asynchronous micro controller interface mode	Second chip select signal in compatibility mode, see **Chapter 3.1.1**.
A(5:0)	Only in SCI interface mode	Defines the six LSBs of the SCI source address, see **Chapter 3.4.2.1**
D(15:5)	Only in SCI or SPI interface mode	Programs the parameters N and M of the PLL in the master clocking unit instead of registers GCM5 and GCM6, see **Chapter 3.4.6** and **GCM6_E**. - D(15:11) values programs PLL dividing factor M - D(10:5) values programs PLL dividing factor N Programming by pin strapping is equivalent to programming by register bits GCM5.PLL_M(4:0) and GCM6.PLL_N(5:0) which is used in asynchronous micro controller modes.

3 Functional Description E1/T1/J1

3.1 Compatibility

To ensure an easy transition from QuadFALC® to OctalFALC™ designs, software written for the QuadFALC® can be used for the OctalFALC™ without changes. Board space is saved by using a PG-LBGA-256 package.

3.1.1 Software Compatibility

The OctalFALC™ device contains analog and digital function blocks that are configured and controlled by an external microprocessor or micro controller, using either the asynchronous interface, SPI bus or SCI bus.

The OctalFALC™ can be used in two basic modes. The “QuadFALC® Compatibility Mode” allows to use the device like two separate QuadFALC®s (“pseudo QuadFALC®”s) whereas the “OctalFALC™ Generic Mode” handles the device as a single entity. The “Compatibility Mode” option ensures an easy transition of designs from QuadFALC® to OctalFALC™, software written for the QuadFALC® can be used for the OctalFALC™ without changes. As for the QuadFALC® the register addresses are 10 bits wide.

In the “OctalFALC™ Generic Mode” the register addresses are 11 bit wide.

The compatibility mode is choosen by a high level on pin COMP. An overview is given in **Table 3**.

Additional features are available also in compatibility mode, but are disabled by default and must be activated by software.

If compatibility mode is selected, the version status register VSTR shows the same value as in QuadFALC® V2.1 while the JTAG boundary scan ID is always the OctalFALC™ number and not affected by the mode selection. In compatibility mode the behavior of the clocking system is the same as in the QuadFALC®. The multi function pin RPC has the function RCLK after reset (Register bits PC1.RPC(3:0)).

In compatibility mode, and if asynchronous micro controller mode is selected, the pin A(10) - active high - is used as a second chip select signal (CS2) - active low - for the second pseudo QuadFALC®, see **Figure 5** and **Table 3**. The first pseudo QuadFALC® is selected by CS1. Simultaneous activation of both chip selects is not allowed.

The SPI bus or SCI bus can be used also in compatibility mode.

In compatibility mode, every global register exists one times in both of the pseudo QuadFALC®s : CIS, GPC(1:6), IPC, VSTR, GIS, GCM(1:8), GIMR, GIS2, GLC1, INBLDTR, DSTR and PRBSTS(1:4), see also **Table 63**.

In compatibility mode, the registers regarding the central clock PLL, GCM(1:8), exist for each of the pseudo QuadFALC®'s, but the registers of the pseudo QuadFALC® 2 are “dummies”: Writing and reading is possible but their values are not taken for any configuration of the PLL. The PLL is NOT reset by writing the GCM5 and GCM6 registers accociated with pseudo QuadFALC® 2. Only the registers GCM(1:8) of the pseudo QuadFALC® 1 are taken for configuration of the PLL and changing contencies of registers GCM5 or GCM6 causes a reset of the PLL as in QuadFALC® , see also **Chapter 3.4.6.1**.

In compatibility mode the status registers regarding the central clock PLL, GIS2 and GIMR, exists one times in both of the pseudo QuadFALC®s: The status of the main PLL is “doubled” and can be masked individually in every of the both pseudo QuadFALC®s.

In generic mode only a single instance of the registers GIMR, GIS2 and GCM(1:8) exists in the whole device.

In compatibility mode, the version status register VSTR shows the same value as in QuadFALC® V2.1 while the JTAG boundary scan ID is always the OctalFALC™ number and not affected by the compatibility mode selection.

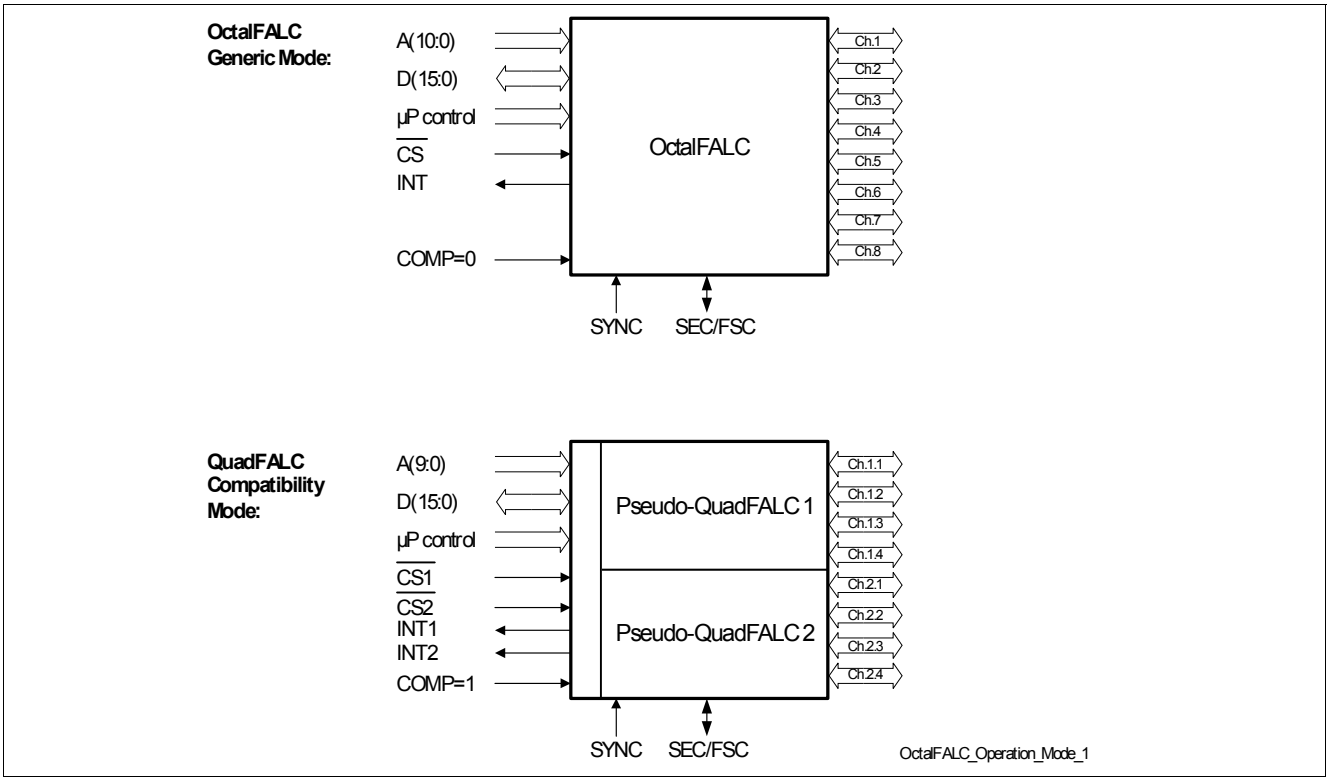


Figure 5 Basic Operation Modes

Table 3 Overview Interface- and Basic Operation- Modes

Interface Mode	IM(1:0)	COMP	$\overline{CS}$	A(10)	A(9:0)	Basic Operation Modes
Intel or Motorola	´0X´	1	$\overline{CS1}$ for pseudo QuadFALC® 1	$\overline{CS2}$ for pseudo QuadFALC® 2	10 bit parallel address	“Compatibility Mode”
		0	$\overline{CS}$	11 bit parallel address		“Generic Mode”
SPI	´10´	Not valid	$\overline{CS}$	Not valid: serial addresses are always 11 bit wide		
SCI	´11´					

3.1.2 Hardware Compatibility

The OctalFALC™ always requires two supply voltages, 1.8 V and 3.3 V. The 3.3 V-only mode usable with QuadFALC® (V1.3 and V2.1) is not supported. (So no internal voltage regulator exists in the OctalFALC™).

To accommodate the PG-LBGA-256 package the number of multifunction ports is reduced to three in the receive and two in the transmit direction per channel. Furthermore RCLK signals are provided on multifunction ports instead of separate pins.

3.2 Functional Overview

The OctalFALC™ device contains analog and digital function blocks that are configured and controlled by an external microprocessor or micro controller either over an asynchronous interface or over the SPI bus or over the SPI bus.

The main interfaces are

- Receive and transmit line interface
- PCM system highway interface/H.100 bus
- Asynchronous Microprocessor interface with two modes: Intel or Motorola
- SPI Bus interface
- SCI Bus interface
- Boundary scan interface

As well as several control lines for reset, mode and clocking purpose.

The main internal functional blocks are

- Analog line receiver with equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper and line build out
- Master clock generation module
- Elastic buffers for receive and transmit direction, controlled by the appropriate jitter attenuators
- Receive Framer, receive line decoding, alarm detection, PRBS and performance monitoring
- Transmit framer, transmit line encoding, alarm and PRBS generation
- Receive jitter attenuator
- Transmit jitter attenuator
- Three HDLC controllers (one of them including SS7 and BOM support) and CAS signaling controller per port
- Available test loops: Local loop, remote loop, payload loop and single time slot
- Register access interface
- Boundary scan control

3.3 Block Diagram

Figure 6 shows the block diagram of the OctalFALC™.

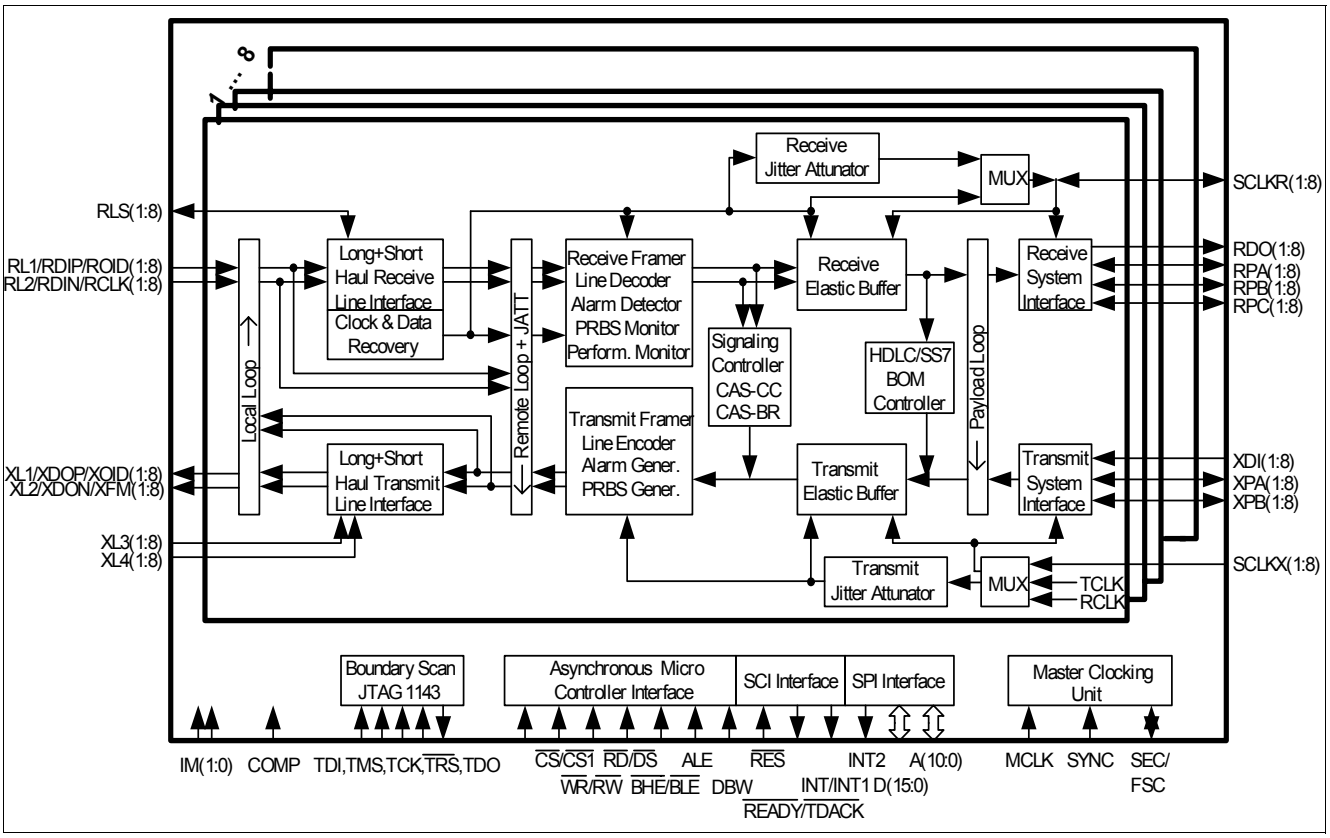


Figure 6 Block Diagram

3.4 Functional Blocks

The four possible micro controller interface modes - two asynchronous modes (Intel, Motorola) and two serial interface modes (SPI bus or SCI bus) - are selected by using the interface mode selection pins IM(1:0). This selection is valid immediately after reset becomes inactive.

After changing of the interface mode by IM(1:0), a hardware reset must be applied.

3.4.1 Asynchronous Micro Controller Interface (Intel or Motorola mode)

The asychronous micro controller interface is selected if IM(1:0) is strapped to ´00B´ (Intel mode) or ´01B´ (Motorola mode).

Compared to the QuadFALC®,an additional handshake signal (data acknowledge $\overline{\text{DTACK}}$ for Motorola- and READY for Intel-mode) is provided indicating a successful read or write cycle. By using $\overline{\text{DTACK}}$ or READY respectively no counter is necessary in the micro controller to finish the access, see also timing diagrams Figure 101 ff.

The generation of READY is asynchronous:

In Intel mode read access READY will be set to low by the OctalFALC™ after the data output is stable at the OctalFALC™. After the rising edge of RD (which is driven by the micro controller), READY is low for a “hold time”, before it will be set to high by the OctalFALC™..

In the Intel mode write access READY will be set to low by the OctalFALC™ after the falling edge of WR (which is driven by the micro controller). After WR is high and data are written successfully into the registers of the OctalFALC™, READY will be set to high by the OctalFALC™.

The general timing diagrams are shown in Figure 101 to Figure 106.

The communication between the external micro controller and the OctalFALC™ is done using a set of directly accessible registers. The interface can be configured as Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The external micro controller transfers data to and from the OctalFALC™, sets the operating modes, controls function sequences, and gets status information by writing or reading control and status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal BHE / $\overline{\text{BLE}}$ as shown in **Table 4** and **Table 5**.

Table 6 shows how the ALE (**A**ddress **L**atch **E**nable) line is used to control the bus structure and interface type. The switching of ALE allows the OctalFALC™ to be directly connected to a multiplexed address/data bus.

3.4.1.1 Mixed Byte/Word Access to the FIFOs

Reading from or writing to the internal FIFOs (RFIFO and XFIFO, for example **RFIFO1L_E** and **XFIFO1L_E** for HDLC channel 1) can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access to the FIFOs is allowed without any restrictions.

Table 4 Data Bus Access (16-Bit Intel Mode)

$\overline{\text{BHE}}$	A0	Register Access	OctalFALC™ Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D(15:0)
0	1	Register byte access (odd addresses)	D(15:8)
1	0	Register byte access (even addresses)	D(7:0)
1	1	No transfer performed	None

Table 5 Data Bus Access (16-Bit Motorola Mode)

$\overline{\text{BLE}}$	A0	Register Access	OctalFALC™ Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D(15:0)
0	1	Register byte access (odd addresses)	D(7:0)
1	0	Register byte access (even addresses)	D(15:8)
1	1	No transfer performed	None

Table 6 Selectable asynchronous Bus and Microprocessor Interface Configuration

ALE	IM(1:0)	Asynchronous Microprocessor Interface Mode	Bus Structure
Constant level	01	Motorola	de-multiplexed
	00	Intel	de-multiplexed
Switching	00	Intel	Multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected asynchronous microprocessor interface mode:

Intel	(Address n + 1)		(Address n)	
Motorola	(Address n)		(Address n + 1)	
	↑		↑	
	↓		↓	
Data lines	D15	D8	D7	D0

n: even address

3.4.2 Serial Micro Controller Interfaces

Two serial interfaces are included to enable device programming and controlling:

- Slave Serial Control Interface (SCI)
- Slave Serial Peripheral Interface (SPI)

In compatibility mode both of these new interfaces are also supported.

By using the SCI Interface, the OctalFALC™ can be easily connected to Infineon interworking devices plus Infineon SHDSL- and ADSL-PHYs so that implementation of different line transmission technologies on the same line card easily is possible. The SCI interface is a three-wire bus and optionally replaces the parallel processor interface to reduce wiring overhead on the PCB, especially if multiple devices are used on a single board. Data on the bus is HDLC encapsulated and uses a message-based communication protocol.

If SCI interface with multipoint to multipoint configuration is used, address pins A(5:0) are used for SCI source (slave) address pin strapping, see **Table 2**.

Note that after a reset writing into or reading from OctalFALC™ registers using the SCI- or SPI-Interface is not possible until the PLL is locked: If the SCI-Interface is used no acknowledge message will be sent by the OctalFALC™. If the SPI-Interface is used pin SDO has high impedance (SDO is pulled up by external resistor). To trace if the SPI interface is accessible, the micro controller should poll for example the register DSTR so long as it read no longer the value ´F_H´.

3.4.2.1 SCI Interface

The Serial Control Interface (SCI) is selected if IM(1:0) is strapped to ´11H´.

The OctalFALC™ SCI interface is always a slave.

Figure 107 shows the timing diagram of the SCI interface, **Table 145** gives the appropriate values of the timing parameters.

The data transfer on the SCI interface is HDLC encapsulated (bit oriented HDLC according to ISO 3309-1984).

Figure 7 shows an application using the SCI interfaces of multiple OctalFALC™s where point to point full duplex connections are realized between each OctalFALC™ and the micro controller. Here the data out pins of the SCI interfaces (SCI_TXD) of the OctalFALC™s must be configured as push-pull (PP), see configuration register bit PP in **Table 9**.

Figure 8 shows an application with Multipoint to multipoint connections between the OctalFALC™s and the micro controller (half duplex). Here the data out pin of the SCI interfaces (SCI_TXD) of all OctalFALC™s must be configured as an open Drain (oD), see configuration register bit PP in **Table 9**. The data out and data in pins (SCI_RXD, SCI_TXD) of each OctalFALC™ are connected together to form a common data line. Together with a common pull up resistor for the data line, all open Drain data out pins form a wired And.

The Infineon proprietary Daisy-Chain approach is not supported

The group address of the SCI interface is ´00_H´ after reset. Recommendation for configuring is ´$C4_H$´ to be different to the group addresses of all other Infineon devices.

In the case of multipoint to multipoint applications the 6 MSBs of the SCI source address will be defined by pinstrapping the address pins A5 to A0. The two LSBs of the SCI source address are constant ´10B´, see **Table 9**. The SCI source address can be overwritten by a write command into the SCI configuration register. For applications with point to point connections on the SCI interface, the source address is not valid.

Because 14 bits are used for the register addresses in the SCI interface macro, the two MSBs of the 16 bit wide register addresses are set fixed to zero.

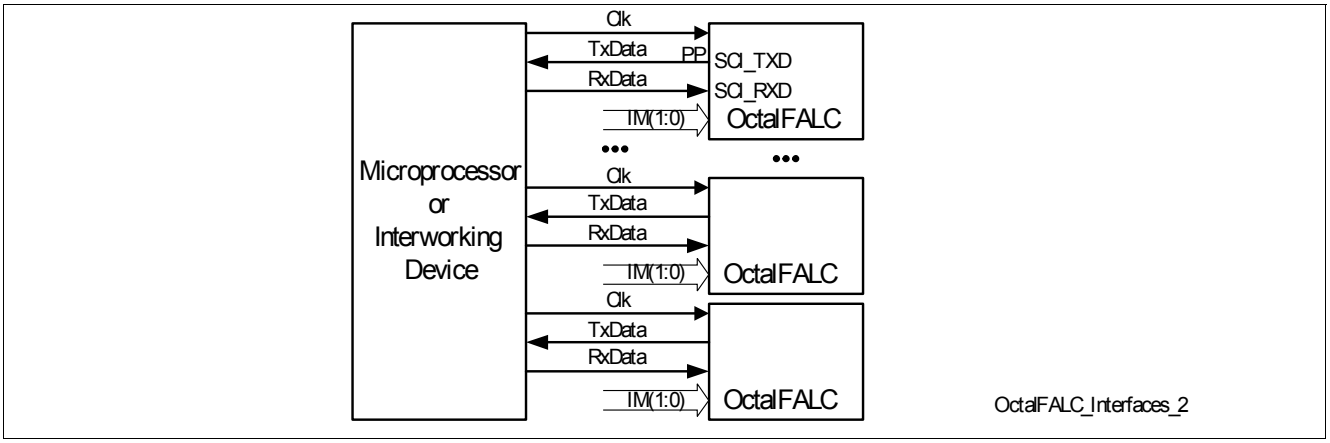


Figure 7 SCI Interface Application with Point To Point Connections

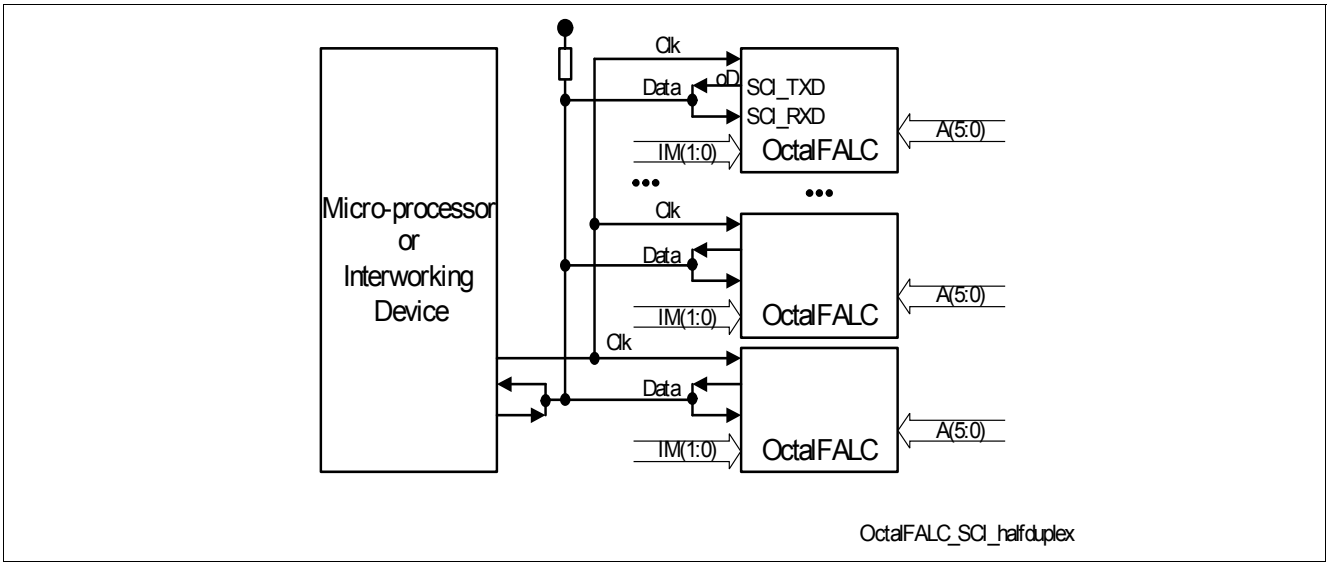


Figure 8 SCI Interface Application with Multipoint To Multipoint Connection

The following configurations of the SCI interface of the OctalFALC™ can be set by the micro controller by a write command to the SCI configuration register (control bits ´10B´, see **Table 9**, SCI register address is ´0000H´, see **Table 4** and **Figure 10**):

- Half duplex/full duplex (reset value: Half duplex), bit DUP.
- openDrain/push-pull (configuration of output pin to openDrain/push-pull is in general independent of the duplex mode and must be set appropriately depending on the application.) (reset value: open Drain), bit PP.
- CRC for transmit and receive on/off (reset value: off), bit CRC_EN.
- Automatic acknowledgement of CMD messages on/off (reset value: off), bit ACK_EN.
- Clock edge rising/falling (reset value: falling), bit CLK_POL.
- Clockgating (reset value: off), bit CLK_GAT.

The following SCI configurations are fixed and cannot be set by the micro controller:

- Interrupt feature is disabled, bit INT_EN = ´0B´.
- Arbitration always made with LAPD (only SCI applications like in **Figure 7** and **Figure 8** are possible), bit ARB = ´0B´.

The maximum possible SCI clock frequency is 6 MHz for point to point applications (full duplex) and about 2 MHz for multipoint to multipoint applications, dependent on the electrical capacity of the bus lines of the PCB.

Figure 9 shows the message structure of the OctalFALC™. Because the SCI interface uses HDLC frames for communication, HDLC flags mark beginning and end of all messages.

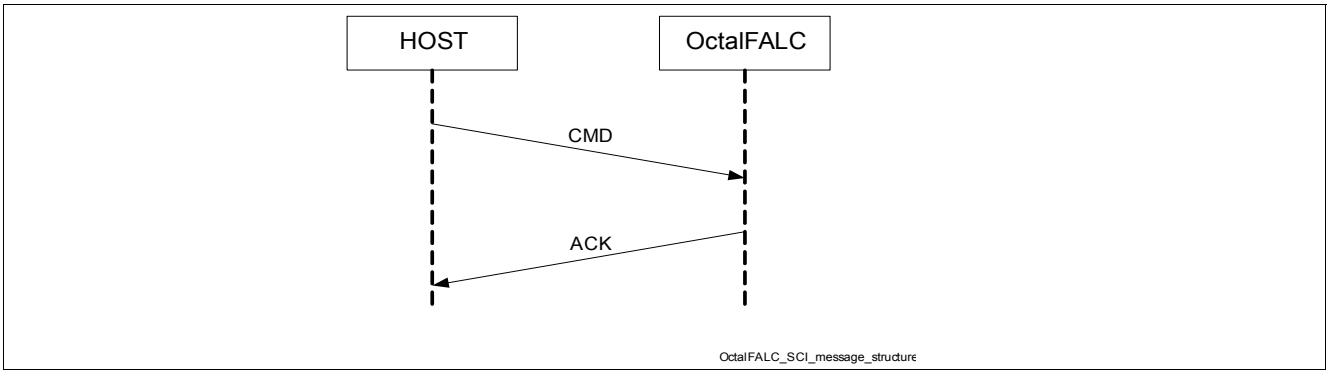


Figure 9 SCI Message Structure of OctalFALC™

Every write into or read from a register of the OctalFALC™ is initiated by a command message CMD from the Host (microcontroller). Write commands are only confirmed by an acknowledge message ACK from the OctalFALC™ if the automatic acknowledgement is set (bit ACK_EN, see **Table 9**). Read commands are always confirmed, independent on the bit ACK_EN.

The frame structure of this messages are shown in **Figure 10**.

In general the LSB of every byte is transmitted first and lower bytes are transmitted before higher bytes (regarding the register address)

Source and destination addresses are 8 bits long. Only the first 6 bits are really used for addressing. The bit C/R (Command/Response) distinguishes between a command and a response. The bit MS (Master/Slave) is ´0B´ for all Slaves and ´1B´ for all masters, see **Table 9** and **Figure 10**

The source address is defined by pinstrapping of A5 to A0 after reset, but other values can be configured by programming the SCI configuration register.

The payload of the write CMD includes two control bits (MSBs of the payload), which distinguish between the different types of commands, see **Table 8**, the 14 bit wide register address and the 8 bit wide data whereas the read CMD payload includes only the control bits and the register address. Register addresses can be either OctalFALC™ register addresses or SCI configuration register addresses. Because of the address space of the OctalFALC™, only 11 LSBs of the 14 bit address are used in the OctalFALC™. The 3 MSBs are ignored

The payload of the read ACK includes the content of the register (one byte) in addition to the payload of the write ACK.

The Frame Check Sequence FCS has 16 bits and is build (or checked) over the address and payload according to ISO 3309-1984.

The Read Status Byte RSTA of the acknowledge message shows the status of the received message and is built by the SCI interface of the OctalFALC™, see **Figure 12** and **Table 7**.

The destination address in the ACK message is always the source address of the corresponding CMD (the address of the micro controller), see **Figure 11**, because no CMD messages will be sent by the OctalFALC™ SCI interface

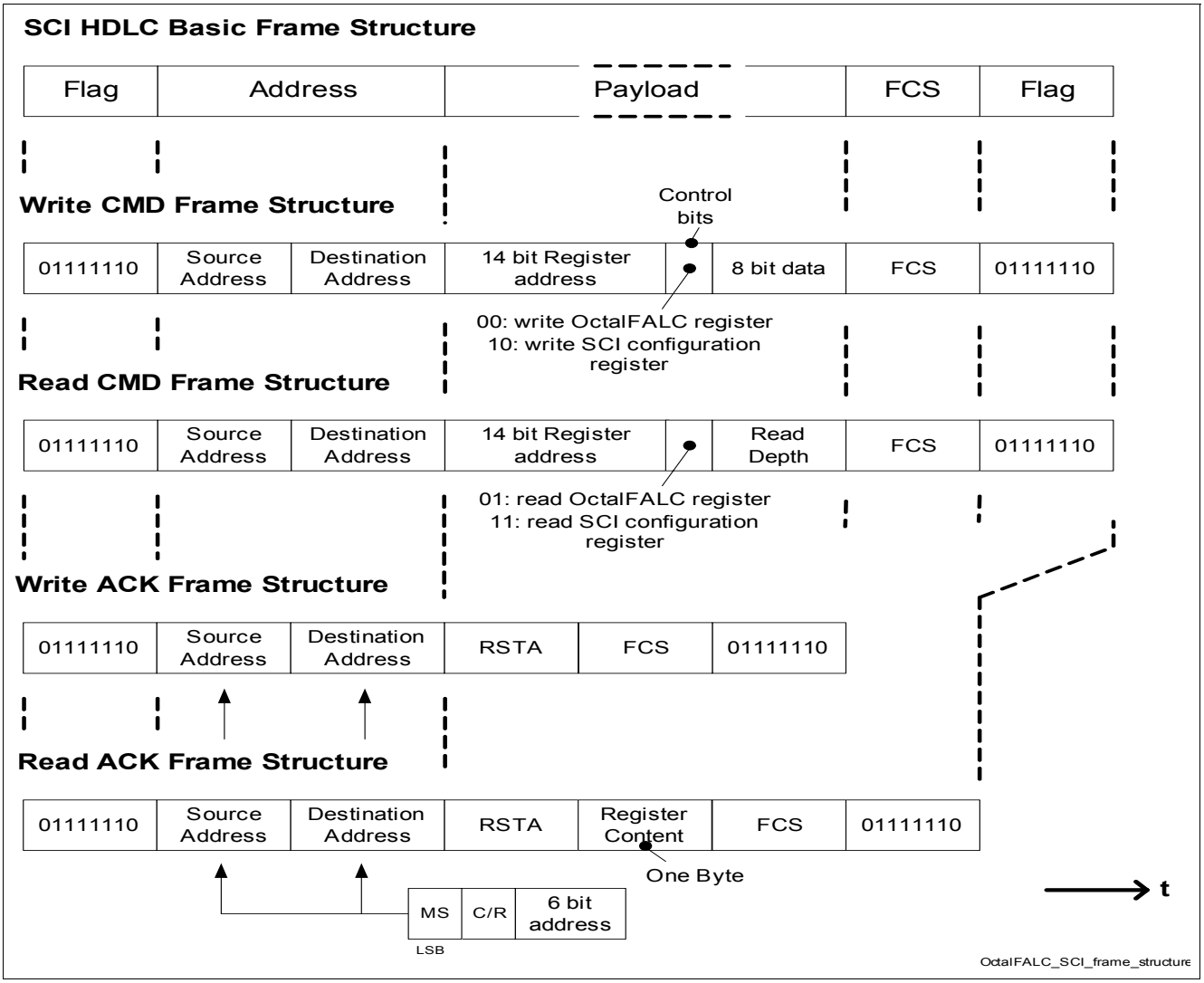


Figure 10 Frame Structure of OctalFALC™ SCI Messages

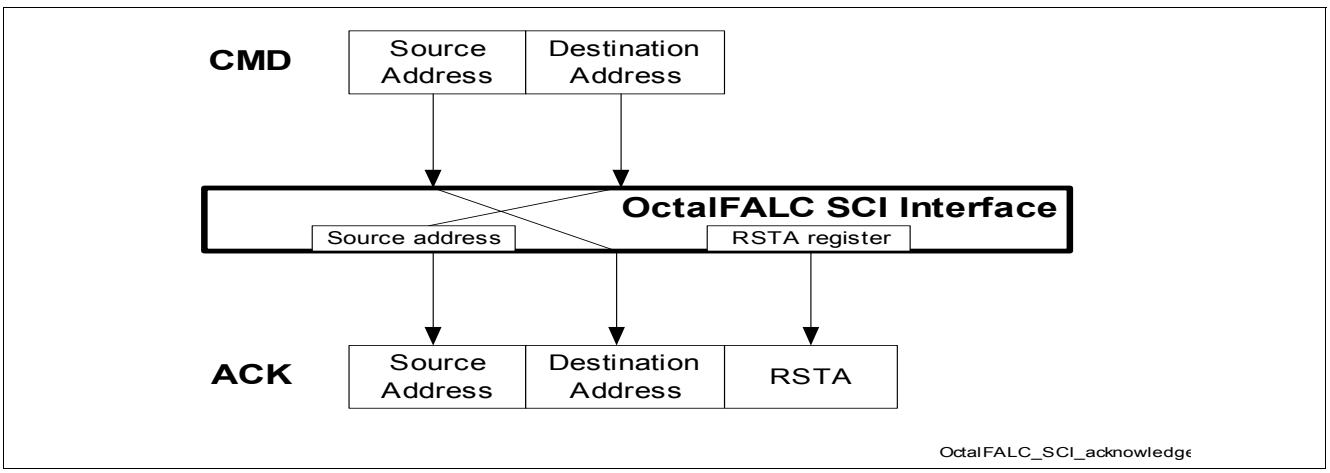


Figure 11 Principle of Building Addresses and RSTA bytes in the SCI ACK Message of the OctalFALC™

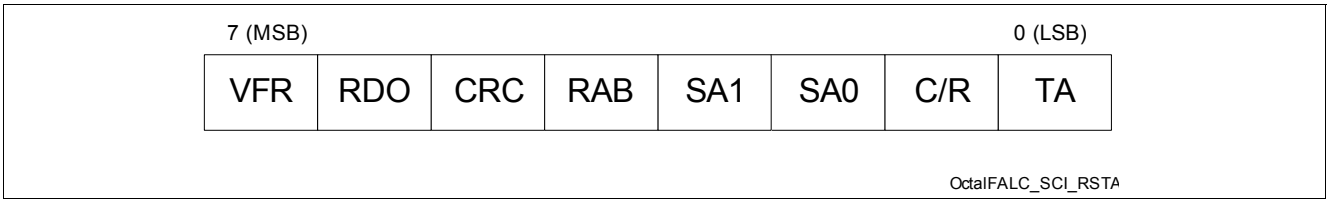


Figure 12 Read Status Byte (RSTA) byte of the SCI Acknowledge (ACK)

Table 7 Read Status Byte (RSTA) Byte of the SCI Acknowledge (ACK)

Field	Bit	Description
VFR	7	Valid Frame. Indicates whether a valid frame has received. ´0´: Received frame is invalid. ´1´: Received frame is valid.
RDO	6	Reserved
CRC	5	CRC compare check. Indicates whether a CRC check is failed or not. ´0´: CRC error check failed on the received frame. ´1´: Received frame is free of CRC errors.
RAB	4	Received message aborted. CMD message abortion is declared. The receive message was aborted by the HOST. A sequence of 7 consecutive ´1´ was detected before closing the flag. Note that ACK message and therefore RAB will not be send before destination address was received. ´0´: Data reception is in progress. ´0´: Data reception has been aborted.
SA1	3	Reserved
SA0	2	Reserved
C/R	1	Reserved
TA	0	Reserved

Table 8 Definition of Control Bits in Commands (CMD)

Control Bits (MSB LSB)	Command type
01	read OctalFALC™ registers
00	write OctalFALC™ register1
10	write SCI configuration register
11	read SCI configuration register

Table 9 SCI Configuration Register Content

Address	bit 7 (MSB)	bit6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
´0000_H´	PP	CLK_POL	CLK_GAT	ACK_EN	INT_EN	CRC_EN	ARB	DUP
´0001_H´	1	Destination Address					1 (=C/R)	0 (=MS)
´0002_H´	0	Group Address					1 (=C/R)	0 (=MS)

3.4.2.2 SPI Interface

The Serial Peripheral Interface (SPI) is selected if IM(1:0) is strapped to ´10_H´ .

The SPI interface of the OctalFALC™ is always a slave.

Figure 13 and **Figure 14** show the read and the write operation respectively. The start of a read or write operation is indicated by the falling edge of the chip select signal CS whereas the end of the operation is indicated by the rising edge of CS. Because of CS the SPI interface has no slave address.

The first bit of the serial data in (SDI) is ´1´ for a read operation and ´0´ for a write operation. The first four bits of the 15 bit address are not valid for the OctalFALC™ .

In read operation the OctalFALC™ delivers the 8 bit wide content of the addressed register at the serial data out (SDO).

In general SPI data are driven with the negative edge of the serial clock (SCLK) and sampled with the positive edge of SCLK. **Figure 108** shows the timing of the SPI interface and **Table 146** the appropriate timing parameter values.

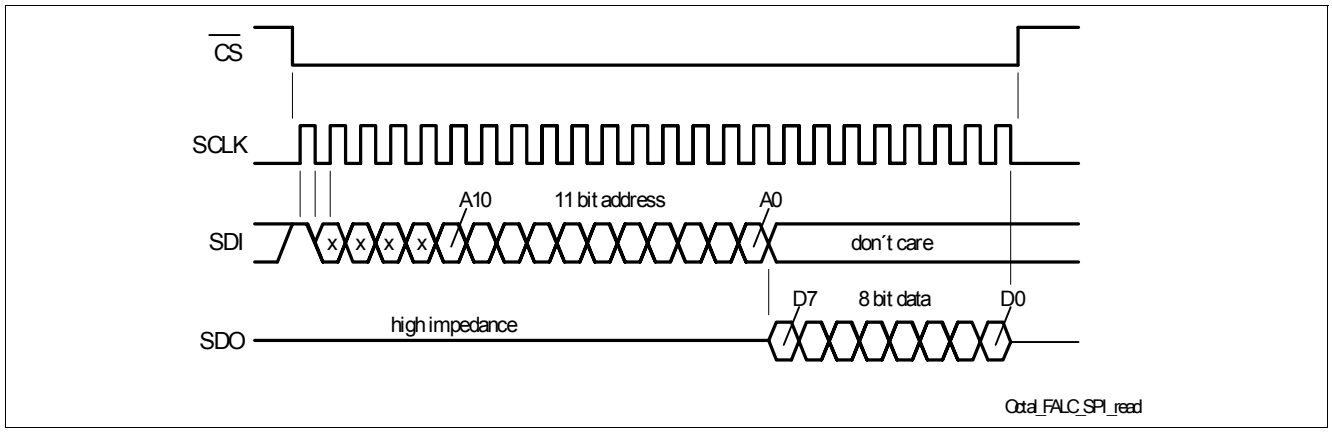


Figure 13 SPI Read Operation

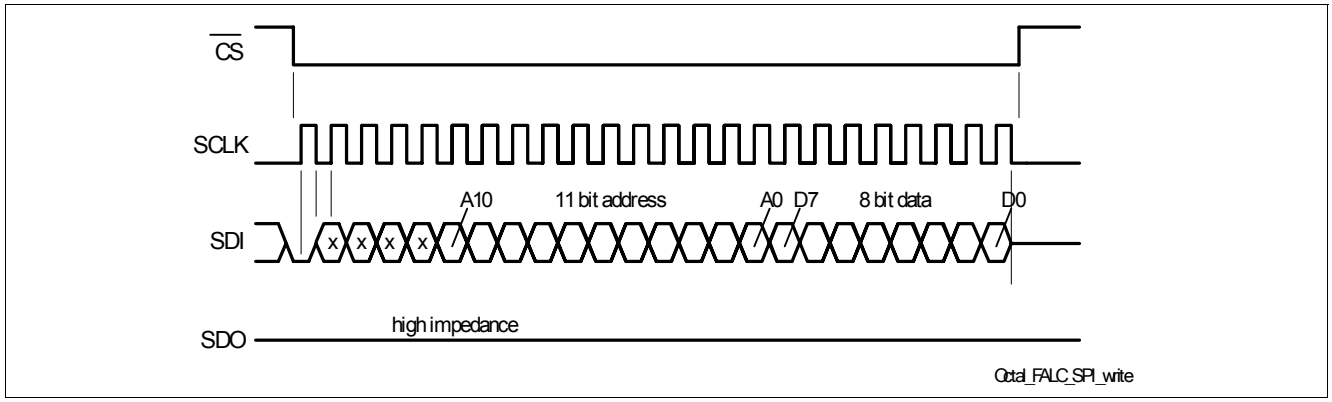


Figure 14 SPI Write Operation

3.4.3 FIFO Structure

For each of the three HDLC/BOM signaling controllers per port, there is one FIFO for transmit and one FIFO for receive. The FIFOs provide intermediate storage of data between the system internal highway (internal datastream) and the micro controller interface. The FIFO depth of all three transmit FIFOs can be configured by CCR2.TFTS up to 128 bytes. The FIFO depth of the receive FIFOs can be configured individually by CCR1.RFT(1:0) (**CCR1_E**, **CCR1_T**) and MODE.RFT2 (**MODE_E**, **MODE_T**) for the HDLC channel 1, CCR3.RFT(2:0)2 for the HDLC channel 2 and CCR3.RFT(2:0)3 for the HDLC channel 3 up to 128 bytes, see **Table 10**. The FIFOs are divided into two halves. Only one half is accessible to the external micro controller at any time.

The total length of the received frame can be directly read in registers RBCL and RBCH after a RME interrupt.

If an HDLC frame was completely received, the content of the register RSIS (for HDLC channel1, RSIS2 and RSIS3 for HDLC channel 2 and 3) will be written as last byte into the receive FIFO.

Table 10 Receive FIFO User Depth (HDLC channel 1) and Bit Positions in Register RBCL

Depth (#bytes)	CCR1.RFT(1:0)	MODE:RFT2	Bit Positions in RBCL. Reset by a CMDR.RMC Command
32	00	0	RBC(4:0)
6	01	0	RBC(3:0)
4	10	0	RBC(1:0)
2	11	0	RBC0
64	xx	1	RBC(5:0)

If the asynchronous micro controller interface mode using 16-bit data bus width is selected by IM(1) = ´0´ and DBW = ´1´, then word access to the FIFOs is enabled. The data output to the bus lines D(15:0) will be a function of the selected interface mode which is shown in **Figure 15** and **Figure 16**. Note, byte access is also allowed in asynchronous micro controller interface mode. If either the SCI or SPI are selected then only byte access is possible.

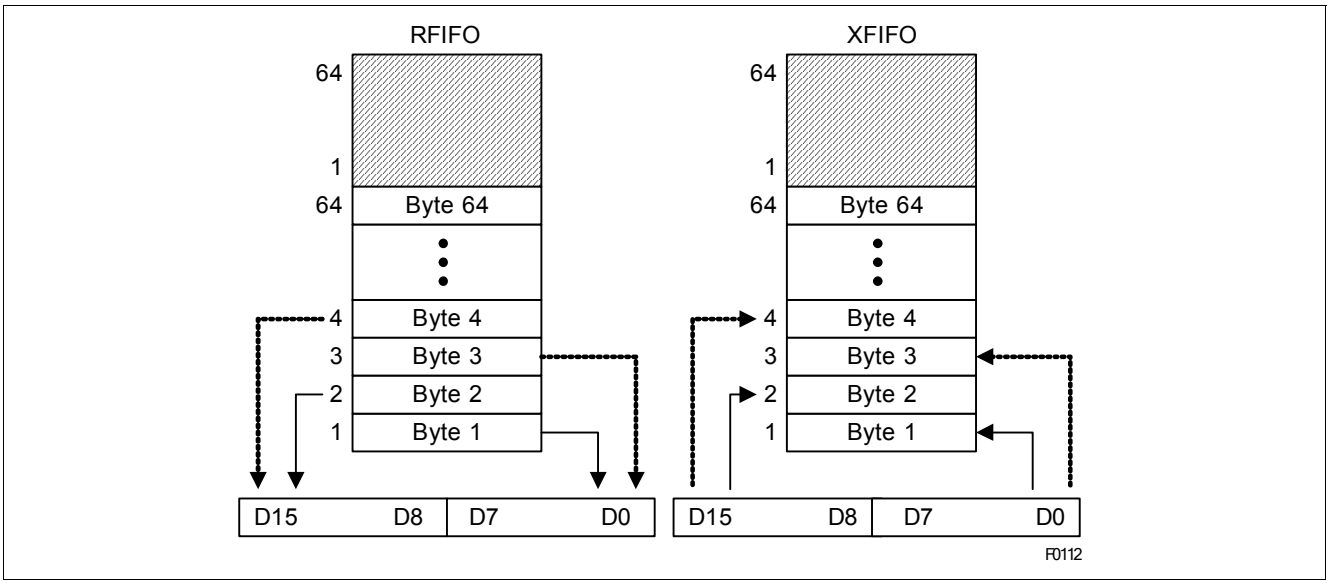


Figure 15 FIFO Word Access in Intel Mode (shown for 128 byte depth)

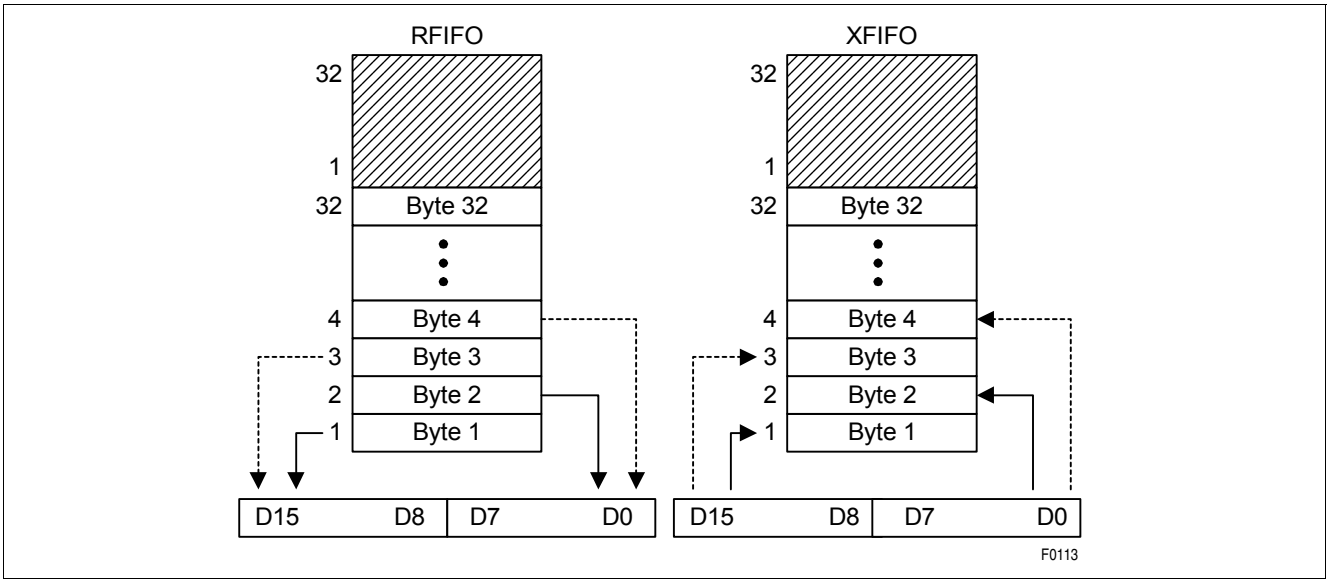


Figure 16 FIFO Word Access in Motorola Mode (shown for 64 byte depth)

3.4.4 Interrupt Interface

Special events in the OctalFALC™ are indicated by means of an interrupt output INT, which requests the external micro controller to read status information from the OctalFALC™, or to transfer data from/to the OctalFALC™. The electrical characteristics (open drain or push-pull) is programmed defined by the register bits IPC.IC(1:0), see **IPC_E** or **IPC_T**.

In the OctalFALC™ compatibility mode both pseudo QuadFALC®s have single interrupt outputs (INT1 and INT2 respectively) with programmable characteristics (open drain or push-pull, defined by registers IPC).

Since only one INT request output is provided for the OctalFALC™ (or for each of the two pseudo QuadFALC®s), the cause of an interrupt must be determined by the external micro controller by reading the OctalFALC™'s interrupt status registers (GIS, ISR(7:0)). The interrupt on pin INT (or INT1, INT2 respectively) and the interrupt status bits are reset by reading the interrupt status registers. The registers ISR(7:0) are of type “clear on read“ (“rsc”).

The structure of the interrupt status registers is shown in **Figure 17** for the compatibility mode and in **Figure 18** for the generic mode.

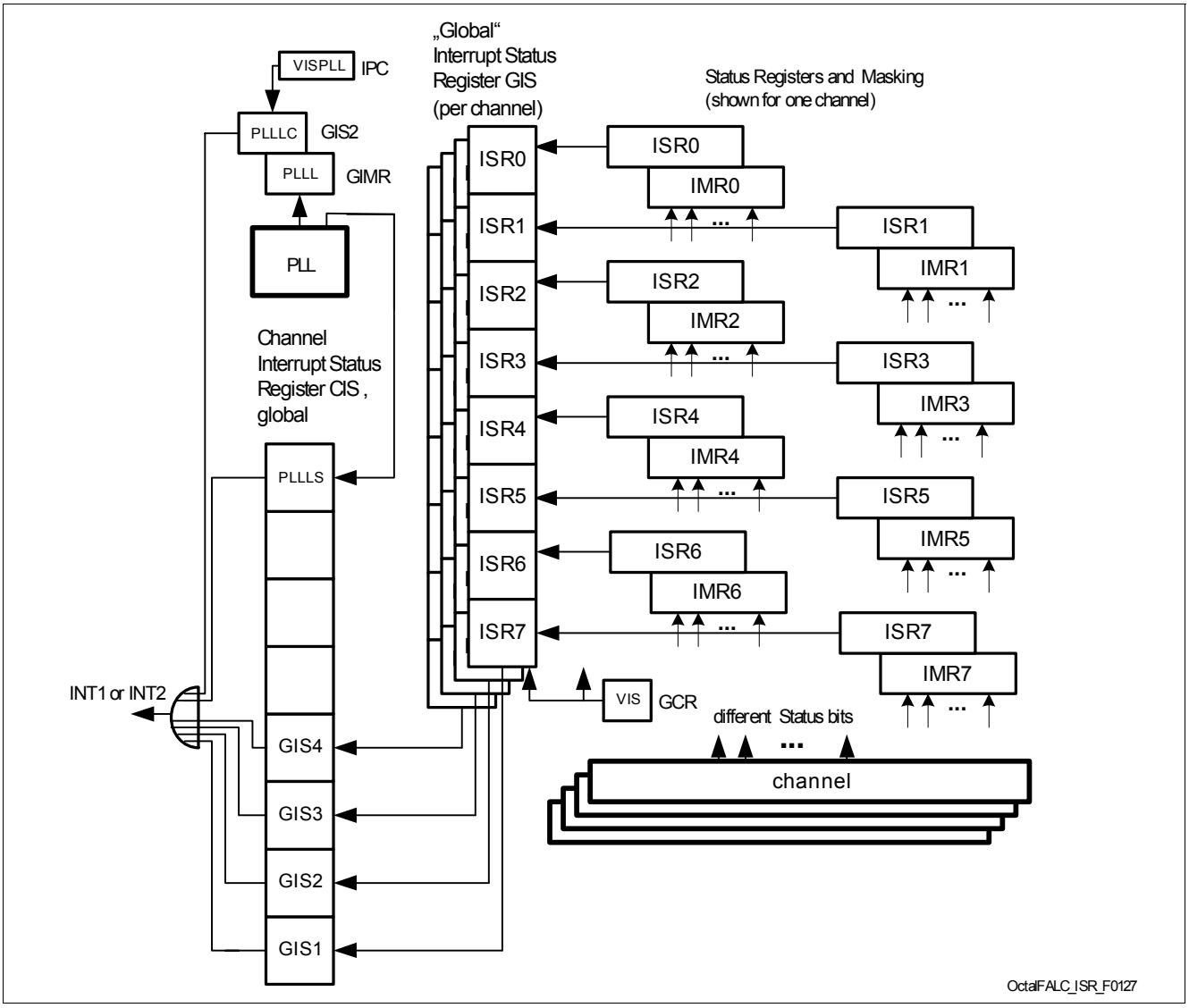


Figure 17 Interrupt Status Registers in Compatibility Mode (COMP = ´1´) for one pseudo QuadFALC®

Each interrupt indication bit of the registers ISR(7:0) can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR(7:0). If the interrupt status bits are masked they neither generate an interrupt at INT nor are they visible in ISR(7:0).

GIS, the non-maskable “Global” Interrupt Status Register per channel, serves as pointer to pending interrupts sourced by registers ISR(7:0).

The non-maskable Channel Interrupt Status Register CIS serves as channel pointer to pending interrupts sourced by registers GIS.

After the OctalFALC™ has requested an interrupt by activating its INT pin, the external micro controller should first read the register CIS to identify the requesting interrupt source channel. Then it should read the Global Interrupt Status register GIS to identify the requesting interrupt source register ISR(7:0) of that channel.

After reading the assigned interrupt status registers ISR(7:0), the pointer bit in register GIS is cleared or updated if another interrupt requires service. After all bits ISR(7:0) of a register GIS are cleared, the assigned bit in register CIS is cleared. After all bits in register CIS are cleared the INT pin will be deactivated.

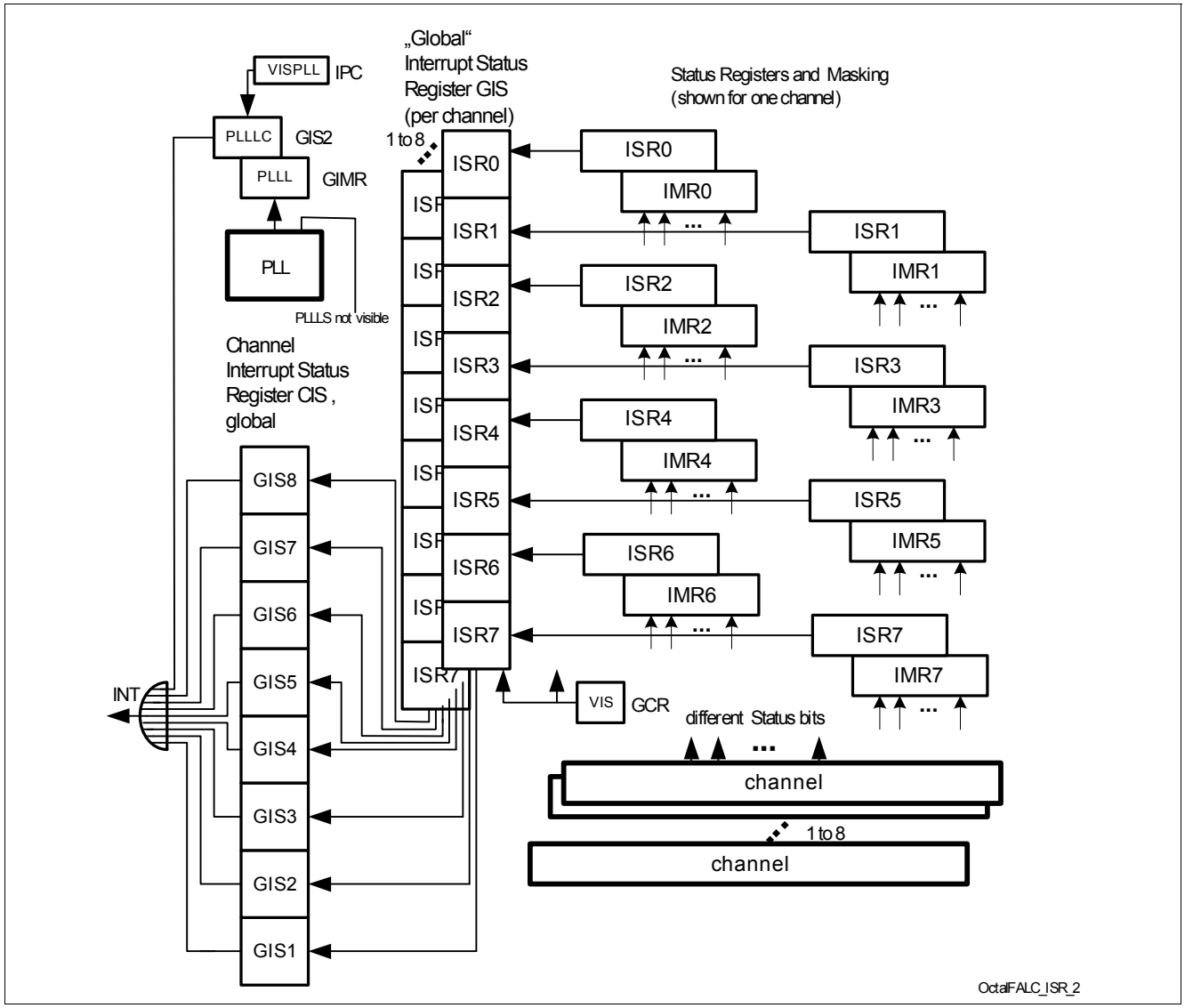


Figure 18 Interrupt Status Registers for COMP = ´0´

If **all** pending interrupts are acknowledged by reading (GIS is reset), pin INT goes inactive.

Updating of interrupt status registers ISR(7:0) and GIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

- The “Global” Interrupt Status register (GIS) indicates those interrupt status registers with active interrupt indications (bits GIS.ISR(7:0)).
- An additional interrupt mode can be selected per port via bit GCR.VIS (**GCR_E**, **GCR_T**), see **Table 11**. In this mode, masked interrupt status bits neither generate an interrupt on pin INT nor are they visible in GIS, **but are displayed in the corresponding interrupt status register(s) ISR(7:0)**. In compatibility mode both of the pseudo QuadFALC®‘s have its own bit GCR.VIS.

PLL Interrupt Status Register

- In compatibility mode, the PLL status is indicated by bit 7 of the register CIS as bit PLLLS in both of the pseudo QuadFALC®s. (So both INT1 and INT2 will be set if PLLS is set. The status of the one PLL is duplicated in each of the pseudo QuadFALC®s.)
- In generic mode the bit 7 of the register CIS indicates a pending interrupt on channel 8 so that the PLL status PLLLS is not visible here but in register GIS2.

- The Global Interrupt Status register GIS2 indicates the lock status of the (global) PLL. Masking can be done by the register GIMR. In compatibility mode both of the pseudo QuadFALC®'s have their own registers GIS2 and GIMR.
- An additional interrupt mode can be selected per port via bit IPC.VISPLL (**IPC_E**) where the masked interrupt status bit GIS2.PLLLS does not generate an interrupt on pin INT, **but is displayed in the corresponding interrupt status register bit GIS2.PLLLC**, see **Table 11**. In compatibility mode each of the pseudo QuadFALC®'s have its own bit IPC.VISPLL.

The additional interrupt mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Table 11 Interrupt Modes

GCR.VIS; IPC.VISPLL	Appropriate Mask bit	Interrupt active	Visibility in ISR(7:0) ; GIS2
0	0	Yes	Yes
0	1	No	No
1	0	Yes	Yes
1	1	No	Yes

Notes:

1. *In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.*
2. *The behaviour of all unmasked interrupts does not change in visible mode.*

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no "hierarchical" polling possible), since GIS only contains information on actually generated, i.e. unmasked interrupts.

3.4.5 Boundary Scan Interface

In the OctalFALC™ a **T**est **A**ccess **P**ort (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard IEEE 1149.1-2001. **Figure 19** gives an overview, **Figure 99** shows the timing diagram and **Table 141** gives the appropriate values of the timing parameters.

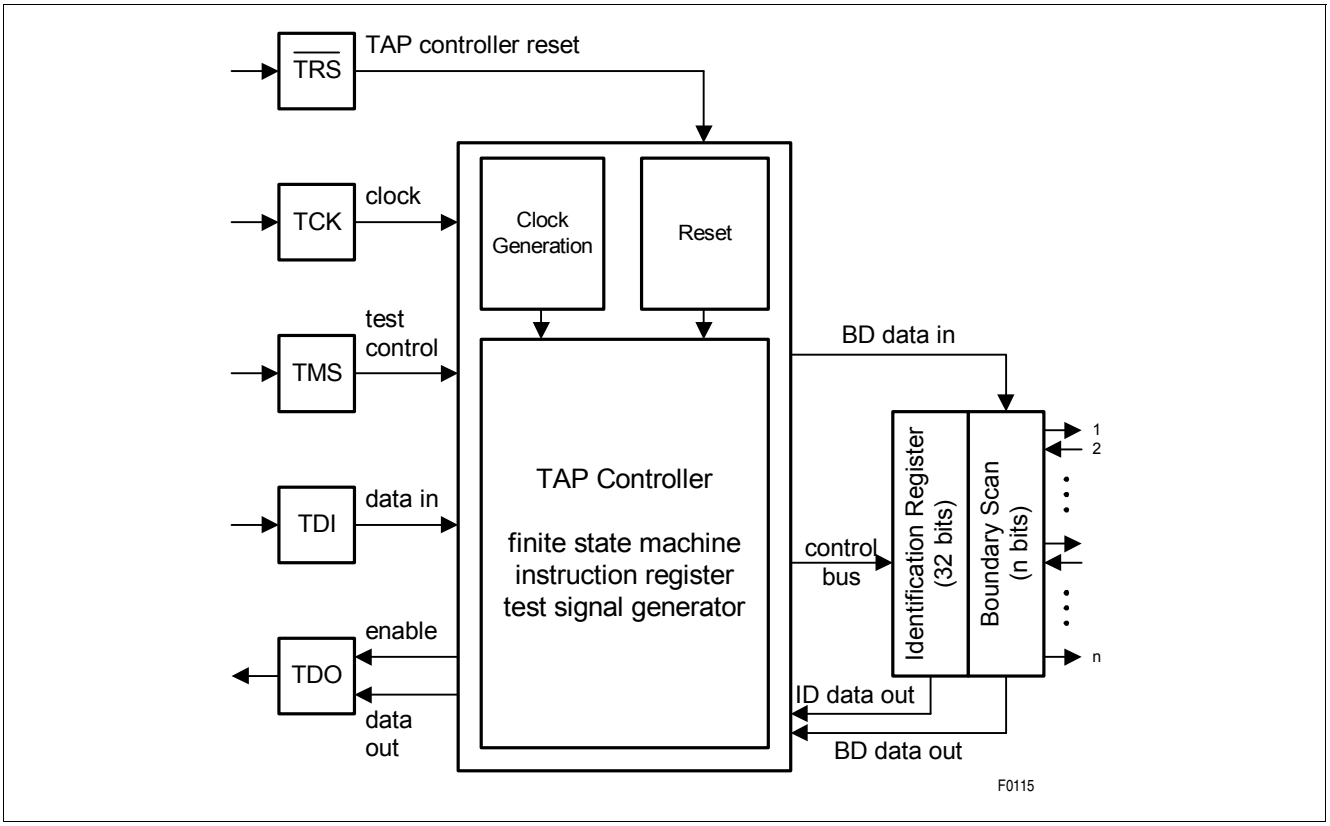


Figure 19 Block Diagram of Test Access Port and Boundary Scan

After switching on the device (power-on), a reset signal has to be applied to $\overline{TRS}$, which forces the TAP controller into test logic reset state.

For normal operation without boundary scan access, the boundary reset pin $\overline{TRS}$ can be tied to the device reset pin $\overline{RES}$.

If no boundary scan operation is used, $\overline{TRS}$ has to be connected to $\overline{RST}$ or V_{SS}. TMS, TCK and TDI do not need to be connected since pullup transistors ensure high input levels in this case.

Test handling (boundary scan operation) is performed using the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, that means $\overline{TRS}$ is connected to V_{DD} or it remains unconnected due to its internal pull up. Test data at TDI is loaded with a clock signal connected to TCK. "1" or "0" on TMS causes a transition from one controller state to another; constant "1" on TMS leads to normal operation of the chip.

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out and enable) and an I/O-pin (I/O) uses three cells (data in, data out and enable). Note that most functional output and input pins of the OctalFALC™ are tested as I/O pins in boundary scan, hence using three cells.

The boundary scan length is 247.

The desired test mode is selected by serially loading a 8-bit instruction code into the instruction register through TDI (LSB first), see **Table 12**. The test modes are:

EXTEST

Extest is used to examine the interconnection of the devices on the board. In this test mode at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values ("0" or "1"). Then the contents of the boundary scan is shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

SAMPLE

Is a test mode which provides a snapshot of pin levels during normal operation.

IDCODE

A 32-bit identification register is serially read out on pin TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

The ID code field is set to (MSB to LSB): ´0001 0000 0000 1101 1110 0000 1000 0011_B´.

Version number (first 4 bits) = ´0001_B´

Part Number (next 16 bits) = ´0000000011011110_B´

Manufacturer ID (next 11 bits) = 00001000001_B´

LSB fixed to ´1´.

BYPASS

A bit entering TDI is shifted to TDO after one TCK clock cycle.

An alphabetical overview of all TAP controller operation codes is given in **Table 12**.

Table 12 TAP Controller Instruction Codes

TAP Instruction	Instruction Code
BYPASS	11111111
EXTEST	00000000
IDCODE	00000100
SAMPLE	00000001
Reserved for device test	01010011

3.4.6 Master Clocking Unit

The OctalFALC™ provides a flexible clocking unit, which references to any clock in the range of 1.02 to 20 MHz supplied on pin MCLK, see **Figure 20**.

The clocking unit has two different modes:

- In the “flexible master clocking mode” (GCM2.VFREQ_EN = ´1´, **GCM2_E**) the clocking unit has to be tuned to the selected reference frequency by setting the global clock mode registers GCM(8:1) accordingly, see formulas in **GCM6_E** or **GCM6_T** respectively. All eight ports can work in E1 or T1 mode individually. After reset the clocking unit is in “flexible master clocking mode”.
- In the “clocking fixed mode” (GCM2.VFREQ_EN = ´0´) the tuning of the clocking unit is done internally so that no setting of the global clock mode registers GCM(8:1) is necessary. All eight ports must work together either in E1 or in T1 mode.

For the calculation for the appropriate register settings see **Chapter 13.3**. Calculation can be performed by using the flexible Master Clock Calculator which is part of the software support of the OctalFALC™.

All required clocks for E1 or T1/J1 operation are generated by the device internally. The global setting depends only on the selected master clock frequency and is the same for E1 and T1/J1 because both clock rates are provided simultaneously.

To meet the E1 requirements the MCLK reference clock must have an accuracy of better than ± 32 ppm. The synthesized clock can be controlled on pins RCLK, SCLKR and XCLK.

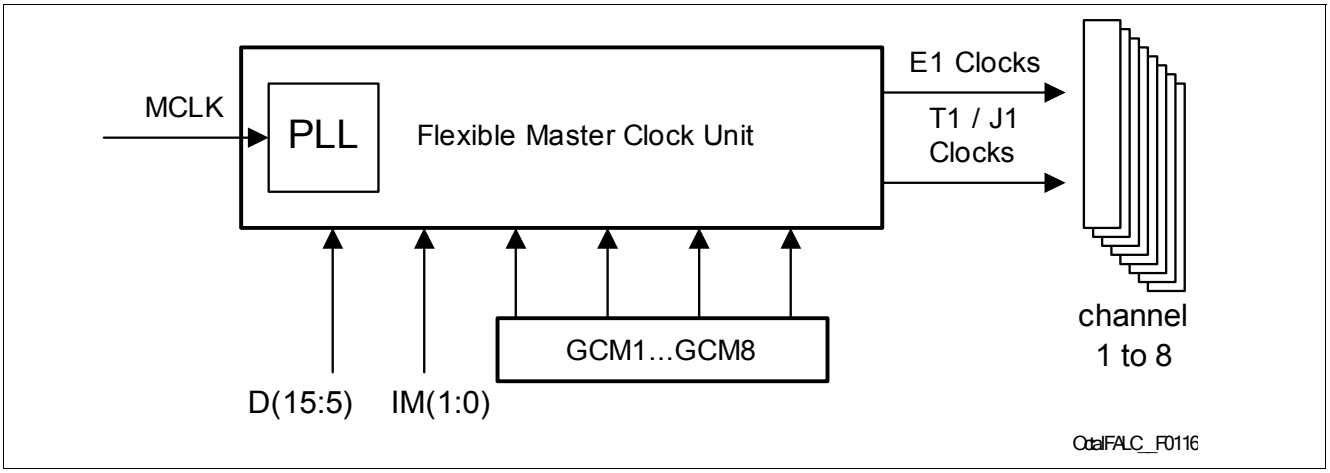


Figure 20 Flexible Master Clock Unit

3.4.6.1 PLL (Reset and Configuring)

If the (asynchronous) microcontroller interface mode is selected by IM(1:0) the PLL must be configured either

- By programming of the registers GCM5 and GCM6 in “flexible master clocking mode”. Every change of the contents of these registers - the divider factors N and M of the PLL - causes a reset of the PLL. Switching between E1 and T1 modes in arbitrary channels causes a reset of the clock unit but not of the PLL itself.
- Or by enabling of the ” fixed mode”: GCM2.VFREQ_EN = ´0´ (**GCM2_E**). Programming of registers GCM5 and GCM6 is not necessary. Any programming of GCM5 and GCM6 does NOT cause a reset of the PLL. Switching between E1 and T1 modes (for all channels) causes a reset of the clock unit but not of the PLL itself.

The SPI and SCI are synchronous interfaces and therefore need defined clocks immediately after reset, before any device configuration is done. To enable access to serial interfaces, the clock MCLK must be active and must have a defined frequency before reset becomes inactive. Depending on the supplied MCLK frequency the internal PLL must be configured if the SCI- or SPI-Interface mode is selected by IM(1:0). This can be performed either

- By strapping of the pins D(15:5) if “flexible master clocking mode” is enabled (GCM2.VFREQ_EN = ´1´), see also **Table 2**. Because the “flexible master clocking mode” is enabled after reset, pinstrapping at D(15:5) is always necessary! Every status change of the signals at these pins causes a reset of the PLL. Configuring by the registers GCM5 and GCM6 has no effect and does not cause a reset of the main PLL
- Or by usage of the ”clocking fixed mode” (GCM2.VFREQ_EN = ´0´). This is only allowed if the values of N and M defined by pinstrapping are identical to that values which are internally used for the “clocking fixed mode”. This avoids changing of N and M by switching into the ”clocking fixed mode” and therefore a new reset of the PLL. (A reset of the PLL can cause a reset of the hole transceiver! Clock and data processing will be interrupted.) The used values of N and M in “clocking fixed mode” are: N = ´33_{10}´, M = ´0_{10}´. This requires the pinstrapping configuration to be: D(10:5) = ´HLLLLH´, D(15:11) = ´LLLLL´. In ”clocking fixed mode” further programming of the registers GCM1 to GCM8 is no longer necessary. The pinstrapping configuration at the pins D(15:5) do not have any effect. Changing of these values does NOT cause a reset of the PLL. Switching between E1 and T1 modes causes a reset of the clock unit but not of the main PLL itself.

The configuration of the PLL by pinstrapping (see **Table 2**) in case of serial interface modes is done in the same way as by using the registers GCM5 and GCM6 if asynchronous micro controller interface mode (Intel or Motorola) is selected. Calculation of the values to be configured by pinstrapping can be done also by using the formulas described for the registers **GCM6_E** or **GCM6_T** respectively or by using the “flexible Master Clock Calculator” which is part of the software support of the OctalFALC™, see **Chapter 13.3**. If the serial interfaces are selected, pinstrapping of D(15:5) configures the PLL directly, so changes causes a direct reset of the PLL.

The conditions to trigger a reset of the central clock PLL are listed in **Table 13**. Every reset of the PLL causes a reset of the clock system.

Table 13 Conditions for a PLL Reset

Reset Pin	GCM2.VFREQ_EN	Used controller interface	a PLL reset is made if ...
Active	X (will be set to ´1´ by reset)	X	Always
Inactive	1	Asynchron (Motorola or Intel)	If GCM5 or GCM6 are written and their values N or M change
		SPI or SCI	If pinstrapping values change
	0	Asynchron (Motorola or Intel)	Never
		SPI or SCI	If pinstrapping values change
	0 -> 1 or 1 -> 0	Asynchron (Motorola or Intel)	If actual values of N or M in GCM5 or GCM6 are different to internal settings of the “clocking fixed mode”
		SPI or SCI	If pinstrap values are different to internal settings of the “clocking fixed mode”; That is not allowed!

3.5 Line Coding

The OctalFALC™ supports both optical and analog ternary/digital dual rail input/output network signals.

Supported for the optical interface (separate clock and data lines) are:

- In E1 mode NRZ and CMI (Code Mark Inversion or known as 1T2B)
- In T1/J1 mode NRZ.

Supported for the analog ternary or digital dual rail interface (clock is embedded in data) are

- In E1 mode Alternate Mark Inversion (AMI) and High Density Bipolar of order 3 (HDB3)
- In T1/J1 mode AMI and Bipolar with 8 Zero Substitution (B8ZS).

An overview of the line coding is given in **Table 14**.

The receiver and transmitter can be programmed with different line coding, although they are generally programmed the same.

Table 14 Summary of Line Coding

Line Interface	LIM1.DRS	E1 Coding		FMR3.CMI	T1 Coding	FMR0.RC (1:0)	FMR0.XC (1:0)
		RX	TX				
Optical NRZ	X	NRZ		X	NRZ	00	00
Optical CMI, single line	X	1T2B/HDB3	1T2B/HDB3	0	Unassigned T1	01	01
			1T2B	1			
Ternary	0	AMI		X	AMI/ B7ZCS clear channel	10	10
Dual Rail	1						
Ternary	0	AMI/HDB3		X	AMI/B8ZS	11	11
Dual Rail	1						

In T1/J1 an alternative scheme is called bit 7 zero code substitution (B7ZCS). If a DS0 channel contains 8 zeros (´00_H´), then the code ´02_H´ is substitude into the data stream to assure the minimum „1“s density. At the receiving end it is not possible to distinguish whether the received byte is actually ´02_H´ or substituded for ´00_H´. Therefore, data can be corrupted at the transmission end by virtue of this substitution technique. B7ZCS is not suitable for data transmission applications.

The function of B7ZCS in the transmit direction can be selectively defeated on a channel by channel basis by using the OctalFALC™´s clear channel capability. Registers CCB(3:1) are used to disable B7ZCS and insertion of robbed bit signaling.

3.6 Receive Path

An overview about the receive path of one channel of the OctalFALC™ is given in **Figure 21**.

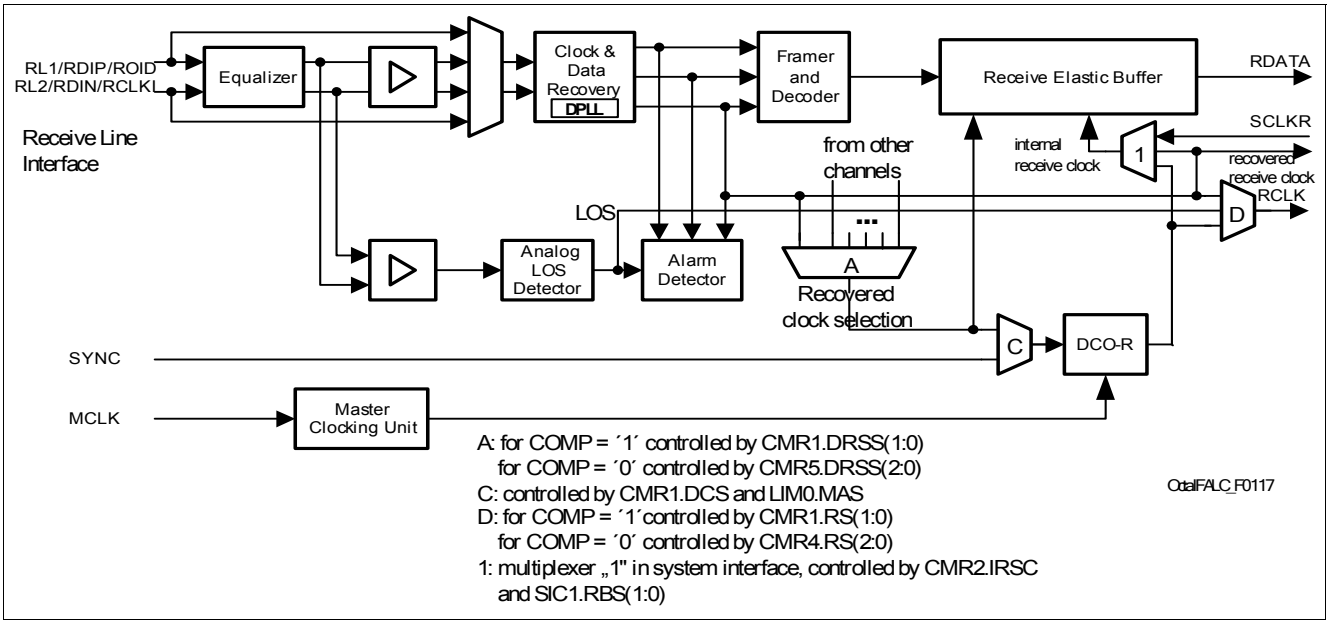


Figure 21 Receive System of one channel

The recovered clock selection of **Figure 21** (multiplexer “A”) is shown in more detail for compatibility mode in **Figure 22** and for generic mode in **Figure 23**.

The multiplexer “C” in **Figure 21** selects the mode of the receive jitter attenuator, see chapter **Chapter 3.6.5**.

The multiplexer “D” in **Figure 21** selects if the receive clock RCLK of a channel is sourced by the recovered route clock or by the DCO-R (see above). The appropriate register bits are CMR1.RS(1:0) (**CMR1_E**) in compatibility mode or CMR4.RS(2:0) (**CMR4_E**) in generic mode. These register bits also select different DCO-R output frequencies.

The sources of the receive clock output pins (RCLK(8:1)), configured by the multi function ports, can be selected out of the receive clocks of the channels:

For COMP = ´0´ the source of each of the eight receive clock pins (RCLK(8:1)) can be independently selected out of each of the eight receive clocks of the channels by programming the registers bits GPC(2:6).RS(2:0) (**GPC2_E**), see cross connection “B” in **Figure 23**. For COMP = ´0´ the register bits GPC1.RS(1:0) are not valid for selection of the receive clock, see also **Table 62**.

For COMP = ´1´ the source of the RCLK1 pin can only be selected by the register GPC1 (**GPC1_E**) of the pseudo QuadFALC®1, see multiplexer “B” in **Figure 22**. The sources of the pins RCLK2,3,4 are the appropriate channel receive clocks. Similarly, the RCLK5 pin source can be selected by the register GPC1 of the pseudo QuadFALC®2 and the sources of the pins RCLK6,7,8 are the appropriate channel receive clocks. After reset pin RCLK1 is sourced by the receive clock of channel 1 and pin RCLK5 is sourced by the receive clock of channel 5 and they are switched to the multi function ports RPC. The registers GPC2 to GPC6 are not valid if COMP = ´1´.

Note that in channel translation (CT) mode the DCO-R is always on.

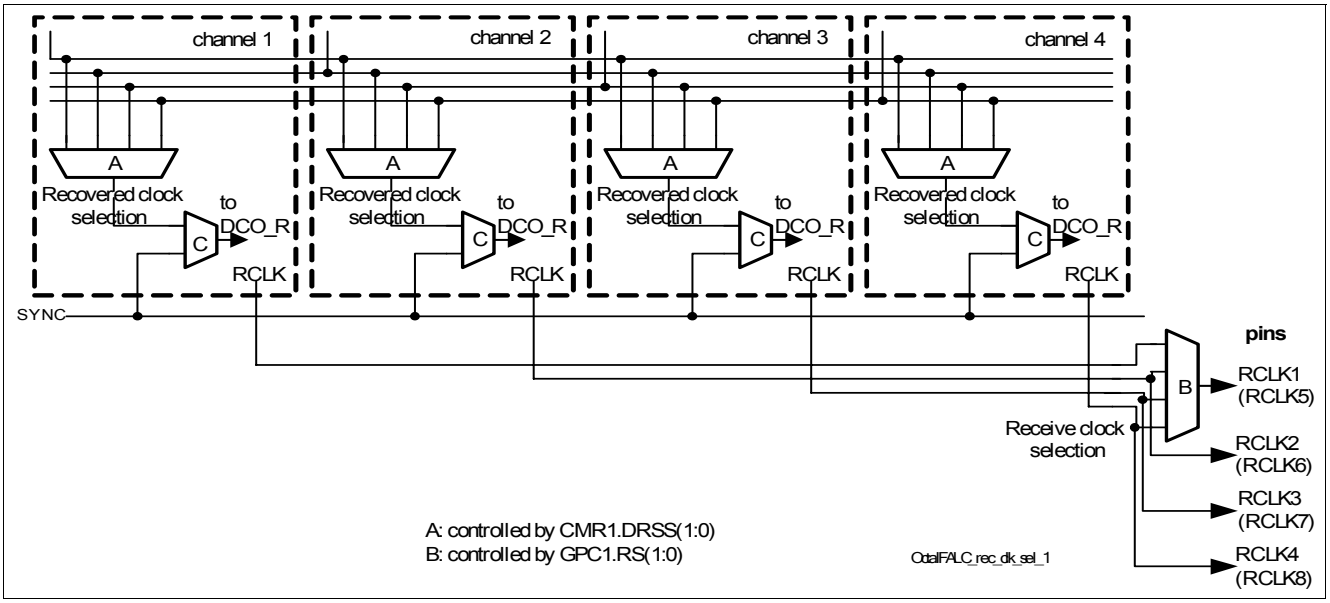


Figure 22 Recovered and Receive Clock Selection of a pseudo QuadFALC® in compatibility mode

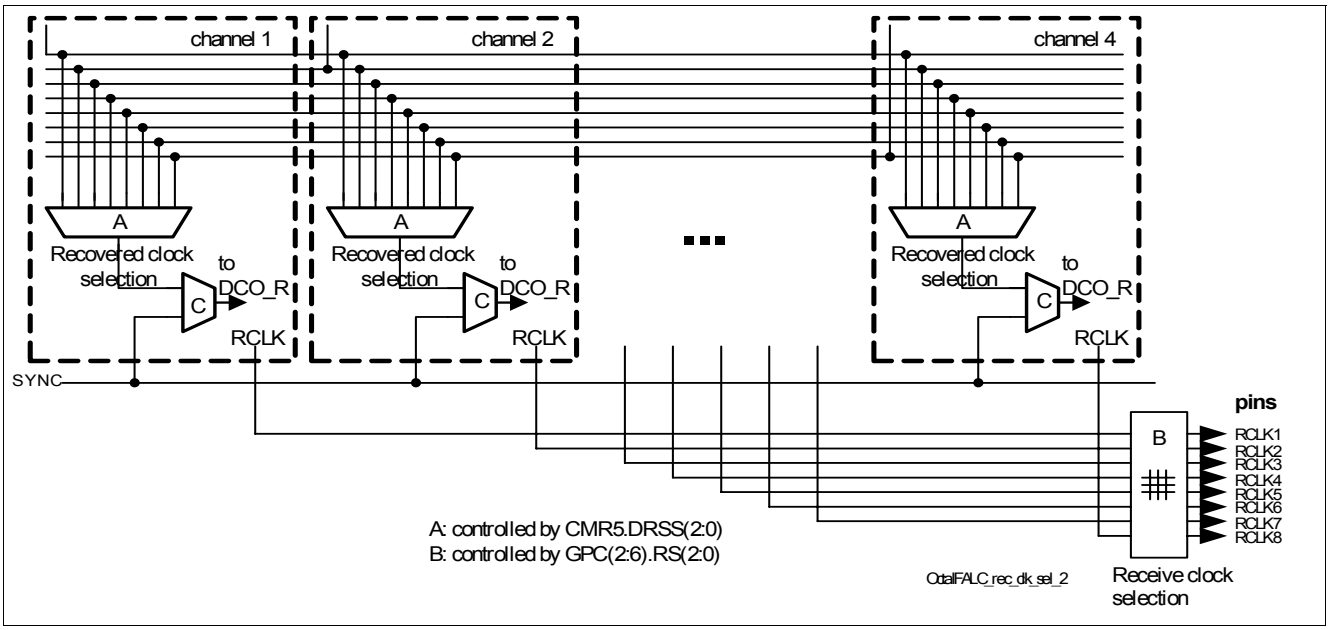


Figure 23 Recovered and Receive Clock Selection of a OctalFALC™ in Generic Mode

3.6.1 Receive Line Interface

For data input, three different data types are supported:

- Ternary coded signals received at pins RL1 and RL2 from 0 dB down to -43 dB for E1 if the Infineon software package is used (see **Chapter 13.3**) or downto -36 dB for T1/J1 ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Digital dual-rail signals received on pins RDIP and RDIN. The dual-rail interface is selected if LIM1.DRS and FMR0.RC1 is set.
- Unipolar data on pin ROID received from a fiber-optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1 is reset.

An overview about the line coding is given in **Table 14**.

3.6.2 Receive Equalization Network

The OctalFALC™ automatically recovers the signals received on pins RL1 and RL2 in a range of up to -43 dB for E1 if the Infineon software package is used (see **Chapter 13.3**) or -36 dB for T1/J1. The maximum reachable length with a 22 AWG twisted pair cable is about 1500 m for E1 and about 2000m (~6560 ft.) for T1. The integrated receive equalization network recovers signals with up to -43 dB for E1 or -36 dB for T1/J1 of cable attenuation automatically. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak-detected and sliced to produce the digital data stream. The slicing level is software selectable in four steps (45%, 50%, 55%, 67%), see **Table 139**. For typical E1 applications, a level of 50% is used. The received data is then forwarded to the clock & data recovery unit.

For non standard applications individual coefficients for the receive equalizer can be programmed into the RAM of the OctalFALC™.

3.6.3 Receive Line Attenuation Indication

Status register RES reports the current receive line attenuation

- For E1 in a range from 0 to -43 dB in 25 steps of approximately 1.7 dB each.
- For T1/J1 in a range from 0 to -36 dB in 25 steps of approximately 1.4 dB each.

The least significant 5-bits of this register indicate the cable attenuation in dB. These 5-bits are only valid in combination with the most significant two bits (RES.EV(1:0) = ´01_b´).

3.6.4 Receive Clock and Data Recovery

The analog received signal on pins RL1 and RL2 is equalized and then peak-detected to produce a digital signal. The digital received signal on pins RDIP and RDIN is directly forwarded to the clock & data recovery. The DPLL (digital PLL) of the receive clock & data recovery circuit extracts the route clock from the data stream received at the RL1/2, RDIP/RDIN or ROID lines. The clock & data recovery circuit converts the data stream into a dual-rail, unipolar bit stream. The clock and data recovery circuit uses an internally generated high frequency clock out of the master clocking unit based on MCLK.

The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI. In digital bipolar line interface mode the clock and data recovery requires HDB3 coded signals with 50% duty cycle.

3.6.5 Receive Jitter Attenuator

The receive jitter attenuator is based on the DCO-R (digital clock oscillator, receive) in the receive path. Jitter attenuation of the received data is done in the receive elastic buffer. The working clock is an internally generated high frequency clock based on the clock provided on pin MCLK. The jitter attenuator meets the E1 requirements of ITU-T I.431, G. 736 to 739, G.823 and ETSI TBR12/13 and the T1 requirements of AT&T PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824.

The internal PLL circuitry DCO-R generates a "jitter-free" output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock. The receive jitter attenuator can be synchronized either on the extracted receive clock RCLK or on a 2.048 MHz/8 kHz or 1.544 MHz/8 kHz clock provided on pin SYNC (8 kHz in master mode only). The jitter attenuated DCO-R output clock can be output on pin RCLK. Optionally an 8 kHz clock is provided on pin SEC/FSC.

For jitter attenuation the received data is written into the receive elastic buffer with the recovered clock sourced by the clock & data recovery and are read out with the de-jittered clock sourced by DCO-R.

If the receive elastic buffer is read out directly with the recovered receive clock, no jitter attenuation is performed.

If the receive elastic buffer is read out with the receive system clock SCLKR of the system interface, the receive elastic buffer performs a clock adoption from the recovered receive clock to SCLKR.

The DCO-R circuitry attenuates the incoming jittered clock starting at its corner frequency with 20 dB per decade fall-off. Wander with a jitter frequency below the corner frequency is passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02 UI.

The corner frequency of the DCO-R can be configured in a wide range, see **Table 15** and **Figure 24**. The jitter attenuator PLL in the transmit path, the DCO-X, is equivalent to the DCO-R so that the principle for its configuration is the same.

Table 15 Overview DCO-R (DCO-X) programming

CMR6.DCOCOMPN	CMR2.ECFAR (CMR2.ECFAX)	LIM2.SCF (CMR6.SCFX)	CMR3.CFAR(3:0) (CMR3.CFAX(3:0))	CMR4.IAR(3:0) (CMR5.IAX(4:0))	Corner-frequencies of DCO-R (DCO-X) E1 / T1
X	0	0	Not used	Not used	2 Hz / 6 Hz
X	0	1	Not used	Not used	0.2 Hz / 0.6 Hz
0	1	X	QuadFALC® compatible programming: ´7_H´ ´4_H´	Not used	 0.2 Hz / 0.6 Hz 2 Hz / 6 Hz
1	1	X	´0_H´ ...´F_H´ , used as proportional parameter ´9_H´ ´8_H´ ´6_H´ ´4_H´	´00_H´ ...´$1F_H$´ used as integral parameter ´19_H´ ´13_H´ ´12_H´ ´$0F_H$´	Range 0.2 Hz ... 20 Hz 0.2 Hz 0.6 Hz 2 Hz 6Hz

After reset the corner frequencies are 2 Hz in E1 and 6 Hz in T1/J1 mode and can be switched to 0.2 Hz in E1 mode or 0.6 Hz in T1 mode by setting the register bit LIM2.SCF for the DCO-R or the register bit CMR5.SCFX for the DCO-X respectively. A logical table builds the integral (I) and proportional (P) parameter for the PI filter of the DCO-R or DCO-X, see **Figure 24**.

If QuadFALC® compatible programming is enabled by setting the register bits CMR2.ECFAR or CMR2.ECFAX for the DCO-R or the DCO-X respectively, the corner frequencies can be configured in a range between 2 Hz and 0.2 Hz using the register bits CMR3.CFAR(3:0) or CMR3.CFAX(3:0) respectively, see **CMR3_E**, **CMR4_E** and **CMR5_E**. A logical table builds the integral and proportional parameter for the PI filter of the DCO-R or DCO-X out of the settings in CMR3.CFAR(3:0) or CMR3.CFAX(3:0) respectively.

If additionally to CMR2.ECFAR or CMR2.ECFAX the bit CMR6.DCOCOMPN (**CMR6_E**) is set, which is valid for the DCO-R and the DCO-X, the corner frequencies and attenuation factors can be programmed in a wide range using the register bits CMR3.CFAR(3:0) and CMR4.IAR(4:0) for the DCO-R and CMR3.CFAX(3:0) and CMR5.IAX(4:0) for the DCO-X. The settings in CMR3.CFAR(3:0)/CFAX(3:0) build the proportional parameter, the settings in CMR4.IAR(4:0) and CMR5.IAX(4:0) build the integral parameter for the PI filters, independent from another.

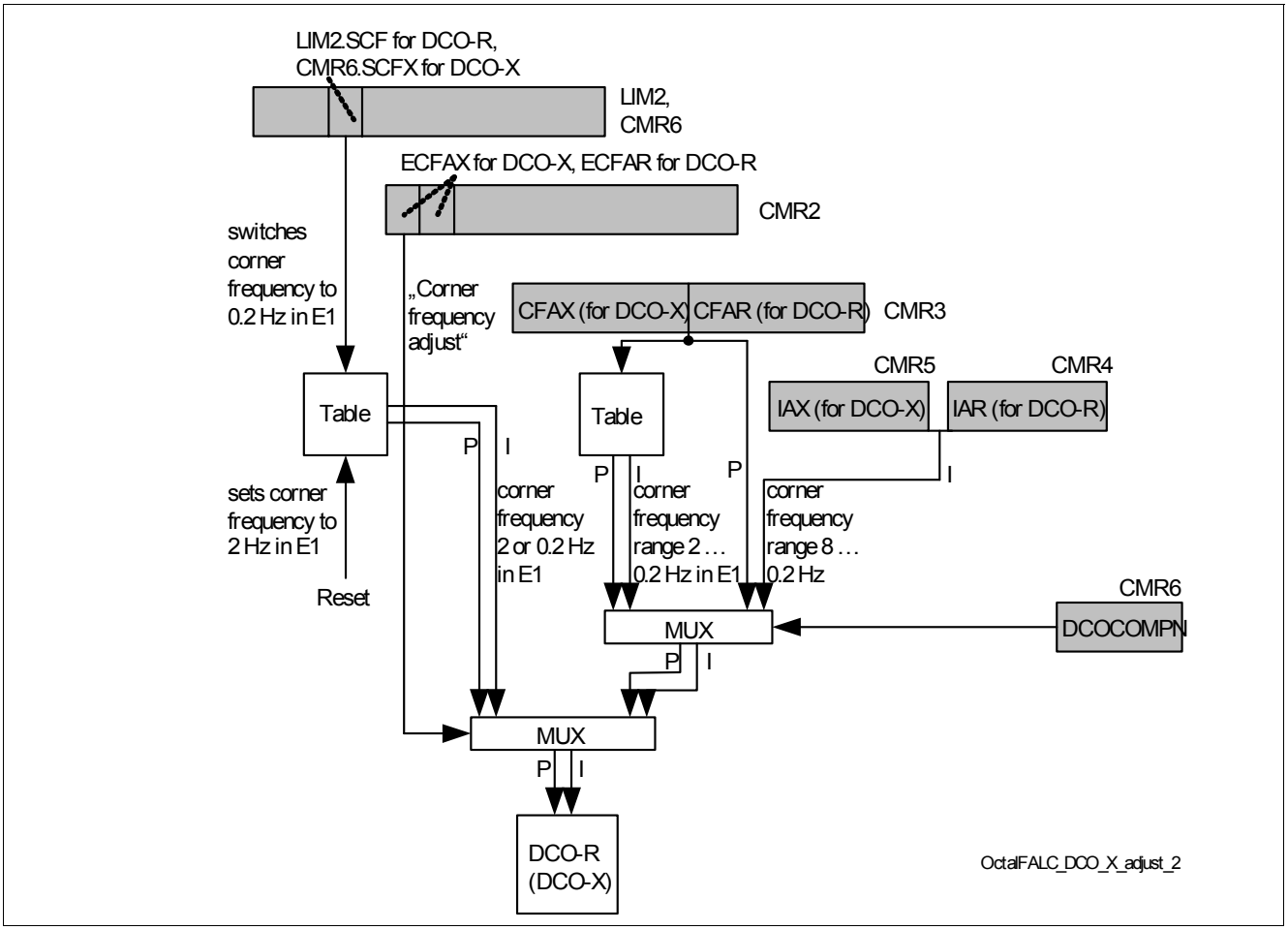


Figure 24 Principle of Configuring the DCO-R and DCO-X Corner Frequencies

The DCO-R reference clock is watched: If one, two or three clock periods of the 2.048 MHz (1.544 MHz in T1/J1 mode) clock at pin SYNC or RCLKI (in single rail digital line interface mode) are missing the DCO-R regulates it´s output frequency. If four or more clock periods are missing

- The DCO-R circuitry is automatically centered to the nominal bit rate if the center function of DCO-R is enabled by CMR2.DCF = ´0´.
- The actual DCO-R output frequency is “frozen” if the center function of DCO-R is disabled by CMR2.DCF = ´1´.

The receive jitter attenuator works in two different modes, selected by the multiplexer “C” in **Figure 21**:

- Slave mode: In slave mode (LIM0.MAS = ´0´) the DCO-R is synchronized on the recovered route clock. In case of loss of signal (LOS) the DCO-R switches automatically to Master mode. The frequency at the pin SYNC must be 2.048 MHz (1.544 MHz). If bit CMR1.DCS is set automatic switching from the recovered route clock to SYNC is disabled.
- Master mode: In master mode (LIM0.MAS = ´1´) the DCO-R is in free running mode if no clock is supplied on pin SYNC. If an external clock on the SYNC input is applied, the DCO-R synchronizes to this input. The external frequency can be 2.048 MHz (1.544 MHz) for IPC.SSYF = ´0´ or 8.0 kHz for IPC.SSYF = ´1´.

The following table **Table 16** shows this modes with the corresponding synchronization sources.

Table 16 Clocking Modes of DCO-R

Mode	Internal LOS Active	SYNC Input	System Clocks generated by DCO-R
Master	Independent	Fixed to V_{DD}	DCO-R centered, if CMR2.DCF = ´0´. (CMR2.DCF should not be set), see also **CMR2_E**
Master	Independent	2.048 MHz (E1) or 1.544 MHz (T1)	Synchronized to SYNC input (external 2.048 MHz or 1.544 MHz, IPC.SSYF = ´0´), see also **IPC_E**
Master	Independent	8.0 kHz	Synchronized to SYNC input (external 8.0 kHz, IPC.SSYF = ´1´, CMR2.DCF = ´0´)
Slave	No	Fixed to V_{DD}	Synchronized to recovered line clock
Slave	No	2.048 MHz (E1) or 1.544 MHz (T1)	Synchronized to recovered line clock
Slave	Yes	Fixed to V_{DD}	CMR1.DCS = ´0´: DCO-R is centered, if CMR2.DCF = ´0´. (CMR2.DCF should not be set)
			CMR1.DCS = ´1´: Synchronized on recovered line clock
Slave	Yes	2.048 MHz	CMR1.DCS = ´0´: Synchronized to SYNC input (external 2.048 MHz or 1.544 MHz)
			CMR1.DCS = ´1´: Synchronized on recovered line clock

The receive clock output RCLK of every channel can be switched between two sources, see multiplexer “D” in **Figure 21**:

- If the DCO-R is the source of RCLK the following frequencies are possible: 1.544, 3.088, 6.176, and 12.352 in T1/J1 mode and 2.048, 4.096, 8.192, and 16.384 MHz in E1 mode and in T1/J1 channel translation mode. If COMP = ´0´ controlling of the frequency is done by the register CMR4, bits RS(1:0), if COMP = ´1´ controlling is done by the register CMR1, bits RS(1:0).
- If the recovered clock out (of the clock and data recovery) is the source of RCLK (see multiplexer “D” in **Figure 21**), only 2.048 MHz (1.544 MHz) is possible as output frequency.

3.6.6 Receive Line Termination (Analog Switch)

In general the E1 line impedance operating modes with 75 Ω (used with coaxial cable) or with 120 Ω (used with twisted pair cable) line termination are selectable by switching resistors in parallel or using special transformers with different transfer ratios in one package (using center tap). These two options both provide only one analog front end circuitry for both transmission media types.

The OctalFALC™ supports a software selectable generic E1/T1/J1 solution without the need for external hardware changes by using the integrated analog switch and two external resistors for line impedance matching, see application example in **Figure 25**. By default the analog switch is off for QuadFALC® compatibility.

This allows, for example, to switch between 100 W (T1/E1 twisted pair) and 75 W (E1 coax) termination resistance using the external resistors R_{E1} = 100 Ω and R_{E2} = 300 Ω, see **Table 17**. The analog switch can be controlled by access to the register bit LIM0.RTRS (**LIM0_E**, **LIM0_T**) and by hardware using the receive Multi Function Ports. For that, only one (but not more) of the receive Multi Function Ports must be configured as Receive Line Termination (RLT) input. For controlling of the analog switch a logical equivalence is build out of RLT and the register bit LIM0.RTRS if RLT is configured at one multi function port.

If the analog switch is not used in an application, the pin RLS can be left open.

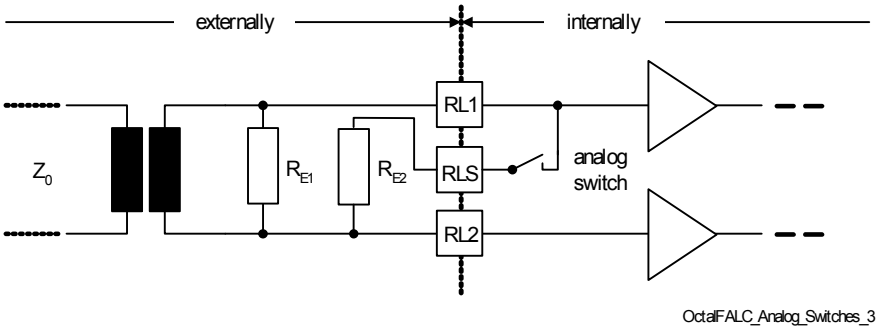


Figure 25 Receiver Configuration with Integrated Analog Switch for Receive Impedance Matching

Table 17 Receiver Configuration Examples

Line Impedance Z_0	External Resistor R_{E1}	External Resistor R_{E2}	Internal Analog Switch	LIM0.RTRS; RLT
120 Ω	*100* Ω (for common E1/T1/J1 applications)	300 Ω (for common E1/T1/J1 applications)	off	If RLT is configured: (LIM0.RTRS equivalent RLT) = ´0´ If RLT is not configured: LIM0.RTRS = ´0´
100 Ω			off	
75Ω			on	If RLT is configured: (LIM0.RTRS equivalent RLT) = ´1´ If RLT is not configured: LIM0.RTRS = ´1´

3.6.7 Receive Line Monitoring Mode

For short-haul applications like shown in **Figure 26**, the receive equalizer can be switched into receive line monitoring mode (LIM0.RLM = ´1´). One channel is used as a short-haul receiver while the other is used as a short-haul monitor. In this mode the receiver sensitivity is increased to detect an incoming signal of -20 dB resistive attenuation. The required resistor values are given in **Table 18**.

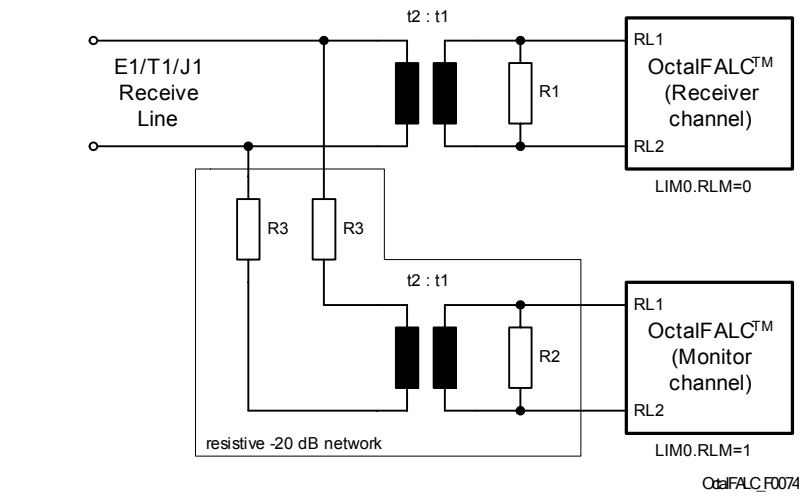


Figure 26 Receive Line Monitoring RLM (shown for one line)

Table 18 External Component Recommendations (Monitoring)

Parameter[1)]	Characteristic Impedance [Ω]		Characteristic Impedance [Ω]	
	E1		T1	J1
	75	**120**	**100**	**110**
R_1 (±1 %) [Ω]	75	120	100	110
R_2 (±1 %) [Ω]	75	120	100	110
R_3 (±1 %) [Ω]	330	510	430	470
$t_2 : t_1$	1 :1	1 :1	1 : 1	1 : 1

1) This includes all parasitic effects caused by circuit board design.

Using the receive line monitor mode and the hardware tristate function of transmit lines XL1/2 on the line side and the tristate functions on the system side, the OctalFALC™ supports applications connecting two channels to one receive and transmission line. In these kind of applications both channels are working in parallel for redundancy purpose (see **Figure 27**). While one of them is driving the line, the other one must be switched into transmit line tristate mode. If both channels are configured identically and supplied with the same system data and clocks, the transmit path can be switched from one channel to the other without causing a synchronization loss at the remote end.

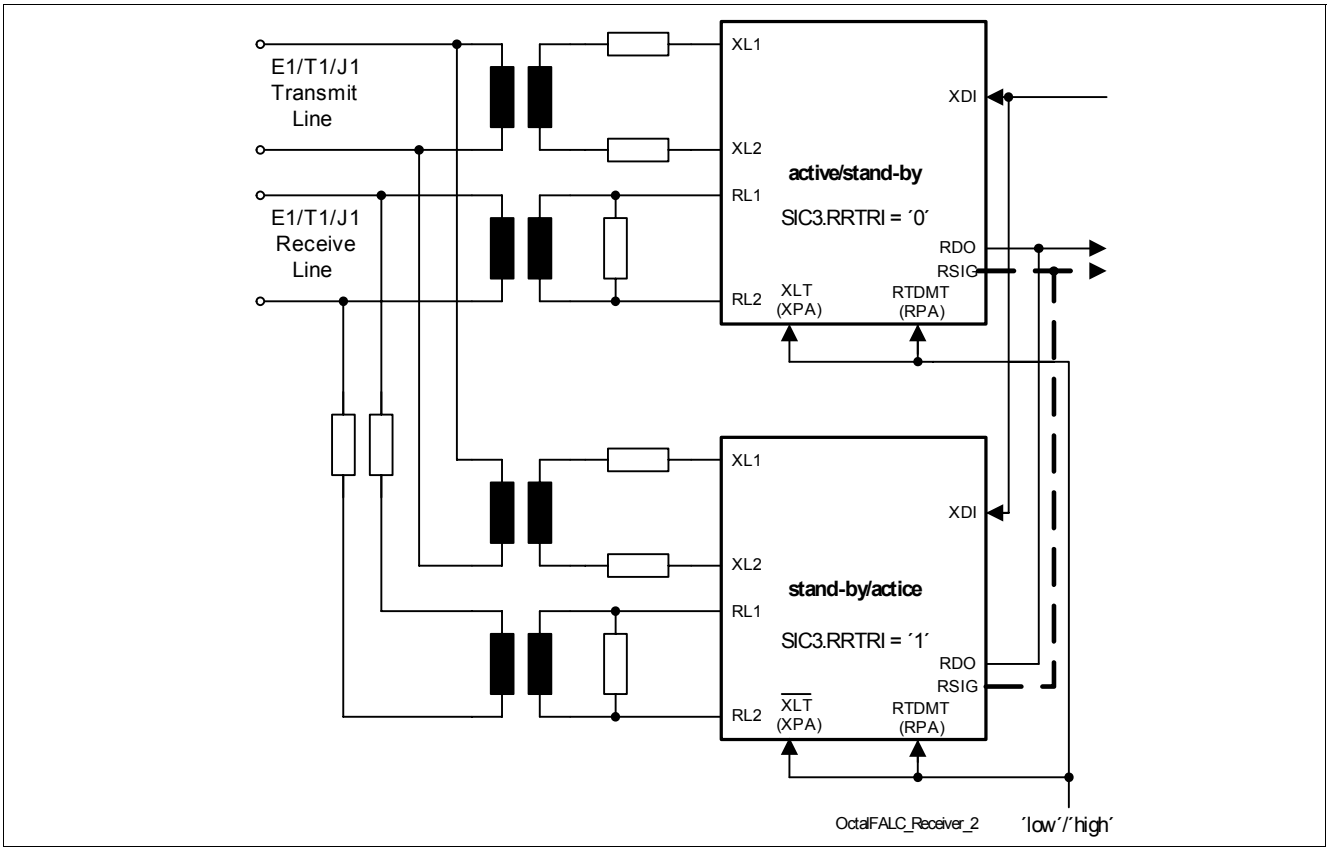


Figure 27 Redundancy Application using RLM (shown for one line)

RDO, RSIG, SCLKR and RFM can be set into tristate mode constantly for redundancy applications using the register bit SIC3.RRTRI (**SIC3_E**) and - if the RTDMT function is selected on one of the multi function port - by RTDMT, see **Chapter 3.8**. If the RTDMT function is selected the values of RTDMT and SIC3.RRTRI are logically exored. This enables an easy redundancy application using only one signal for switching between two devices. If the RTDMT function is not selected SIC3.RRTRI = ´1´ set the pins into tristate mode constantly. In this mode “tristate” means high impedance against V_{DD} and V_{SS}: No pull up or pull down resistor is active.

An overview about the tristate configurations of RDO, RSIG, SCLKR and RFM is given in Table 19.

Table 19 Tristate Configurations for the RDO, RSIG, SCLKR and RFM pins

SIC3.RRTRI / SIC3.RRTRI exor RTDMT if RTDMT is selected on multi function port	SIC3.RTRI	Pins RDO and RSIG	Pins SCLKR and RFM
1	X	Constant tristate (without pull up and pull down resistor)	Constant tristate (without pull up and pull down resistor)
0	0	Never tristate	Never tristate
0	1	Tristate during inactive channel phases (with pull up resistor	Never tristate

Switching between both channels can be done on the line side in transmit direction by a hardware signal if the multi function pin XPA is configured as tristate input XLT by the register bits PC1.XPC1 = ´1000_b´, see PC1_E. If one pin XPA is programmed as low active (PC1.XPC1 = ´1110_b´) and the one of the other channel as high active (PC1.XPC1 = ´1000_b´), no external inverter is necessary as shown in Figure 27. So switching between both channels on line side is possible using only one signal

Switching can also be done on the line side in transmit direction by software, if setting the register bit XPM2.XLT. The register bit value XPM2.XLT and the pin value of XPA are logically ored. (That means if XPA is configured as low active then

Tristate = XPM2.XLT or not($\overline{\text{XPA}}$).

Because the register bit XPM2.XLT and the multi function pin XPA exist individually for every channel, switching on the line side in transmit direction can be done between channels of different or of the same OctalFALC™ device

Switching between both channels can be done on the system side in receive direction by using the register bit SIC3.RRTRI and with or without selection of the multi function port as RTDMT. If the RTDMT function is selected, the values of RTDMT and SIC3.RRTRI are logically exored. If in one of the both channels SIC3.RRTRI is set, RTDMT is low active because of the logical exor, and if in the other channel SIC3.RRTRI is cleared, RTDMT is low active because of the logical exor. So switching between both channels on system side in receive direction is possible using only one board signal.

By using the XLT, $\overline{\text{XLT}}$ and RTDMT function of the multi function ports and do the appropriate programming of the bits SIC3.RRTRI (SIC3_E), switching between both channels can be done on the system and the line side together with only one common board signal, connected to XPA (XLT, $\overline{\text{XLT}}$) and RPA (RTDMT), as shown in Figure 27 and Table 20: If this signal has low level channel 1 is active and channel 2 is in stand-by, if it has high level channel 1 is in stand-by and channel 2 is active.

Table 20 Redundancy Application using RLM, switching with only one board signal

Configuration	Register Bits	Channel 1 (active/stand-by)	Channel 2 (stand-by/active)
XLT, $\overline{\text{XLT}}$	PC1.XPC1(3:0)	1000	1110
RTDMT	PC1.RPC1(3:0)	1101	1101
Receive system interface	SIC3.RRTRI	0	1
RLM mode	LIM0.RLM	0	1

Figure 28 shows a redundancy application for long haul mode using the internal analog switch. With the configuration shown in Table 21, switching between both channels is possible using only one board signal which is connected to XLT, $\overline{\text{XLT}}$, RLT and RTDMT. Because the OctalFALC™ builds the logical equivalence out of RLT and LIM0.RTRS, the analog switches of both channels are controlled by these signal.

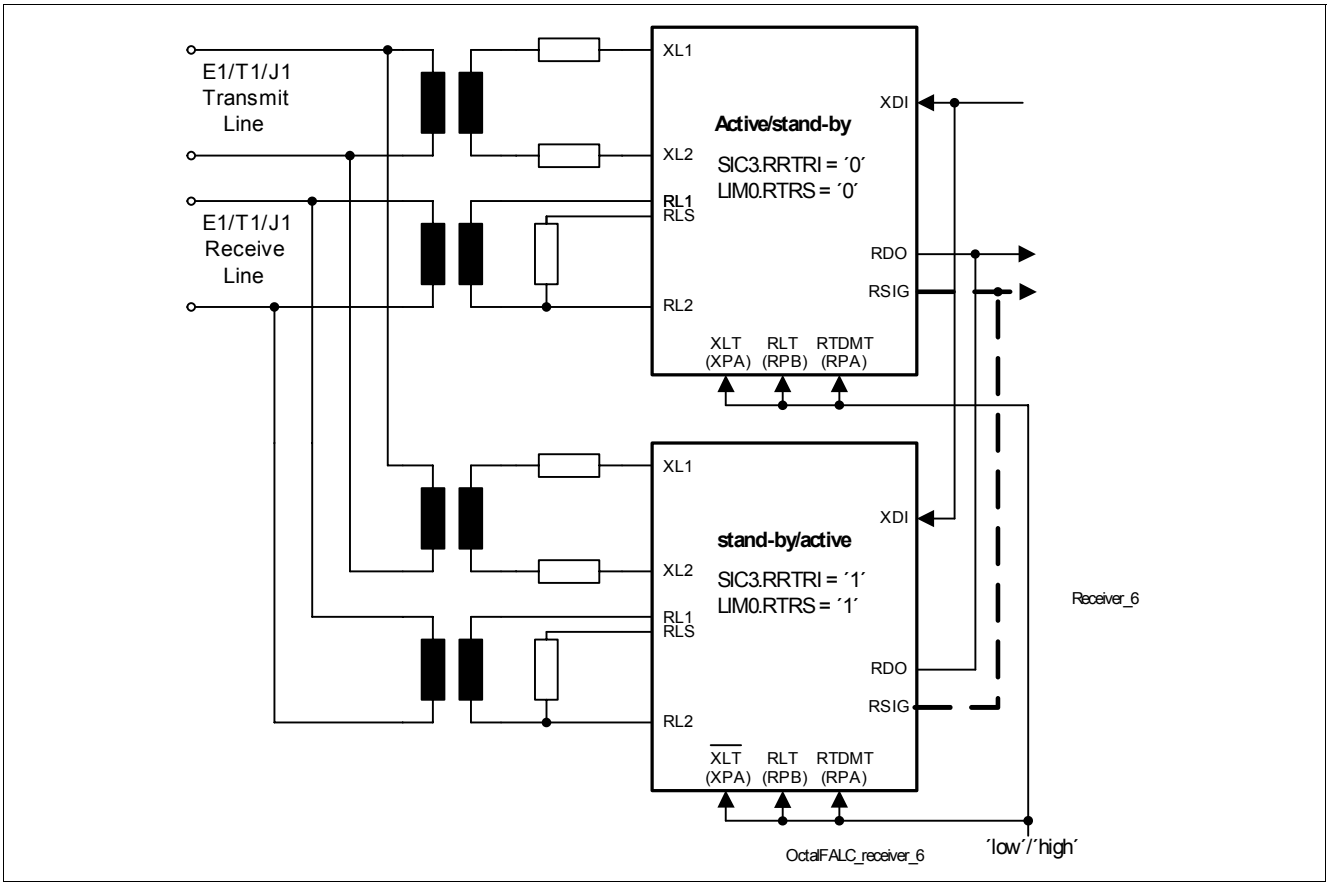


Figure 28 Long Haul Redundancy Application using the Analog Switch (shown for one line)

Table 21 Redundancy Application using the Analog Switch, switching with only one board signal

Configuration	Register Bits	Channel 1 (active/stand-by)	Channel 2 (stand-by/active)
XLT, $\overline{\text{XLT}}$	PC1.XPC1(3:0)	1000	1110
RTDMT	PC1.RPC1(3:0)	1101	1101
Receive system interface	SIC3.RRTRI	0	1
RLT	PC2.RPC2(3:0)	1000	1000
Receive line termination	LIM0.RTRS	0	1

3.7 Transmit Path

The transmit path of the OctalFALC™ is shown in **Figure 29**.

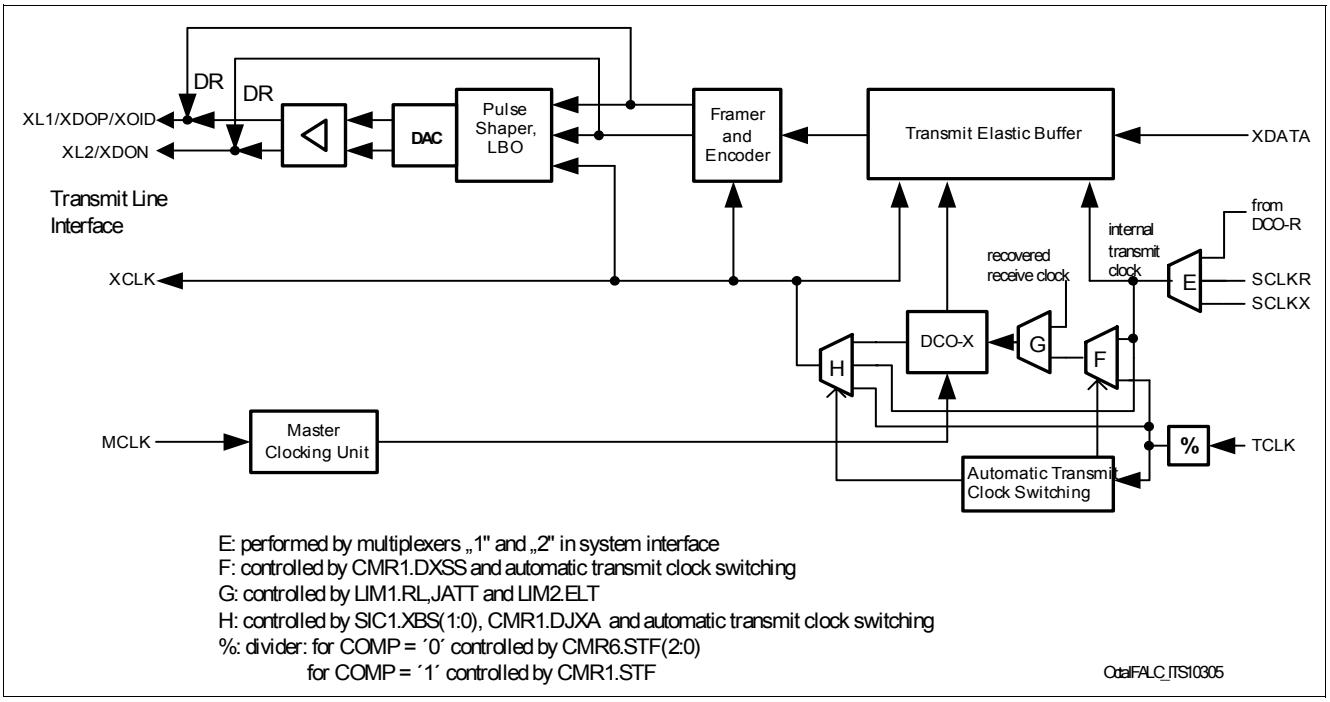


Figure 29 Transmit System of one channel

Note: DR = Dual-Rail interface

The serial bit stream is processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the four selectable framing formats
- Insertion of service and data link information
- AIS generation (blue alarm)
- Remote alarm (yellow alarm) generation
- CRC generation and insertion of CRC bits
- CRC bits inversion in case of a previously received CRC error or in case of activating per control bit
- Generation of loop-up/-down code
- Idle code generation per DS0

The frame/multiframe boundaries of the transmitter can be synchronized externally by using the $\overline{\text{SYPX}}$/XMFS pin. Any change of the transmit time slot assignment subsequently produces a change of the framing bit positions on the line side. This feature is required if signaling and data link bits are routed through the switching network and are inserted in transmit direction by the system interface.

In loop-timed configuration (LIM2.ELT) disconnecting the control of the transmit system highway from the transmitter is done by setting FMR5.XTM. The transmitter is now in a free running mode without any possibility to update the multiframe position in case of changing the transmit time slot assignment. The FS/DL-bits are generated independent of the transmit system interface. For proper operation the transmit elastic buffer size should be programmed to 2 frames.

The contents of selectable time slots is overwritten by the pattern defined by register IDLE. The selection of “idle channels” is done by programming the three-byte registers ICB(3:1).

If AMI coding with zero code suppression (B7-stuffing) is selected, “clear channels” without B7-stuffing can be defined by programming registers CCB(3:1).

3.7.1 Transmit Line Interface

The principal transmit line interface is shown in **Figure 30**. Two application modes are possible:

- For non-generic applications pins XL3 and XL4 can be left open. The serial resistance R_{SER} is dependent on the operation mode (E1/T1/J1) as shown in **Table 22**.
- For generic E1/T1/J1 applications with optimized return loss the transmit output resistance is configured by using the pins XL3 and XL4 as shown in **Figure 30**. The operation mode (E1/T1/J1) is selected by software (register bit PC6.TSRE) without the need for external hardware changes: Here R_{SER} is always 2 Ω, see **Table 22**.

In E1 mode the value of R_{SER} in **Table 22** is valid for both characteristic line impedances Z_0 = 120 Ω and Z_0 = 75 Ω.

In generic mode shorts between XL1 and XL2 cannot be detected, because the short current is lower than 120 mA, see **Chapter 3.7.6**.

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided on pin XDI and the digital transmitter.

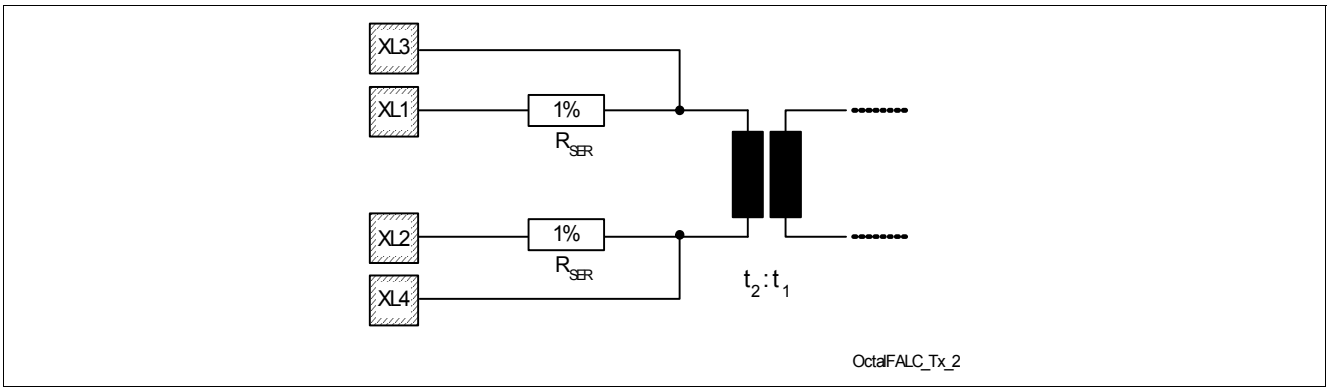


Figure 30 Transmit Line Interface

Table 22 Recommended Transmitter Configuration Values

R_{SER} [Ω], accuracy +/- 1 %	Application Mode	PC6.TSRE	XL3, XL4	Operation Mode
2[1)]	Generic	1	Connected to R_{SER} and Xformer junction	E1
		0		T1/J1
7.5	Non generic	0	Left open	E1
2		0	Left open	T1/J1

1) The values in this column refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

Similar to the receive line interface three different data types are supported:

- Ternary Signal: Single-rail data is converted into a ternary signal which is output on pins XL1 and XL2. Selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided. B7 stuffing can be disabled on a per time slot basis (Clear Channel capability). Selected by FMR0.XC(1:0) and LIM1.DRS = ´0´.
- Dual-rail data PCM(+), PCM(-) at multifunction ports XDOP and XDON with 50% or 100% duty cycle and with programmable polarity. Line coding is done in the same way as in ternary interface mode. Selected by FMR0.XC1 = ´1´ and LIM1.DRS = ´1´.
- Unipolar data on port XOID is transmitted in NRZ (non return to zero) with 100% duty cycle or in CMI code with or without (SIC3.CMI) preprocessed by B8ZS coding to a fiber-optical interface. Data is clocked on the rising edge of the transmit clock XCLK (1544 kHz). Selection is done by FMR0.XC1 = ´0´ and LIM1.DRS = ´1´.

An overview about the line coding is given in **Table 14**.

3.7.2 Transmit Clock TCLK

The transmit clock input TCLK of the OctalFALC™ can be configured for 1.544, 3.088, 6.176, 12.352 and 24.704 MHz input frequency in T1/J1 mode and 2.048, 4.096, 8.192, 16.384 and 32.768 MHz input frequency in E1 mode and in T1/J1 channel translation mode. If COMP = ´0´ frequency selection is done by the register bits CMR6.STF(2:0) (**CMR6_E**), if COMP = ´1´ selection is done by the register bit CMR1.STF (**CMR1_E**). See divider "%" in **Figure 29**.

3.7.3 Automatic Transmit Clock Switching

The transmit clock output XCLK can be derived from TCLK in two ways:

- Directly. In this case the TCLK frequency must be 32.768 MHz in E1 or 24.704 MHz in T1/J1 mode. (This can be performed only for COMP = ´0´.) or
- By using the DCO-X, were the DCO-X reference is TCLK.

If TCLK fails, then the transmit clock output XCLK will also fail. To avoid this, a so called automatic transmit clock switching can be enabled by setting the register bit CMR6.ATCS (**CMR6_E**). Then SCLKX will be used instead of TCLK if TCLK is lost. The transmit elastic buffer must be active. Automatically switching between TCLK and SCLKX is done in the following both cases:

- If the TCLK input is used directly as source for the transmit clock XCLK: The output of the DCO-X is not used. The DCO-X reference clock is SCLKX (selected by multiplexers "E", "F" and "G" in **Figure 29**). If loss of TCLK is detected, the transmit clock XCLK will be switched automatically (if CMR6.ATCS = ´1´) to the DCO-X output which is synchronous to SCLKX (see multiplexer "H" in **Figure 29**). If XCLK was switched to the DCO-X output and TCLK becomes active, switching of XCLK (back) to TCLK is automatically performed if CMR6.ATCS = ´1´. All switchings of XCLK between TCLK and the DCO-X output are shown in the interrupt status bit ISR7.XCLKSS0 which is masked by IMR7.XCLKSS0. These kinds of switching cannot be done in general without causing phase jumps in the transmit clock XCLK. Additionally after loss of TCLK the transmit clock XCLK is also lost during the "detection time" for loss of TCLK and the transmit pulses are disturbed. If CMR6.ATCS is cleared, TCLK is used (again) as source for the transmit clock XCLK, independent if TCLK is lost or not. The interrupt status bit ISR7.XCLKSS0 will be set also.
- If the transmit clock XCLK is sourced by the DCO-X output and the DCO-X reference clock is TCLK: The DCO-X reference will be switched automatically (if CMR6.ATCS = ´1´) to SCLKX (by multiplexer "F" of **Figure 29**) if SCLK is selected by multiplexer "E" of **Figure 29** after a loss of TCLK was detected. If the DCO-X reference was switched to SCLKX and TCLK becomes active, switching of the reference (back) to TCLK is automatically performed if CMR6.ATCS = ´1´. All switching of the reference between TCLK and SCLKX are shown in the interrupt status bit ISR7.XCLKSS1 which is masked by IMR7.XCLKSS1. For these kinds of automatic switching, the transmit clock XCLK fulfills the jitter-, wander- and frequency deviation- requirements as specified for E1/T1 after the clock source of the DCO-X is changed. If CMR6.ATCS is cleared, TCLK is used (again) as reference for the DCO-X, independent of whether TCLK is lost or not. The interrupt status bit ISR7.XCLKSS1 will be set also.

The status register bits CLKSTAT.TCLKLOS and CLKSTAT.SCLKXLOS (**CLKSTAT_E**, **CLKSTAT_T**) show if the appropriate clock is actually lost or not, so together with ISR7.XCLKSS1 and ISR7.XCLKSS0 the complete information regarding the current status of the transmit clock system is provided.

3.7.4 Transmit Jitter Attenuator

The transmit jitter attenuator is based on the so called DCO-X (digital clock oscillator, transmit) in the transmit path. Jitter attenuation of the transmit data is performed in the transmit elastic buffer, see **Figure 29**. The DCO-X circuitry generates a "jitter-free" transmit clock and meets the E1 requirements of ITU-T I.431, G. 736 to 739, G.823 and ETSI TBR12/13 and the T1 requirements of AT&T PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824. The DCO-X circuitry works internally with the same high frequency clock as the DCO-R. It synchronizes either to the working clock of the transmit system interface (internal transmit clock) or the clock provided on pin TCLK or the receive clock RCLK (remote loop/loop-timed). The DCO-X attenuates the incoming jitter starting at its corner frequency with 20 dB per decade fall-off. With the jitter attenuated clock, which directly depends on the phase difference between the incoming clock and the jitter

attenuated clock, data is read from the transmit elastic buffer (2 frames) or from the JATT buffer (2 frames, remote loop), see **Figure 31**. Wander with a jitter frequency below the corner frequency is passed transparently.

The DCO-X is equivalent to the DCO-R so that the principle for its configuration is the same, see **Figure 24** and **CMR3_E**, **CMR4_E** and **CMR5_E**.

The DCO-X reference clock is monitored: If one, two or three clock periods of the 2.048 MHZ (1.544 MHz in T1/J1 mode) clock at SCLKX are missing the DCO-X regulates it´s output frequency. If four or more clock periods are missing

- The DCO-X circuitry is automatically centered to the nominal frequency of 16 x f_{DATA} if the center function of DCO-X is enabled by CMR2.DCOXC = ´1´.
- The actual DCO-X output frequency is “frozen” if the center function of DCO-X is disabled by CMR2.DCOXC = ´0´.

The jitter attenuated clock is output on pin XCLK if the transmit jitter attenuator is enabled, see multiplexer “H” in **Figure 29**.

The transmit jitter attenuator can be disabled. In that case data is read from the transmit elastic buffer with the clock sourced on pin TCLK, see multiplexer “H” in **Figure 29**. Synchronization between SCLKX and TCLK has to be done externally.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized on RCLK, see **Figure 31** and multiplexers “G” and “F” in **Figure 29**. In this configuration the transmit elastic buffer has to be enabled.

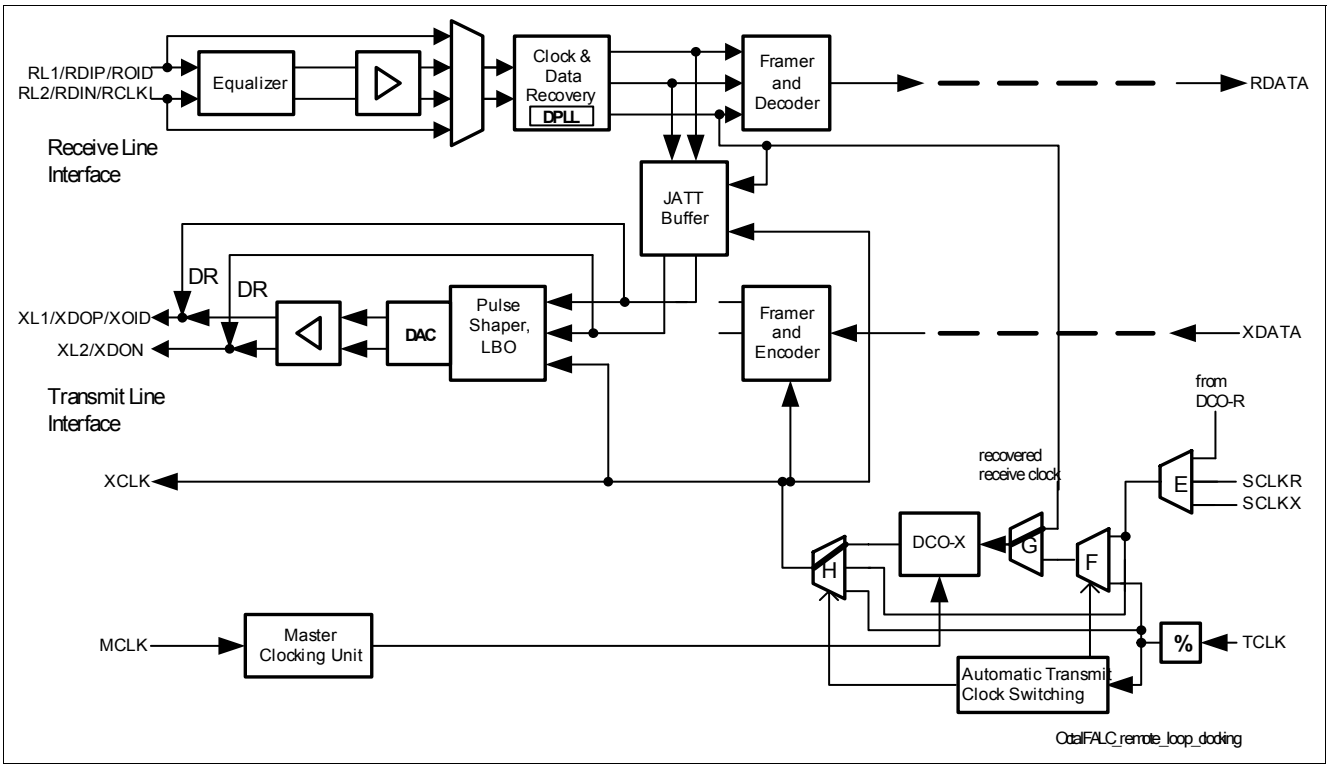


Figure 31 Clocking and Data in Remote Loop Configuration

3.7.5 Programmable Pulse Shaper and Line Build-Out

The transmitter includes a programmable pulse shaper to generate transmit pulse masks according to:

- For T1: FCC68; ANSI T1. 403 1999, figure 4; ITU-T G703 11/2001, figure 10 (for different cable lengths), see **Figure 122** and **Figure 33** for measurement configuration were R_{load} = 100 Ω
- For E1: ITU-T G703 11/2001, figure 15 (for 0 m cable length) see **Figure 121**; ITU-T G703 11/2001, figure 20 (for DCIM mode), see **Figure 32** for measurement configuration were R_{load} = 120 Ω or R_{load} = 75 Ω

The transmit pulse shape (U_{PULSE}) is programmed either

- By the registers XMP(2:0) compatible to the QuadFALC®, see **Table 23** and **Table 24**, if the register bit XPM2.XPDIS is cleared, see **XPM2_E**
- Or by the registers TXP(16:1), see **TXP1_E**, if the register bit XPM2.XPDIS is set, see **Table 25** and **Table 26**. For more details see chapter “Operational Description”

To reduce the crosstalk on the received signals in long haul applications the OctalFALC™ offers the ability to place a transmit attenuator (Line Build-Out, LBO) in the data path. This is used only in T1 mode. LBO attenuation is selectable with the values 0, -7.5, -15 or -22.5 dB (register bits **LIM2_T**.LBO(2:1)). ANSI T1. 403 defines only 0 to -15 dB.

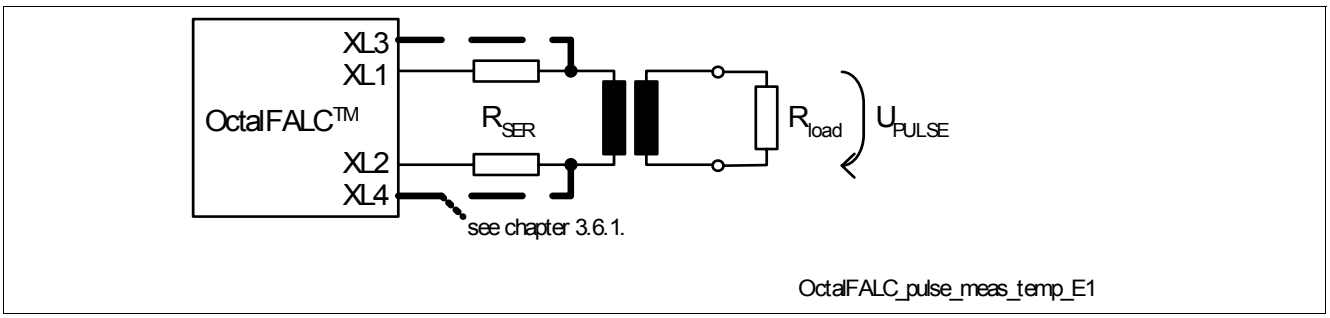


Figure 32 Measurement Configuration for E1 Transmit Pulse Template

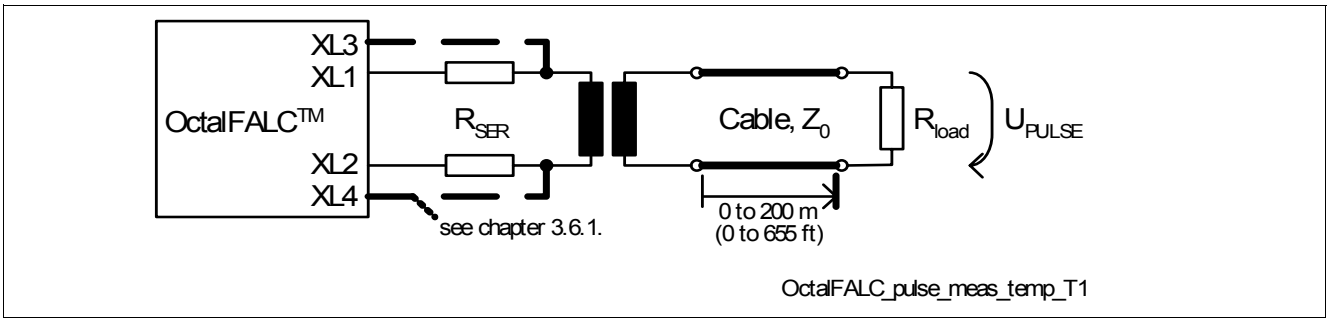


Figure 33 Measurement Configuration for T1/J1 Transmit Pulse Template

3.7.5.1 QuadFALC® Compatible Programming

After reset XPM2.XPDIS is zero so that QuadFALC® compatible programming is selected. The default setting after reset for the registers XMP(2:0) generates the E1 pulse shape, see **Table 24**, but with an unreduced amplitude. No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming as described in **Table 23** is necessary.

If LBO attenuation is selected, the programming of XPM(2:0) will be ignored. Instead the pulse shape programming is handled internally: The generated pulse shape before LBO filtering is the same as for T1 0 to 40 m.

The given values are optimized for transformer ratio: 1 : 2.4 and cable type AWG24 using transmitter configurations listed in **Table 22** and shown in **Figure 30**. The measurement configurations of **Figure 32** with R_{load} = 120 Ω and **Figure 33** with R_{load} = 100 Ω are used.

Table 23 Recommended Pulse Shaper Programming for T1/J1 with registers XPM(2:0) (Compatible to QuadFALC®)

LBO	Range	Range	XPM0	XPM1	XPM2
[dB]	[m]	[ft]	hexadecimal		
0	0 to 40	0 to 133	D7	22	1
0	40 to 81	133 to 266	FA	26	1
0	81 to 122	266 to 399	3D	37	1
0	122 to 162	399 to 533	5F	3F	1

Table 23 Recommended Pulse Shaper Programming for T1/J1 with registers XPM(2:0) (Compatible to QuadFALC® (cont'd))

LBO	Range	Range	XPM0	XPM1	XPM2
0	162 to 200	533 to 655	3F	CB	1
7.5	---		Are not taken into account: Pulse shape generation is handled internally.		
15	---				
22.5	---				

Table 24 Recommended Pulse Shaper Programming for E1 with registers XPM(2:0) (Compatible to QuadFALC®)

R_{SER}	Z_0	Transmit Line Interface Mode	XPM0	XPM1	XPM2
[Ω]	[Ω]		hexadecimal		
7.5[1)]	120	Non generic	9C	03	00
7.5	75	Non generic	BD	03	00
---	Reset values		7B	03	40
7.5	DCIM Mode	Non generic	EF	BD	07

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

3.7.5.2 Programming with TXP(16:1) Registers

By setting of register bit XPM2.XPDIS the pulse shape will be configured by the registers TXP(16:1) (TXP1_E). Each of these registers define the amplitude value of one sampling point in the symbol. A symbol is formed by 16 sampling points.

The default setting after reset for the registers TXP(16:1) generates also the E1 pulse shape (0m), but with an unreduced amplitude. (TXP(9:16) = ´00_H´; TXP(1:8) = ´38_H´= 56_D´) No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming like Table 25 is necessary.

The pulse shape configuration will be done also by the registers TXP(16:1) if LBO attenuation is selected. The pulse shape is then determined by both the values of TXP(16:1) and the LBO filtering.

The given values in Table 25 and Table 26 are optimized for transformer ratio: 1 : 2.4; cable: AWG24 and configurations listed in Table 22 and shown in Figure 30.

Table 25 Recommended Pulse Shaper Programming for T1 with registers TXP(16:1)

LBO	Range	Range	TXP values, decimal															
[dB]	[m]	[ft]	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0 to 40	0 to 133	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
0	40 to 81	133 to 266	48	50	48	46	46	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
0	81 to 122	266 to 399	56	58	54	52	48	48	48	48	16	-25	-17	-14	-4	-4	-4	-4
0	122 to 162	399 to 533	63	63	58	56	52	52	51	51	16	-34	-32	-17	-4	-4	-4	-4
0	162 to 200	533 to 655	63	63	63	58	50	50	50	50	50	-60	-26	-20	-12	-8	-6	-4
7.5	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
155	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
22.5	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4

Table 26 Recommended Pulse Shaper Programming for E1 with registers TXP(16:1)

R_{SER}	Z_0	Transmit Line Interface Mode	TXP values, decimal															
[Ω]	[Ω]		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
2[1)]	120	Generic	42	40	40	40	40	40	40	42	0	0	0	0	0	0	0	0
7.5	120	Non generic	63	57	57	57	57	57	57	57	-4	0	0	0	0	0	0	0
2	75	Generic	42	40	40	40	40	40	40	40	0	0	0	0	0	0	0	0
7.5	75	Non generic	60	58	58	58	58	58	58	58	0	0	0	0	0	0	0	0
--	Reset values		56	56	56	56	56	56	56	56	0	0	0	0	0	0	0	0
2	DCIM Mode	Generic	20	20	20	20	20	20	20	20	-20	-20	-20	-20	-20	-20	-20	-20
7.5	DCIM mode	Non generic	28	28	28	28	28	28	28	28	-28	-28	-28	-28	-28	-28	-28	-28

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

3.7.6 Transmit Line Monitor

The transmit line monitor (see principle in **Figure 34**) compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly increased transmit line current (more than 120 mA for at least 3 consecutive pulses sourced by VDDX) and protects the device from damage by setting the transmit line driver XL1/2 into high-impedance state automatically (if enabled by XPM2.DAXLT = ´0´, see **XPM2_E**). The current limiter checks the actual current value of XL1/2 and if the transmit line current drops below the detection limit the high-impedance state is cleared.

Two conditions are detected by the monitor:

- Transmit line ones density (more than 31 consecutive zeros) indicated by FRS1.XLO (**FRS1_E**).
- Transmit line high current indicated by FRS1.XLS.

In both cases a transmit line monitor status change interrupt is provided.

Shorts between XL1 or XL2 and V_{DD} , V_{DDC} or V_{DDP} are not detected.

Note that in generic mode (see **Chapter 3.7.1**) where the pins XL3 and XL4 are used, shorts between XL1 and XL2 cannot be detected, because the short circuit current is lower than 120 mA. This way a short between XL1 and XL2 will not harm the device.

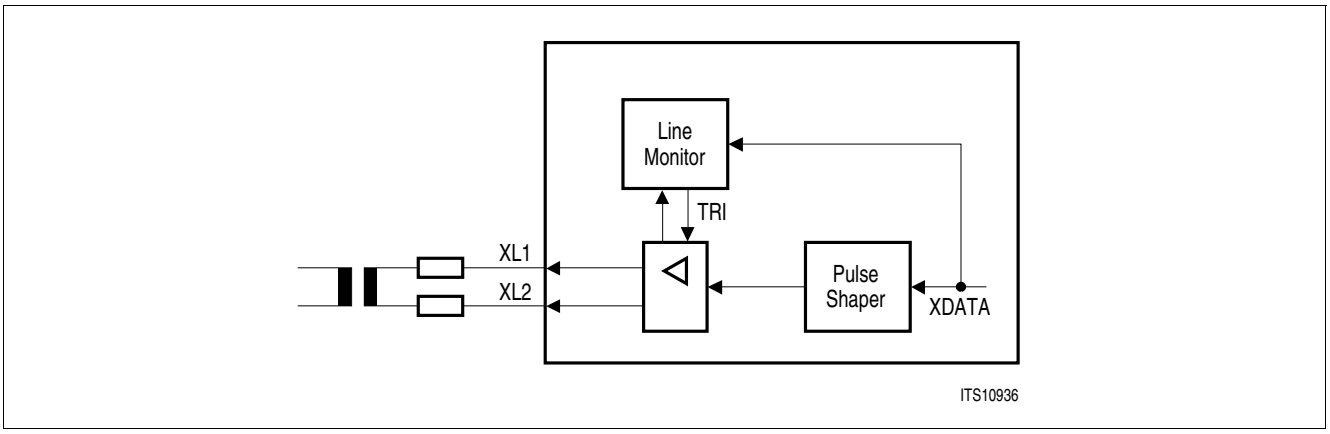


Figure 34 Transmit Line Monitor Configuration

3.8 Multi Function Ports

Several signals are available on the multi function ports, see **Table 27** and **PC1_E**. After reset, input function is selected ($\overline{\text{SYPR}}$ or $\overline{\text{SYPX}}$) with exception of the ports RPC were RCLK output is selected: The register bits PC3.RPC2 have the reset value ´FH´. (Note that PC5.CRP must be set to ´1´ for an active RCLK output. After reset PC5.CRP is ´0´ and RCLK is pulled up.)

Three multi function ports (MFP) for RX - so called as RPA, RPB, RPC - and two MFPs for TX - so called as XPA, XPB - are implemented for each channel.

The functions of RPA, RPB and RPC are configured by PC1.RPC1(3:0) , PC2.RPC2(3:0) and PC3.RPC3(3:0) respectively.

The functions of XPA and XPB are configured by PC1.XPC1(3:0) and PC2.XPC2(3:0) respectively.

The actual logical state of the 5 multifunction ports can be read out using the register MFPI (**MFPI_E**). This function together with static output signal options in **Table 27** offers general purpose I/O functionality on unused multi function port pins.

If a port is configured as GPOH or GPOL the port level is set to high or low level respectively.

Each of the input functions may only be selected once in a channel except for the GPI functionality. No input function must be selected twice or more.

Table 27 Multi Function Port Selection

Selection	RFP Signal	Available on port	RFP Function	XFP Signal	Available on port	XFP Function
0000	$\overline{\text{SYPR}}$	A, B, C	Synchronous pulse receive input	$\overline{\text{SYPX}}$	A, B	Synchronous pulse transmit input
0001	RFM	A, B, C	Receive frame marker output	XMFS	A, B	Transmit multiframe synchronization input
0010	RMFB	A, B, C	Receive multiframe begin marker output	XSIG	A, B	Transmit signaling data input
0011	RSIGM	A, B, C	Receive signaling marker output	TCLK	A, B	Transmit clock input
0100	RSIG	A, B, C	Receive signaling data output	XMFB	A, B	Transmit multiframe begin marker output
0101	DLR	A, B, C	Data link bit receive output	XSIGM	A, B	Transmit signaling marker output
0110	FREEZE	A, B, C	Freeze signaling output	DLX	A, B	Data link bit transmit output
0111	$\overline{\text{RFSP}}$	A, B, C	Frame synchronous pulse output	XCLK	A, B	Transmit clock output
1000	RLT	A, B, C	Receive line termination (analog switch); a logical equivalence is build with LIM0.RTRS	XLT	A, B	Transmit line tristate control, high active
1001	GPI	A, B, C	General purpose input	GPI	A, B	General purpose input

Table 27 Multi Function Port Selection (cont'd)

Selection	RFP Signal	Available on port	RFP Function	XFP Signal	Available on port	XFP Function
1010	GPOH	A, B, C	General purpose output high	GPOH	A, B	General purpose output high
1011	GPOL	A, B, C	General purpose output low	GPOL	A, B	General purpose output low
1100	LOS	A, B, C	Loss of signal indication output	Reserved	A, B	Reserved
1101	RTDMT	A, B, C	Receive system interface tristate for pins RDO, RSIG, SCLKR, RFM; logically exored with SIC3.RRTRI	XDIN	A, B	Transmit data negative input
1110	RDON	A, B, C	Receive data negative output or bipolar violation output	$\overline{\text{XLT}}$	A, B	Transmit line tristate control, low active
1111	RCLK	A, B, C	RCLK output	Reserved	A, B	Reserved

4 Functional Description E1

4.1 Receive Path (E1)

An overview of the receive path of one channel of the OctalFALC™ for all modes is given in **Figure 21**. Only special E1 functionalities are described in this chapter.

4.1.1 Receive Line Coding (E1)

The HDB3 line code or the AMI coding is provided for the data received from the ternary or the dual-rail interface. In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with HDB3 or AMI postprocessing is provided. If CMI code is selected the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. For NRZ coding, data is latched with the falling edge of signal RCLKI. The HDB3 code is used along with double violation detection or extended code violation detection (selectable by FMR0.EXZE)). In AMI code all code violations are detected. The detected errors increment the code violation counter (16 bits length).

When using the optical interface with NRZ coding, the decoder is bypassed and no code violations are detected.

The signal at the ternary interface is received at both ends of a transformer.

4.1.2 Loss-of-Signal Detection (E1)

There are different definitions for detecting Loss-Of-Signal (LOS) alarms in the ITU-T G.775 and ETS 300233. The OctalFALC™ covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable by using register GCR.SCI.

- Detection: An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS = ´0´) (**LIM1_E**). The receive signal level Q is programmable by three control bits LIM1.RIL(2:0) see **Table 139**. The number N can be set by an 8-bit register (PCD). The contents of the PCD register is multiplied by 16, which results in the number of pulse periods, i.e. the time which has to suspend until the alarm has to be detected. The programmable range is 16 to 4096 pulse periods. ETS300233 requires detection intervals of at least 1 ms. This time period results always in a LFA (Loss of Frame Alignment) before a LOS is detected.
- Recovery: In general the recovery procedure starts after detecting a logical one (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL(2:0)) of the nominal pulse. The value in the 8-bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm.

If a loss-of-signal condition is detected in long-haul mode, the data stream can optionally be cleared automatically to avoid bit errors before LOS is indicated. The Selection is done by LIM1.CLOS = ´1´.

4.1.3 Receive Jitter Attenuation Performance (E1)

The jitter attenuator meets the jitter transfer requirements of the ITU-T I.431 and G.735 to 739 (refer to **Figure 35**)

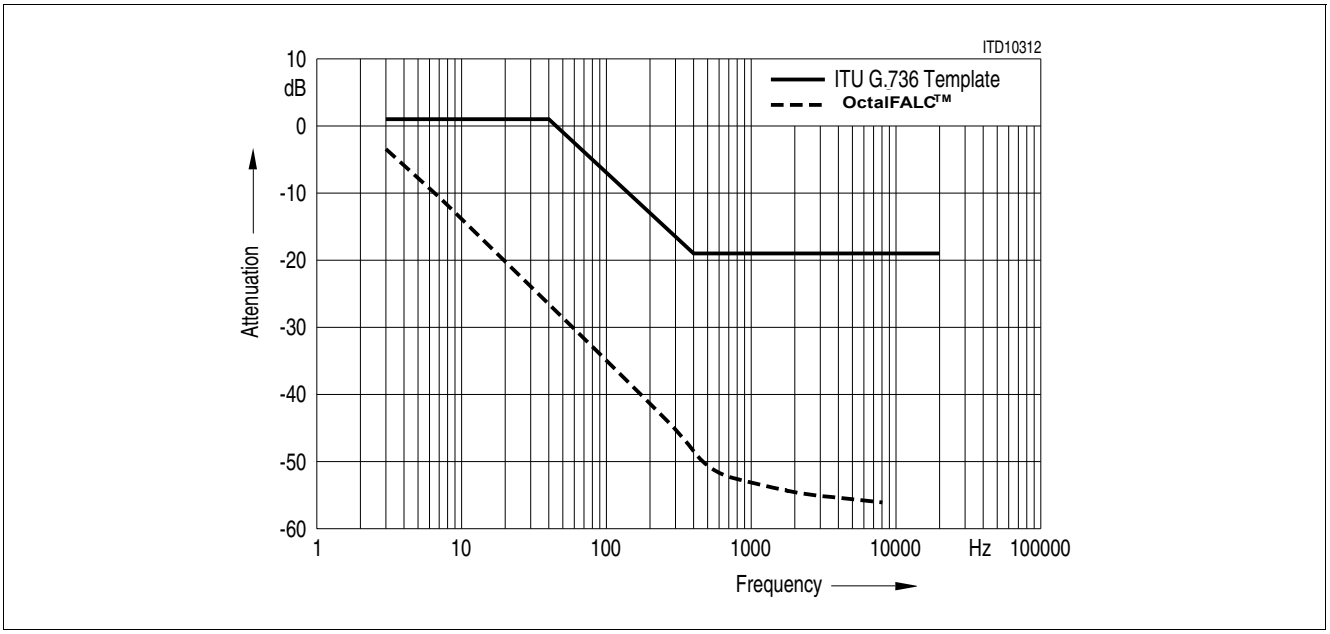


Figure 35 Jitter Attenuation Performance (E1)

Also the requirements of ETSI TBR12/13 are satisfied. Insuring adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz the DCO-R circuitry starts jitter attenuation at about 2 Hz.

4.1.4 Jitter Tolerance (E1)

The OctalFALC™ receiver's tolerance to input jitter complies with ITU for CEPT applications.

Figure 36 shows the curves of different input jitter specifications stated below as well as the OctalFALC™ performance.

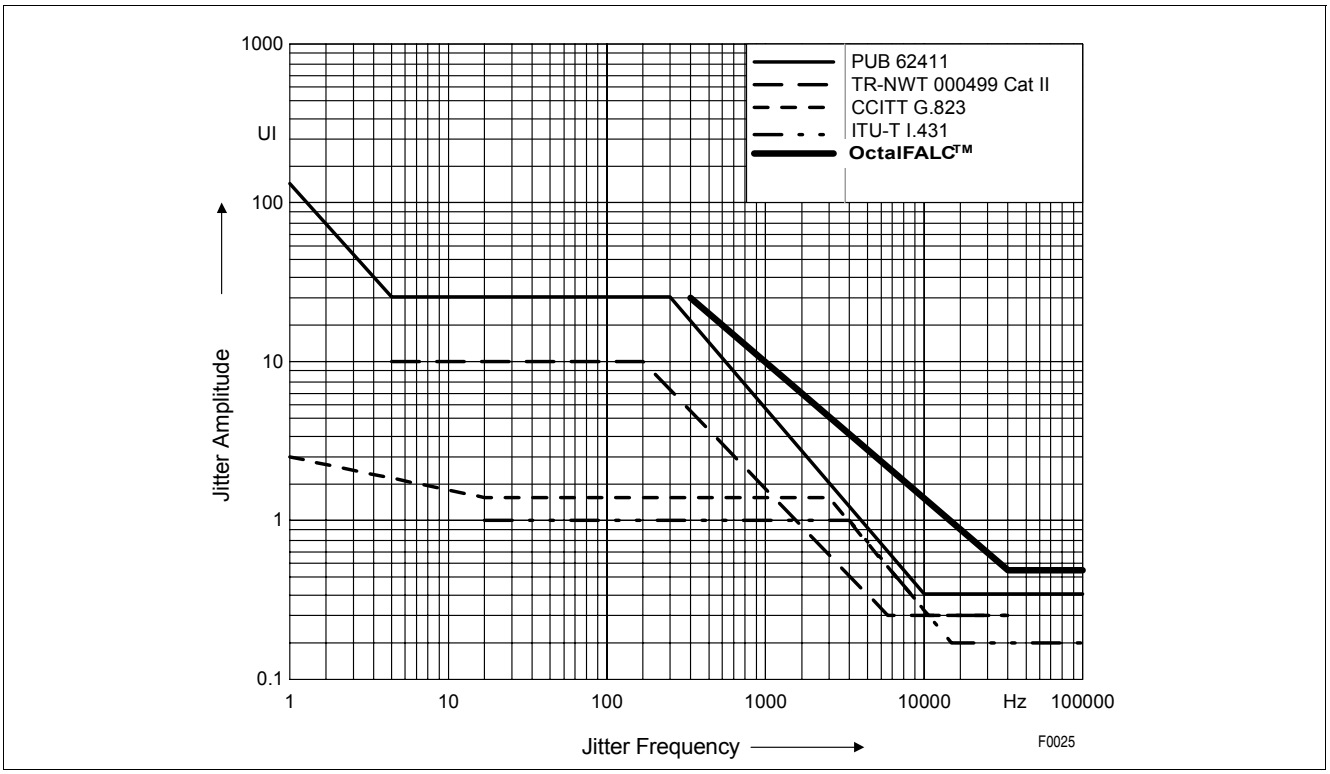


Figure 36 Jitter Tolerance (E1)

4.1.5 Output Jitter (E1)

In the absence of any input jitter the OctalFALC™ generates the intrinsic output jitter, which is specified in the**Table 28** below.

Table 28 Output Jitter (E1)

Specification	Measurement Filter Bandwidth		Intrinsic Output Jitter [UI peak to peak]
	Lower Cutoff	Upper Cutoff	
ITU-T I.431	20 Hz	100 kHz	< 0.015
	700 Hz	100 kHz	< 0.015
ETSI TBR 12	40 Hz	100 kHz	< 0.11

4.1.6 Framer/Synchronizer (E1)

The following functions are performed:

- Synchronization on pulse frame and multiframe
- Error indication when synchronization is lost. In this case, AIS is sent automatically to the system side and remote alarm is sent to the remote end if enabled.
- Initiating and controlling of re synchronization after reaching the asynchronous state. This can be done automatically by the OctalFALC™ or user controlled over the asynchronous, SPI or SCI interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in status registers.
- Generation of various maskable interrupt statuses of the receiver functions.
- Generation of control signals to synchronize the CRC checker, and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe according to the CRC4 procedure (refer to ITU-T G.704). These bits are compared with those check bits that are received during the next CRC submultiframe. If there is at least one mismatch, the CRC error counter (16 bit) is incremented.

4.1.7 Receive Elastic Buffer (E1)

The received bit stream is stored in the receive elastic buffer, see **Figure 21**. The size of the elastic buffer can be configured independently for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS(1:0):

- RBS(1:0) = ´00_b´: two frame buffer or 512 bits. Maximum of wander amplitude (peak-to-peak): 190 UI (1 UI = 488 ns). Average delay after performing a slip: 1 frame or 256 bits
- RBS(1:0) = ´01_b´: one frame buffer or 256 bits. Maximum of wander amplitude: 100 UI. Average delay after performing a slip: 128 bits,
- RBS(1:0) = ´10_b´: short buffer or 96 bits. Maximum of wander amplitude: 38 UI. Average delay after performing a slip: 48 bits,
- RBS(1:0) = ´11_b´: Bypass of the receive elastic buffer

The functions are:

- Clock adoption between system clock (SCLKR) and internally generated route clock (recovered line clock), see **Chapter 3.6.5**.
- Compensation of input wander and jitter.
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel data which is circularly written to the elastic buffer using internally generated receive route clock.

Writing of received data from the line is controlled by the internally generated route clock (recovered line clock).

Reading of stored data is controlled either by the system clock sourced by SCLKR or by the DCO-R of the receive jitter attenuator and the synchronization pulse ($\overline{SYPR}$) together with the programmed offset values for the receive time slot/clock slot counters. After conversion into a serial data stream, the data is given out on port RDO. If the

receive buffer is bypassed programming of the time slot offset is disabled and data is clocked off with internally generated route clock (recovered line clock) instead of SCLKR.

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 128 or 46 bits. In bypass mode the time slot assigner is disabled. In this case $\overline{SYPR}$ programmed as input is ignored. Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

The following table gives an overview of the receive buffer operating mode.

Table 29 Receive Buffer Operating Modes (E1)

Buffer Size (SIC1.RBS(1:0))	TS Offset Programming (RC(1:0)) + $\overline{SYPR}$ = input	Slip Performance
Bypass[1)]	Disabled Recommended: $\overline{SYPR}$ = output	No
Short buffer	Not recommended, Recommended: $\overline{SYPR}$ = output	Yes
1 frame	Not recommended, Recommended: $\overline{SYPR}$ = output	Yes
2 frames	Enabled	Yes

1) In bypass mode the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

In single frame mode (SIC1.RBS), values of receive time slot offset (RC(1:0)) have to be specified large enough to prevent approach of frame begin on the line side and frame begin on the system side.

Figure 37 gives an idea of operation of the receive elastic buffer: A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface. I.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

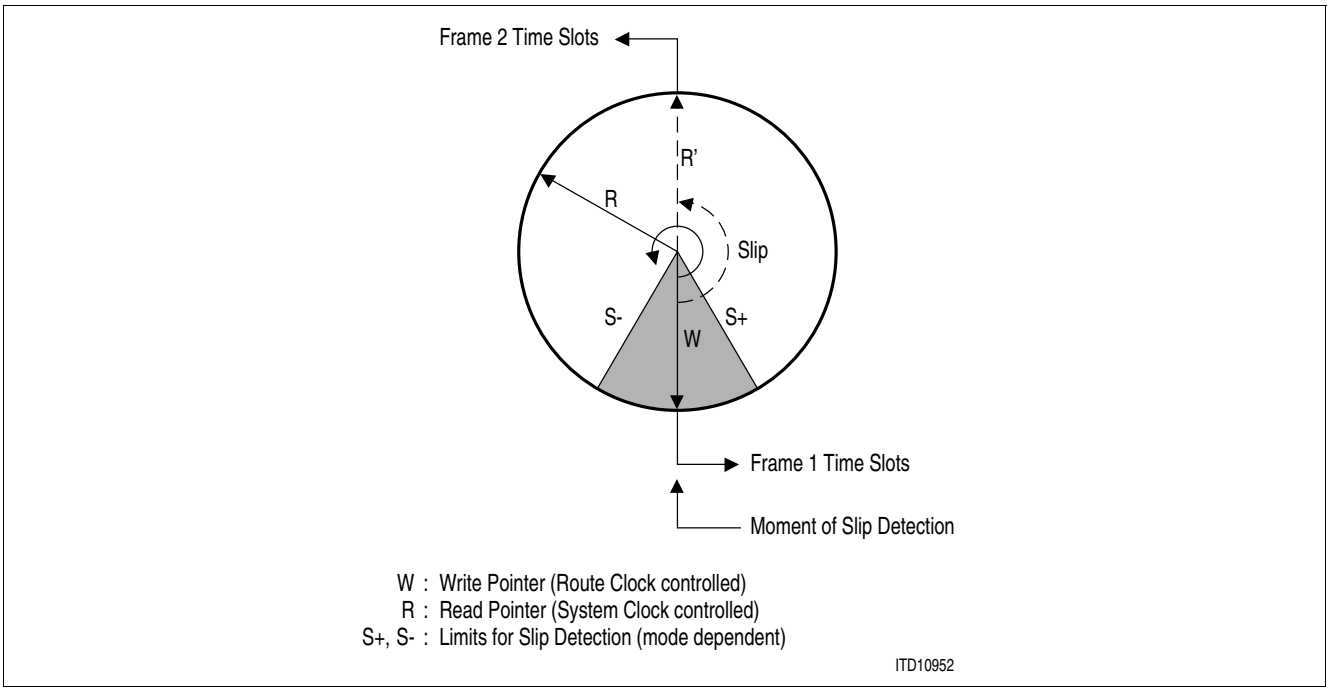


Figure 37 The Receive Elastic Buffer as Circularly Organized Memory

4.2 Transmit Path (E1)

An overview of the transmit path of one channel of the OctalFALC™ for all modes is given in **Figure 29**. Only special E1 functionalities are described in this chapter.

4.2.1 Transmit Elastic Buffer (E1)

The received bit stream from pin XDI is optionally stored in the transmit elastic buffer, see **Figure 29**. The memory is organized as the receive elastic buffer. The functions are the same as for the receive side. Programming of the transmit buffer size is done by SIC1.XBS1/0:

- XBS(1:0) = ´00_b´: Bypass of the transmit elastic buffer
- XBS(1:0) = ´01_b´: one frame buffer or 256 bits Maximum of wander amplitude (peak-to-peak): 100 UI (one UI = 488 ns) average delay after performing a slip: 128 bits
- XBS(1:0) = ´10_b´: two frame buffer or 512 bits Maximum of wander amplitude: 190 UI average delay after performing a slip: 1 frame or 256 bits
- XBS(1:0) = ´11_b´: short buffer or 92 bits: Maximum of wander amplitude: 18 us average delay after performing a slip: 46 bits

The functions of the transmit buffer are:

- Clock adoption between system clock (SCLKX) and internally generated transmit route clock (XCLK), see **Chapter 3.7.4**.
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit route frame
- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX/R and $\overline{\text{SYPX}}$/XMFS in combination with the programmed offset values for the transmit time slot/clock slot counters.

Reading of stored data is controlled by the clock generated either by the DCO-X circuitry or the externally generated TCLK and the transmit framer. With the de-jittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN. If the transmit buffer is bypassed data is directly transferred to the transmitter.

The following table gives an overview of the transmit buffer operating modes.

Table 30 Transmit Buffer Operating Modes (E1)

SIC1.XBS(1:0)	Buffer Size	TS Offset Programming	Slip Performance
00	Bypass	Enabled	No
11	Short buffer	Enabled	Yes
01	1 frame	Enabled	Yes
10	2 frames	Enabled	Yes

4.3 Signaling Controller (E1)

The signaling controller can be programmed to operate in various signaling modes. The OctalFALC™ performs the following signaling and data link methods.

4.3.1 HDLC or LAPD Access (E1)

The OctalFALC™ offers three independent HDLC controllers for each of the eight channels. All of them provide the following features:

- Receive FIFO for each channel, configurable up to 128 byte, see also **Chapter 3.4.3**
- 128 byte transmit FIFO for each channel
- Transmission in one of 31 time slots (time slot number programmable for each channel individually)
- Transmission in even frames only, odd frames only or both (programmable for each channel individually)

- Bit positions to be used in selected time slots are maskable (any bit position can be enabled for each channel individually)
- HDLC or transparent mode
- Flag detection
- CRC checking
- Bit-stuffing
- Flexible address recognition (1 byte, 2 bytes)
- C/R-bit processing (according to LAPD protocol)

In addition to this, HDLC channel 1 provides:

- SS7 support
- BOM (bit oriented message) support
- Use of time slot 0 (up to 32 time slots)
- Use of S_a-bits
- Flexibility to insert and extract data during certain time slots, any combination of time slots can be programmed independently for the receive and transmit direction

The receive FIFO structure is described in **Chapter 3.4.3**.

Each of these HDLC controllers can be attached to either the line side (so called as “standard configuration”, see **Figure 38**) or the system side (“inverse configuration”, see **Figure 39**). Inverse HDLC mode is selected by setting MODE.HDLCI = ´1´, MODE2.HDLCI2 = ´1´ or MODE3.HDLCI3 = ´1´ (for each of the three HDLC controllers and each of the eight E1/T1/J1 ports individually).

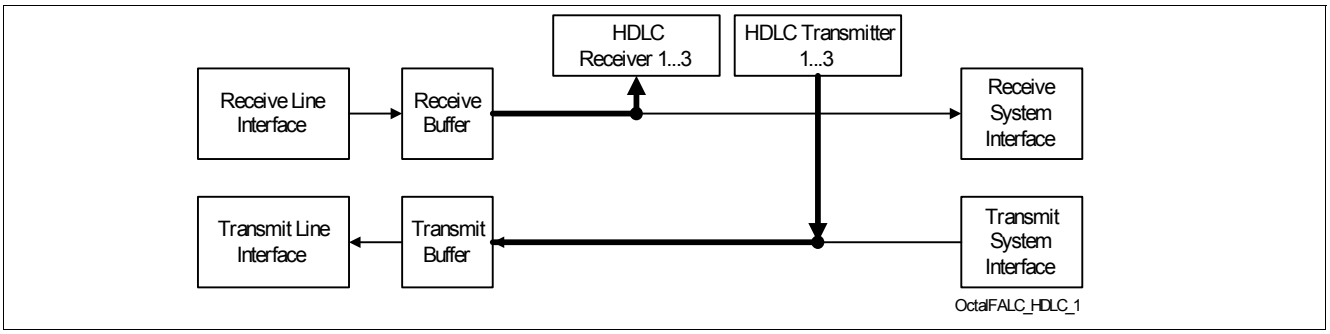


Figure 38 HDLC Controller Standard Configuration

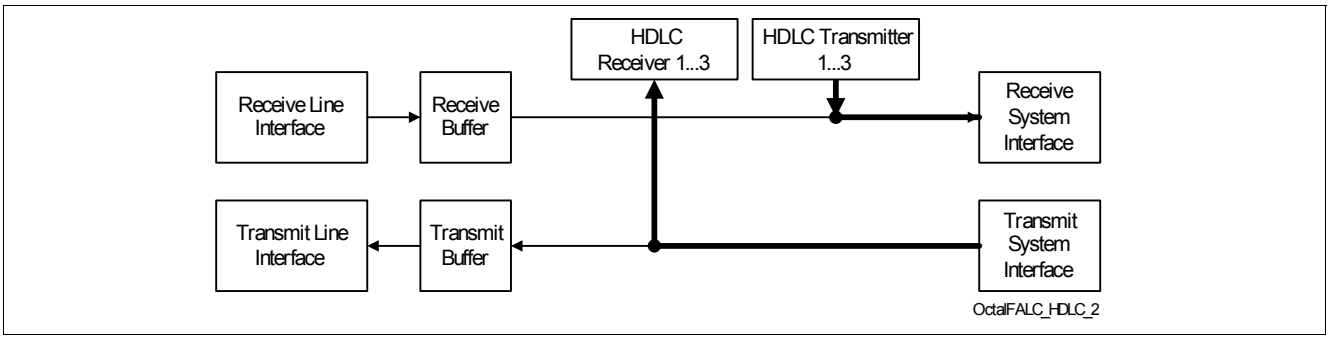


Figure 39 HDLC Controller Inverse Configuration

Each HDLC controller can be reset individually without disturbing the transmission on the remaining channels. Use CMDR.SRES for HDLC channel 1, CMDR3.SRES2 for HDLC channel 2 and CMDR4.SRES3 for HDLC channel 3, respectively.

Note that CMDR.RRES resets the whole RX path and therefor all HDLC channels.

After a XDU interrupt on a HDLC controller, the appropriate transmit signaling controller must be reset.

After an RDO interrupt on a HDLC controller, the receive HDLC controller needs no reset. So a receive HDLC controller reset per channel is not necessary.

In case of common channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 is supported. The signaling controller of the OctalFALC™ performs the flag detection, CRC checking, address comparison and zero-bit removing. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the OctalFALC™ performs a 1 or 2-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value ´FE_H´ or ´FC_H´ (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison. Buffering of receive data is done in a 128 byte deep RFIFO. In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without flag recognition, CRC checking or bit stuffing. This allows user specific protocol variations.

The transmit signaling controller of the OctalFALC™ performs the flag generation, CRC generation, zero-bit stuffing and programmable idle code generation. Buffering of transmit data is done in the 128 byte deep XFIFO. The signaling information is internally multiplexed with the data applied to port XDI or XSIG. In signaling controller transparent mode, fully transparent data transmission without HDLC framing is performed. Optionally the OctalFALC™ supports the continuous transmission of the XFIFO contents. The OctalFALC™ offers the flexibility to insert data during certain time slots. Any combinations of time slots can be programmed separately for the receive and transmit direction if using HDLC channel 1. HDLC channel 2 and 3 support one programmable time slot common for receive and transmit direction each.

4.3.2 Support of Signaling System #7 (E1)

HDLC controller 1 of each of the eight channels of the OctalFALC™ supports the signaling system #7 (SS7) which is described in ITU-Q.703. The following description assumes, that the reader is familiar with the SS7 protocol definition.

SS7 support must be activated by configuring the register bits MODE.MDS(3:0), see **MODE_E**. The SS7 protocol is supported by the following hardware features in receive mode:

- All Signaling Units (SU) are stored in the receive FIFO (RFIFO)
- Detecting of flags from the incoming data stream
- Bit stuffing (zero deletion)
- Checking of seven or more consecutive ones in the receive data stream
- Checking if the received Signaling Unit is a multiple of eight bits and at least six octets including the opening flag
- Calculation of the CRC16 checksum: In receive direction the calculated checksum is compared to the received one; errors are reported in register RSIS.
- Checking if the signal information field of a received signaling unit consists of more than 272 octets, in this case the current signaling unit is discarded.

In order to reduce the microprocessor load, fill In signaling units (FISUs) are processed automatically. By examining the length indicator of a received signal unit the OctalFALC™ decides whether a FISU has been received. Consecutively received FISUs are compared and optionally not stored in the receive FIFO (RFIFO), if the contents is equal to the previous one. The same applies to link status signaling units, if bit CCR5.CSF (**CCR5_E**) is set. The different types of signaling units as message signaling unit (MSU), link status signaling unit (LSSU) and fill in signaling units (FISU) are indicated in the RSIS register, which is automatically added to the RFIFO with each received signaling unit. The complete signaling unit except start and end flags is stored in the receive FIFO. The functions of bits CCR2.RCRC and CCR2.RADD are still valid in SS7 mode (**CCR2_E**). Errored signaling units are handled automatically according to ITU-T Q.703 as shown in **Figure 40**. SU counter (su) and errored SU counter (C_s) are reset by setting CMDR2.RSUC. The error threshold T can be selected to be 64 (default) or 32 by setting/clearing bit CCR5.SUET (**CCR5_E**). If the defined error limit is exceeded, an interrupt (ISR1.SUEX) is generated, if not masked by IMR1.SUEX = ´1´ (**ISR1_E**).

Note: If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).

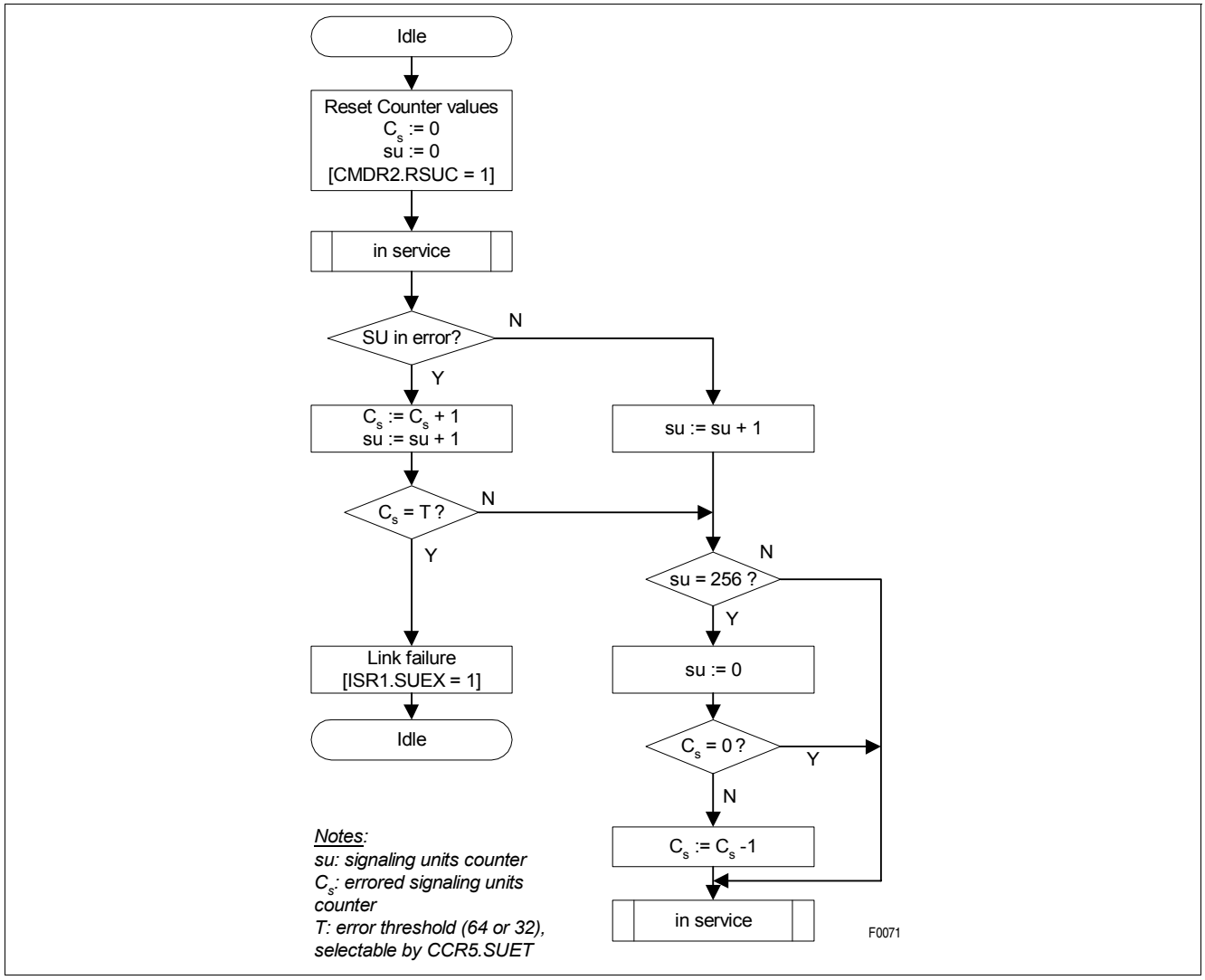


Figure 40 Automatic Handling of Errored Signaling Units

The SS7 protocol is supported by the following hardware features in transmit direction:

- Transmission of flags at the beginning of each Signaling Unit
- Bit stuffing (zero insertion)
- Calculation of the CRC16 checksum: The transmitter adds the checksum to each Signaling Unit.

Each Signaling Unit written to the transmit FIFO (XFIFO) is sent once or repeatedly including flags, CRC checksum and stuffed bits. After e.g. an MSU has been transmitted completely, the OctalFALC™ optionally starts sending of FISUs containing the forward sequence number (FSN) and the backward sequence number (BSN) of the previously transmitted Signaling Unit. Setting bit CCR5.AFX causes Fill In Signaling Units (FISUs) to be sent continuously, if no HDLC or Signaling Unit (SU) is to be transmitted from XFIFO. During update of XFIFO, automatic transmission is interrupted and resumed after update is completed. The internally generated FISUs contain FSN and BSN of the last transmitted Signaling Unit written to XFIFO.

Using CMDR.XREP = ´1´, the contents of XFIFO can be sent continuously. Clearing of CMDR.XREP stops the automatic repetition of transmission. This function is also available for HDLC frames, so no flag generation, CRC byte generation and bit stuffing is necessary. Example: After an MSU has been sent repetitively and XREP has been cleared, FISUs are sent automatically.

Whether a repetitive transmission is currently ongoing can be monitored in SIS.XREP. During a repetitive transmission a write operation to CMDR with CMDR.XREP = ´1´will not interrupt the repetitive transmission.

4.3.3 S_a-Bit Access in Receive Direction (E1)

The OctalFALC™ supports the S_a-bit signaling of time slot 0 of every other frame as follows:

- The access through register RSW
- The access through registers RSA(8:4), capable of storing the information for a complete multiframe
- The access through the up to 128 byte (user) deep receive FIFO of the signaling controller of HDLC channel 1. This S_a-bit access gives the opportunity to receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a-bits which shall be extracted and stored in the RFIFO is selected by XC0.SA(8:4). The access to the RFIFO is supported by ISR0.RME/RPF.

4.3.4 S_a-Bit Access in Transmit Direction (E1)

The OctalFALC™ supports the S_a-bit signaling of time slot 0 of every other frame as follows:

- The access through register XSW
- The access through registers XSA(8:4), capable of storing the information for a complete multiframe
- The access through the up to 128 byte (user) deep XFIFO of the signaling controller (HDLC channel 1 only)

This S_a-bit access gives the opportunity to transparent a bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a-bits which shall be inserted in the outgoing data stream can be selected by XC0.SA(8:4).

4.3.5 Channel Associated Signaling CAS (E1)

The channel associated signaling (CAS) information is carried on the line in time slot 16 (TS16). CAS operation mode of the OctalFALC™ is enabled in E1 mode by setting of register bit XSP.CASEN. Two basic modes can be select for receive and transmit direction independent from another:.

- Serial CAS: If RSIG is configured on one of the receive multifunction ports RPA, RPB or RPC (see **Chapter 3.8**), the received CAS information is given out on RSIG automatically, see **Chapter 4.3.5.1**. The CAS information is also stored in registers RS(16:1) aligned to the CAS multiframe boundary. If XSIG is configured on one of the multifunction ports XPA or XPB, the transmitted CAS information is taken from XSIG automatically and the information in the registers XS(16:1) is ignored, see **Chapter 4.3.5.2**
- Parallel CAS: If RSIG is **not** configured on one of the multifunction ports RPA, RPB or RPC, the received CAS information is stored in registers RS(16:1) aligned to the CAS multiframe boundary, see **Chapter 4.3.5.3**. If XSIG is not configured on one of the multifunction ports XPA or XPB, the transmitted CAS information is taken from the registers XS(16:1), see **Chapter 4.3.5.4**.

4.3.5.1 Serial Receive CAS (E1)

The complete received CAS multiframe is output on pin RSIG. The signaling data is clocked with the working clock of the receive highway (SCLKR) together with the receive synchronization pulse ($\overline{\text{SYPR}}$), see **Chapter 4.6**. Data on RSIG is transmitted in the last 4 bits per time slot and is aligned to the data on RDO. The first 4 bits per time slot can be optionally fixed high or low (SIC2.SSF), except for time slot 0 and 16 (bit 1 to 4 are always "0000" in TS16). In time slot 0 the FAS/NFAS word is transmitted, in time slot 16 the CAS multiframe pattern "0000XYXX". Data on RSIG is only valid if the freeze signaling status is inactive. With FMR1.SAIS an all-ones data stream can be transmitted on RDO and RSIG. The signaling procedure is done as it is described in ITU-T G.704 and G.732. The main functions are:

- Synchronization to a CAS multiframe
- Detection of AIS and remote alarm in CAS multiframes
- Separation of CAS service bits X1 to X3

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a loss-of-signal (FRS0.LOS = ´1´), or a loss of CAS multiframe alignment (FRS1.TSL16LFA = ´1´) or a receive slip occurs. The current freeze status is output on port FREEZE (RPA, RPB or RPC) and indicated by register SIS.SFS. Optionally automatic freeze signaling can be disabled by setting bit SIC3.DAF.

After CAS resynchronization an interrupt is generated. Because at this time the signaling is still frozen, CAS data is not valid yet. Readout of CAS data has to be delayed until the next CAS multiframe is received.

Because the CAS controller is working on the system interface (pcm highway) side of the receive buffer, slips disturb the CAS data.

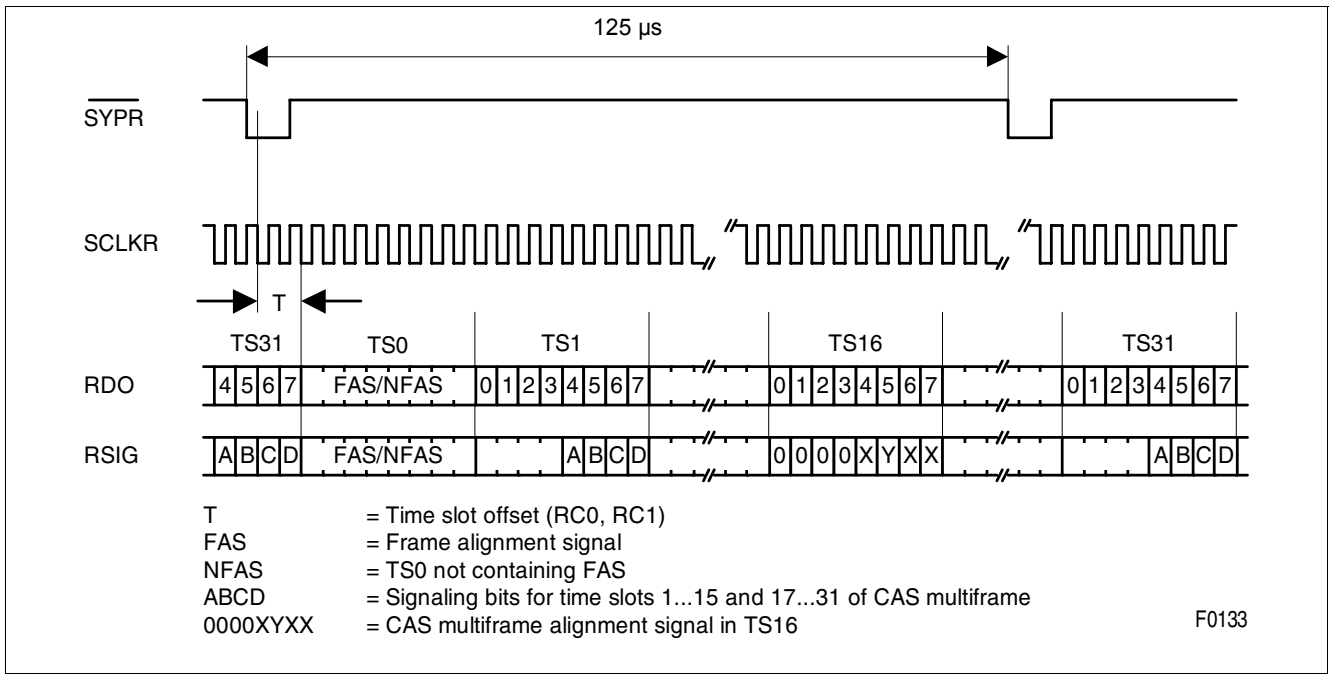


Figure 41 2.048 MHz Receive Signaling Highway (E1)

4.3.5.2 Serial Transmit CAS (E1)

In serial CAS mode the signaling data received on port XSIG is sampled with the working clock of the transmit system interface (SCLKX) in combination with the transmit synchronization pulse ($\overline{\text{SYPX}}$), see **Chapter 4.6**. Data on XSIG is latched in the bit positions 5 to 8 per time slot, bits 1 to 4 are ignored. Time slots 0 and 16 are sampled completely (bit 1 to 8). The received CAS multiframe is inserted frame aligned into the data stream on XDI and must be valid during the last frame of a multiframe if CRC4/multiframe mode is selected. The CAS multiframe is aligned to the CRC4-multiframe; other frames are ignored. Data sourced by the internal signaling controller (µP access mode) overwrites the external signaling data.

If the OctalFALC™ is configured for no signaling, the system interface data stream passes through the OctalFALC™ undisturbed.

Note: CAS data on XSIG is read in the last frame of a multiframe only and ignored in all other frames.

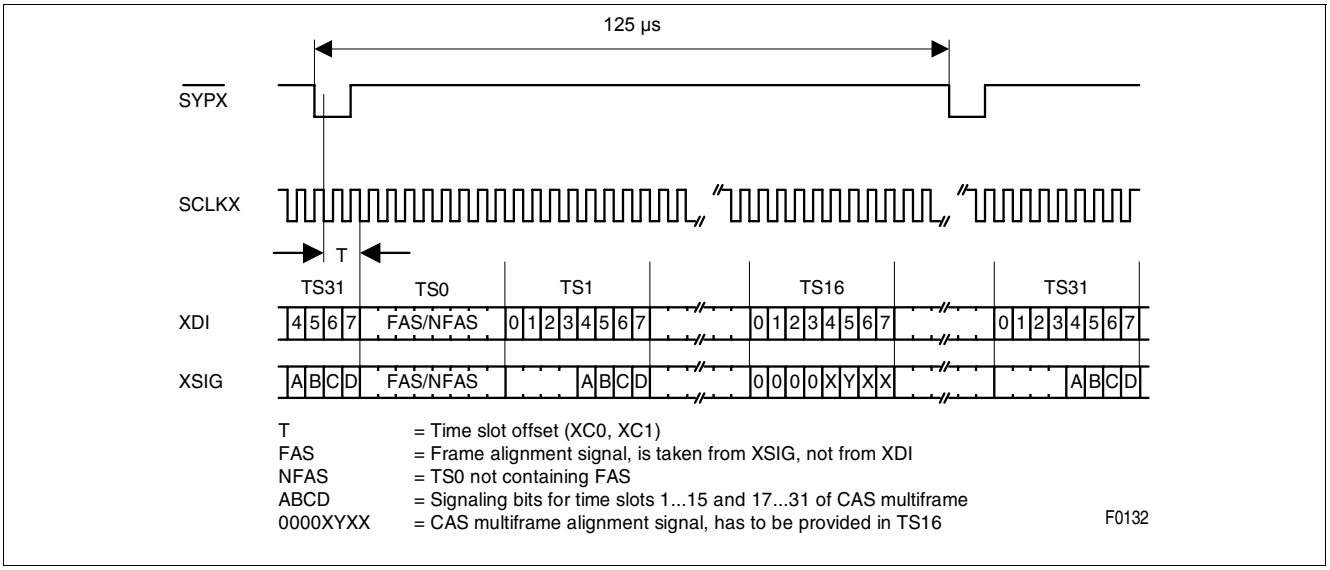


Figure 42 2.048 MHz Transmit Signaling Highway (E1)

4.3.5.3 Parallel Receive CAS (E1)

Received CAS information is stored in registers RS(16:1) (**RS1_E**) aligned to the CAS multiframe boundary. So the CAS information is accessible by the micro controller over the asynchronous, the SPI or the SCI interface.

The signaling procedure is done as it is described in ITU-T G.704 and G.732. The main functions are:

- Synchronization to a CAS multiframe
- Detection of AIS and remote alarm in CAS multiframes
- Separation of CAS service bits X1 to X3
- Storing of received signaling data in registers RS(16:1) with last look capability

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a loss-of-signal (FRS0.LOS = ´1´), or a loss of CAS multiframe alignment (FRS1.TSL16LFA = ´1´) or a receive slip occurs. The current freeze status is output on port FREEZE (RPA, RPB or RPC) and indicated by register SIS.SFS. Optionally automatic freeze signaling can be disabled by setting bit SIC3.DAF. If SIS.SFS is active, updating of the registers RS(16:1) is disabled.

To relieve the micro controller load from always reading the complete RS(16:1) buffer every 2 ms the OctalFALC™ notifies the micro controller through interrupt ISR0.CASC only when signaling changes from one multiframe to the next. Additionally the OctalFALC™ generates a receive signaling data change pointer (RSP(1:2)) which directly points to the updated RS(16:1) register.

Because the CAS controller is working on the system interface (pcm highway) side of the receive buffer, slips disturb the CAS data.

4.3.5.4 Parallel Transmit CAS (E1)

The CAS information is taken from the registers XS(16:1) (**XS1_E**) and is transmitted on a multiframe boundary in time slot 16. So the CAS information is controllable by the micro controller over the asynchronous, the SPI or the SCI interface. The signaling controller inserts the bit stream on the transmit line side.

If the OctalFALC™ is configured for no signaling, the system interface data stream passes the OctalFALC™ undisturbed.

4.4 Framer Operating Modes (E1)

4.4.1 General (E1)

The general parameters are

Bit: FMR1.PMOD	:	0
PCM line bit rate	:	2.048 Mbit/s
Single frame length	:	256 bit, No. 1…256
Framing frequency	:	8 kHz
HDLC controller	:	n x 64 kbit/s, n = 1 to 32 or n x 4 kbit/s, n = 1 to 5
Organization	:	32 time slots, No. 0…31 with 8 bits each, No. 1…8

The operating mode of the OctalFALC™ is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The OctalFALC™ implements all of the standard framing structures for E1 or PCM 30 (CEPT, 2.048 Mbit/s) carriers. The internal HDLC or CAS controller supports all signaling procedures including signaling frame synchronization/synthesis and signaling alarm detection in all framing formats. The time slot assignment from the PCM line to the system highway and vice versa is performed without any changes of numbering (TS0 ↔ TS0, …, TS31 ↔ TS31).

Summary of supported E1 Framing Modes

- Doubleframe format according to ITU-T G. 704
- Multiframe format according to ITU-T G. 704
- CRC4 processing according to ITU-T G. 706
- Multiframe format with CRC4 to non CRC4 interworking according to ITU-T G. 706
- Multiframe format with modified CRC4 to non CRC4 interworking
- Multiframe format with CRC4 performance monitoring

After reset, the OctalFALC™ is switched into doubleframe format automatically. Switching between the framing formats is done by programming bits FMR2.RFS(1:0) and FMR3.EXTIW for the receiver and FMR1.XFS for the transmitter.

4.4.2 Doubleframe Format (E1)

The framing structure is defined by the contents of time slot 0 (refer to **Table 31**).

Table 31 Allocation of Bits 1 to 8 of Time Slot 0 (E1)

Bit Alternate Number Frames	1	2	3	4	5	6	7	8
Frame Containing the Frame Alignment Signal	S_i	0	0	1	1	0	1	1
	1)	Frame Alignment Signal						
Frame not Containing the Frame Alignment Signal or Service Word	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	1)	2)	3)	4)				

1) S_i-bits: reserved for international use. If not used, these bits should be fixed to "1". Access to received information trough bits RSW.RSI and RSP.RSIF. Transmission is enabled by bits XSW.XSIS and XSP.XSIF.

2) Fixed to "1". Used for synchronization.

3) Remote alarm indication: In undisturbed operation "0"; in alarm condition "1".

4) S_a-bits: Reserved for national use. If not used, they should be fixed at "1". Access to received information trough bits RSW.RY0…4. Transmission is enabled by bits XSW.XY0…4. HDLC signaling in bits S_a4 to 8 is selectable. As a special extension for double frame format, the S_a-bit registers RSA4 to 8/XSA4 to 8 can be used optionally.

4.4.2.1 Transmit Transparent Modes (E1)

In transmit direction, contents of time slot 0 frame alignment signal of the outgoing PCM frame are normally generated by the OctalFALC™. However, transparency for the complete time slot 0 can be achieved by selecting the transparent mode XSP.TT0. With the Transparent Service Word Mask register TSWM the S_i-bits, A-bit and the S_a-bits can be selectively switched through transparently.

Table 32 Transmit Transparent Mode (Doubleframe E1)

Transmit Transparent Source for				
Enabled by	**Framing**	**A-Bit**	**S_a-Bits**	**S_i-Bits**
– XSP.TT0 TSWM.TSIF TSWM.TSIS TSWM.TRA TSWM.TSA(8:4)	(int. gen.) via pin XDI[1](int. gen.) (int. gen.) (int. gen.) (int. gen.) (int. gen.)	XSW.XRA[2]via pin XDI XSW.XRA XSW.XRA via pin XDI XSW.XRA	XSW.XY0…4[3]via pin XDI XSW.XY0…4 XSW.XY0…4 XSW.XY0…4 via pin XDI	XSW.XSIS, XSP.XSIF via pin XDI via pin XDI via pin XDI XSW.XSIS, XSP.XSIF XSW.XSIS, XSP.XSIF

1) Pin XDI or XSIG or XFIFO buffer (signaling controller)

2) Additionally, automatic transmission of the A-bit is selectable.

3) As a special extension for double frame format, the S_a-bit register can be used optionally.

4.4.2.2 Synchronization Procedure (E1)

Synchronization status is reported by bit FRS0.LFA. Framing errors are counted by the Framing Error Counter (FEC). Asynchronous state is reached after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (bit 2 = ´0´ in time slot 0 of every other frame not containing the frame alignment word), the selection is done by bit RC0.ASY4. Additionally, the service word condition can be disabled. When the framer lost its synchronization an interrupt status bit ISR2.LFA is generated.

In asynchronous state, counting of framing errors and detection of remote alarm is stopped. AIS is automatically sent to the backplane interface (can be disabled by bit FMR2.DAIS).

Further on the updating of the registers RSW, RSP, RSA(8:4), RSA6S and RS(16:1) is halted (remote alarm indication, S_a/S_i-Bit access).

The resynchronization procedure starts automatically after reaching the asynchronous state. Additionally, it can be invoked user controlled by bit FMR0.FRS (force resynchronization, the FAS word detection is interrupted until the framer is in the asynchronous state. After that, resynchronization starts automatically).

Synchronous state is established after detecting:

- A correct FAS word in frame n,
- The presence of the correct service word (bit 2 = ´1´) in frame n + 1,
- A correct FAS word in frame n + 2.

If the service word in frame n + 1 or the FAS word in frame n + 2 or both are not found searching for the next FAS word starts in frame n + 2 just after the previous frame alignment signal.

Reaching the synchronous state causes a frame alignment recovery interrupt status ISR2.FAR if enabled. Undisturbed operation starts with the beginning of the next doubleframe.

4.4.2.3 A-Bit Access (E1)

If the OctalFALC™ detects a remote alarm indication in the received data stream the interrupt status bit ISR2.RA is set. With setting of bit XSW.XRA a remote alarm (RAI) is sent to the far end.

By setting FMR2.AXRA the OctalFALC™ automatically transmit the remote alarm bit = ´1´ in the outgoing data stream if the receiver detects a loss of frame alignment FRS0.LFA = ´1´. If the receiver is in synchronous state FRS0.LFA = ´0´ the remote alarm bit is reset.

*Note: The A-bit can be processed by the system interface. Setting bit TSWM.TRA enables transparency for the A-bit in transmit direction (refer to **Table 31**).*

4.4.2.4 S_a-Bit Access (E1)

As an extension for access to the S_a-bits through registers RSA(8:4) and XSA(8:4) an option is implemented to allow the usage of internal S_a-bit registers RSA(8:4) and XSA(8:4) in doubleframe format.

This function is enabled by setting FMR1.ENSA = ´1´ for the transmitter and FMR1.RFS(1:0) = ´01_b´ for the receiver. In this case the OctalFALC™ internally works with a 16-frame structure but no CRC multiframe alignment/generation is performed.

4.4.3 CRC-Multiframe (E1)

The multiframe structure shown in **Table 33** is enabled by setting bit: FMR2.RFS(1:0) for the receiver and FMR1.XFS for the transmitter.

Multiframe	:	2 submultiframes = 2 x 8 frames
Frame alignment	:	refer to section Doubleframe Format
Multiframe alignment	:	bit 1 of frames 1, 3, 5, 7, 9, 11 with the pattern "001011_b"
CRC bits	:	bit 1 of frames 0, 2, 4, 6, 8, 10, 12, 14
CRC block size	:	2048 bit (length of a submultiframe)
CRC procedure	:	CRC4, according to ITU-T G.704 and G.706

Table 33 CRC-Multiframe Structure (E1)

	Sub- Multiframe	Frame Number	Bits 1 to 8 of the Frame							
			1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}

E: Spare bits for international use. Access to received information through bits RSP.RS13 and RSP.RS15. Transmission is enabled by register bits XSP.XS13 and XSP.XS15. Additionally, automatic transmission for submultifame error indication is selectable.

S_a: Spare bits for national use. Additionally, S_a bit access through registers RSA(8:4) and XSA(8:4) is provided. HDLC signaling in bits S_a(8:4) is selectable.

C_1 ...C_4: Cyclic redundancy check bits

A: Remote alarm indication. Additionally, automatic transmission of the A-bit is selectable.

For transmit direction, contents of time slot 0 are additionally determined by the selected transparent mode.

Table 34 Transmit Transparent Mode (CRC Multiframe E1)

Transmit Transparent Source for				
Enabled by	**Framing + CRC**	**A-Bit**	**S_a-Bits**	**E-Bits**
–	(int. gen.)	XSW.XRA[2)]	XSW.XY0 … 4[3)]	XSP.XS13/XS15[4)]
XSP.TT0	Via pin XDI[1)]	Via pin XDI	Via pin XDI	Via pin XDI
TSWM.TSIF	Via pin XDI	XSW.XRA[1)]	XSW.XY0 … 4[2)]	(int. generated)
TSWM.TSIS	Via pin XDI	XSW. XRA[1)]	XSW.XY0 … 4[2)]	Via pin XDI
TSWM.TRA	(int. gen.)	Via pin XDI	XSW.XY0 … 4[2)]	XSP.XS13/XS15[3)]
TSWM.TSA(8:4)	(int. gen.)	XSW.XRA[1)]	Via pin XDI	XSP.XS13/XS15[3)]

1) Pin XDI or XSIG or XFIFO buffer (signaling controller)

2) Automatic transmission of the A-bit is selectable

3) The S_a-bit register XSA(8:4) can be used optionally

4) Additionally, automatic transmission of submultiframe error indication is selectable

The CRC procedure is automatically invoked when the multiframe structure is enabled. CRC errors in the received data stream are counted by the 16-bit CRC Error Counter CEC (one error per submultiframe, maximum).

Additionally a CRC4 error interrupt status ISR0.CRC4 is generated if enabled by IMR0.CRC4.

All CRC bits of one outgoing submultiframe are automatically inverted in case a CRC error is flagged for the previous received submultiframe. This function is enabled by bit RC0.CRCI. Setting of bit RC0.XCRCI inverts the CRC bits before transmission to the distant end. The function of RC0.XCRCI and RC0.CRCI are logically ored.

4.4.3.1 Synchronization Procedure (E1)

Multiframe alignment is assumed to have been lost if doubleframe alignment has been lost (flagged on status bit FRS0.LFA). The rising edge of this bit causes an interrupt.

The multiframe resynchronization procedure starts when Doubleframe alignment has been regained which is indicated by an interrupt status bit ISR2.FAR. For Doubleframe synchronization refer to section Doubleframe Format. It is also be invoked by the user by setting

- Bit FMR0.FRS for complete doubleframe **and** multiframe resynchronization
- Bit FMR1.MFCS for multiframe resynchronization only.

The CRC checking mechanism is enabled after the first correct multiframe pattern has been found. However, CRC errors are not counted in asynchronous state.

In doubleframe asynchronous state, counting of framing errors, CRC4 bit errors and detection of remote alarm is stopped. AIS is automatically sent to the backplane interface (can be disabled by bit FMR2.DAIS). Further on the updating of the registers RSW, RSP, RSA(8:4), RSA6S and RS(16:1) is halted (remote alarm indication, S_a/S_i-bit access).

The multiframe synchronous state is established after detecting two correct multiframe alignment signals at an interval of n x 2 ms (n = 1, 2, 3 …). The loss of multiframe alignment flag FRS0.LMFA is reset. Additionally an interrupt status multiframe alignment recovery bit ISR2.MFAR is generated with the falling edge of bit FRS0.LMFA.

4.4.3.2 Automatic Force Resynchronization (E1)

In addition, a search for Doubleframe alignment is automatically initiated if two multiframe pattern with a distance of n x 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained (bit FMR1.AFR). A new search for frame alignment is started just after the previous frame alignment signal.

4.4.3.3 Floating Multiframe Alignment Window (E1)

After reaching doubleframe synchronization a 8 ms timer is started. If a multiframe alignment signal is found during the 8 ms time interval the internal timer is reset to remaining 6 ms in order to find the next multiframe signal within this time. If the multiframe signal is not found for a second time, the interrupt status bit ISR0.T8MS is set. This interrupt usually occurs every 8 ms until multiframe synchronization is achieved.

4.4.3.4 CRC4 Performance Monitoring (E1)

In the synchronous state checking of multiframe pattern is disabled. However, with bit FMR2.ALMF an automatic multiframe resynchronization mode can be activated. If 915 out of 1000 errored CRC submultiframes are found then a false frame alignment is assumed and a search for doubleframe and multiframe pattern is initiated. The new search for frame alignment is started just after the previous basic frame alignment signal. The internal CRC4 resynchronization counter is reset when the multiframe synchronization has been regained.

4.4.3.5 Modified CRC4 Multiframe Alignment Algorithm (E1)

The modified CRC4 multiframe alignment algorithm allows an automatic interworking between framers with and without a CRC4 capability. The interworking is realized as it is described in ITU-T G.706 Appendix B.

If doubleframe synchronization is consistently present but CRC4 multiframe alignment is not achieved within 400 ms it is assumed that the distant end is initialized to doubleframe format. The CRC4/non-CRC4 interworking is enabled by FMR2.RFS(1:0) = ´11_b´ and is activated only if the receiver has lost its synchronization. If doubleframe alignment (basic frame alignment) is established, a 400 ms timer and searching for multiframe alignment are started. A research for basic frame alignment is initiated if the CRC4 multiframe synchronization cannot be achieved within 8 ms and is started just after the previous frame alignment signal. The research of the basic frame alignment is done in parallel and is independent of the synchronization procedure of the primary basic frame alignment signal. During the parallel search all receiver functions are based on the primary frame alignment signal, like framing errors, S_a-, S_i-, A-bits, …). All subsequent multiframe searches are associated with each basic framing sequence found during the parallel search.

If the CRC4 multiframe alignment sequence was not found within the time interval of 400 ms, the receiver is switched into a non-CRC4 mode indicated by setting the bit FRS0.NMF (No Multiframing Found) and ISR2.T400MS. In this mode checking of CRC bits is disabled and the received E-bits are forced to low. The transmitter framing format is not changed. Even if multiple basic FAS resynchronizations have been established during the parallel search, the receiver is maintained to the initially determined primary frame alignment signal location.

However, if the CRC4-multiframe alignment can be achieved within the 400 ms time interval assuming a CRC4-to-CRC4 interworking, then the basic frame alignment sequence associated to the CRC4 multiframe alignment signal is chosen. If necessary, the primary frame alignment signal location is adjusted according to the multiframe alignment signal. The CRC4 performance monitoring is started if enabled by FMR2.ALMF and the received E-bits are processed in accordance to ITU-T G.704.

Switching into the doubleframe format (non-CRC4) mode after 400 ms can be disabled by setting of FMR3.EXTIW. In this mode the OctalFALC™ continues to search for multiframing. In the interworking mode setting of bit FMR1.AFR is not allowed.

4.4.3.6 A-Bit Access (E1)

If the OctalFALC™ detects a remote alarm indication (bit 2 in TS0 not containing the FAS word) in the received data stream the interrupt status bit ISR2.RA is set. With the deactivation of the remote alarm the interrupt status bit ISR2.RAR is generated.

By setting FMR2.AXRA the OctalFALC™ automatically transmits the remote alarm bit = ´1´ in the outgoing data stream if the receiver detects a loss of frame alignment (FRS0.LFA = ´1´). If the receiver is in synchronous state (FRS0.LFA = ´0´), the remote alarm bit is reset in the outgoing data stream.

Additionally, if bit FMR3.EXTIW is set and the multiframe synchronous state cannot be achieved within 400 ms after finding the primary basic framing, the A-bit is transmitted active high to the remote end until the multiframing is found.

*Note: The A-bit can be processed by the system interface. Setting bit TSWM.TRA enables transparency for the A-bit in transmit direction (refer to **Table 33**).*

4.4.3.7 S_a-Bit Access (E1)

Due to signaling procedures using the five S_a-bits (S_{a4}…S_{a8}) of every other frame of the CRC multiframe structure, three possibilities of access by the microprocessor are implemented.

- The standard procedure allows reading/writing the S_a-bit registers RSW, XSW without further support. The S_a-bit information is updated every other frame.
- The advanced procedure, enabled by bit FMR1.ENSA, allows reading/writing the S_a-bit registers RSA(8:4), XSA(8:4).

A transmit or receive multiframe begin interrupt (ISR0.RMB or ISR1.XMB) is provided.

Registers RSA(8:4) contains the service word information of the previously received CRC-multiframe or 8 doubleframes (bit slots 4 to 8 of every service word). These registers are updated with every multiframe begin interrupt ISR0.RMB.

With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of the registers XSA(8:4) is copied into shadow registers. The contents is subsequently sent out in the service words of the next outgoing CRC multiframe (or every doubleframe) if none of the time slot 0 transparent modes is enabled. The transmit multiframe begin interrupt XMB request that these registers issue should be serviced. If requests for new information are ignored, the current contents is repeated.

- The extended access through the receive and transmit FIFOs of the signaling controller. In this mode it is possible to transmit/receive a HDLC frame or a transparent bit stream in any combination of the S_a-bits. Enabling is done by setting of bit CCR1.EITS and the corresponding bits XC0.SA8E to SA4E/TSWM.TSA8 to TSA4 and resetting of registers TTR(4:1), RTR(4:1) and FMR1.ENSA. The access to and from the FIFOs is supported by ISR0.RME, RPF and ISR1.XPR, ALS.

S_a6-Bit Detection According to ETS 300233

Four consecutive received S_a6-bits are checked for the combinations defined by ETS 300233. The OctalFALC™ detects the following fixed Sa6-bit combinations: SA61, SA62, SA63, SA64 = ´1000_b´, ´1010_b´, ´1100_b´, ´1110_b´, ´1111_b´. All other possible 4-bit combinations are grouped to status “X”.

A valid S_a6-bit combination must occur three times in a row. The corresponding status bit in register RSA6S is set. Register RSA6S is of type “clear on read”. Any status change of the S_a6-bit combinations causes an interrupt (ISR0.SA6SC).

During the basic frame asynchronous state update of register RSA6S and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the S_a6-bit combinations can be done either synchronously or asynchronously to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synchronous state (FRS0.LMFA = ´0´). In asynchronous detection mode updating is independent of the multiframe synchronous state.

S_a6-Bit Error Indication Counters

The S_a6-bit error indication counter CRC2L/H (16 bits) counts the received S_a6-bit sequence ´0001_b´ or ´0011_b´ in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors reported from the TE by the S_a6 bit. Incrementing is only possible in the multiframe synchronous state. The S_a6-bit error indication counter CRC3L/H (16 bits) counts the received S_a6-bit sequence ´0010_b´ or ´0011_b´ in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors detected at T-reference point and reporting them by the S_a6-bit. Incrementing is only possible in the multiframe synchronous state.

4.4.3.8 E-Bit Access (E1)

Due to signaling requirements, the E-bits of frame 13 and frame 15 of the CRC multiframe can be used to indicate received errored submultiframes:

Submultiframe I status	E-bit located in frame 13
Submultiframe II status	E-bit located in frame 15

No CRC error: E = 1; CRC error: E = 0

Standard Procedure

After reading the submultiframe error indication RSP.SI1 and RSP.SI2, the microprocessor has to update the contents of register XSP (XS13, XS15). Access to these registers has to be synchronized on transmit or receive multiframe begin interrupts (ISR0.RMB or ISR1.XMB).

Automatic Mode

In the multiframe synchronous state the E-bits are processed according to ITU-T G.704 independently of bit XSP.EBP (E-bit polarity selection).

By setting bit XSP.AXS status information of received submultiframes is automatically inserted in the E-bit position of the outgoing CRC multiframe without any further interventions of the microcontroller.

In the doubleframe and multiframe asynchronous state the E-bits are set or cleared, depending on the setting of bit XSP.EBP.

Submultiframe Error Indication Counter

The EBC (E-Bit) counter EBCL/H (16 bits) counts zeros in the E-bit position of frame 13 and 15 of every received CRC multiframe. This counter option gives information about the outgoing transmit PCM line if the E-bits are used by the remote end for submultiframe error indication. Incrementing is only possible in the multiframe synchronous state.

*Note: E-bits can be processed by the system interface. Setting bit TSWM.TSIS enables transparency for E-bits in transmit direction (refer to **Table 33**).*

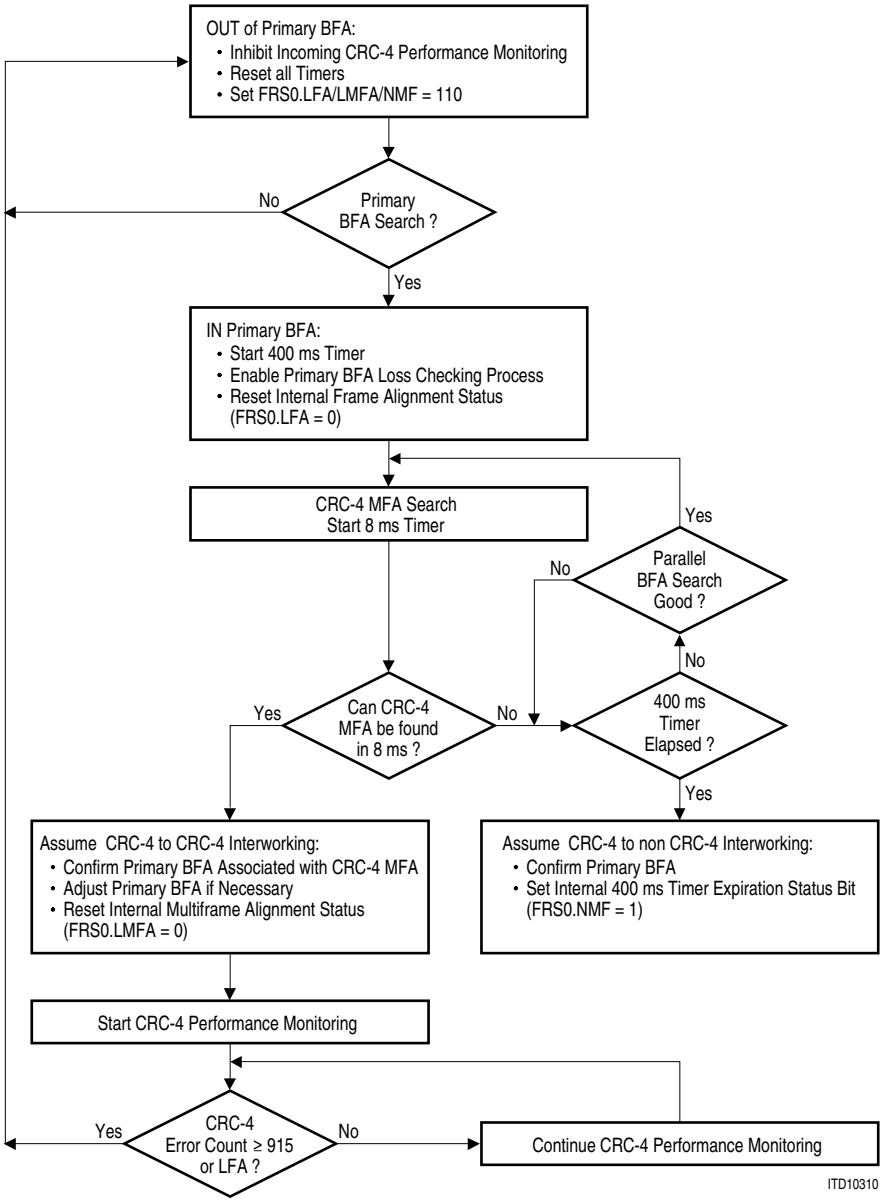


Figure 43 CRC4 Multiframe Alignment Recovery Algorithms (E1)

4.5 Additional Receive Framer Functions (E1)

4.5.1 Error Performance Monitoring and Alarm Handling (E1)

The following error monitoring and alarm handling is supported by the OctalFALC™:

- Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled by bit FMR1.XAIS.
- Loss-Of-Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.
- Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA, RSW.RRA and ISR2.RA/RAR. Transmission is enabled by bit XSW.XRA.
- Remote Defect Indication: In compliance with ITU-T G.775 chapter 6, see **Chapter 4.5.1.1**..

- AIS in time slot 16: Detection and release is flagged by bit FRS1.TS16AIS and ISR3.AIS16. Transmission is enabled by writing all ones in registers XS(16:1).
- LOS in time slot 16: Detection and release is flagged by bit FRS1.TS16LOS. Transmission is enabled by writing all zeros in registers XS(16:1)
- Remote Alarm in time slot 16: Detection and release is flagged by bit FRS1.TS16RA and ISR3.RA16. Transmission is enabled by bit XS1.2
- Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC
- Transmit Ones-Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC

Table 35 Summary of Alarm Detection and Release (E1)

Alarm	Detection Condition	Clear Condition
Loss-Of-Signal (LOS)	No transitions (logical zeros) in a programmable time interval of 16 to 4096 consecutive pulse periods. Programmable receive input signal threshold	Programmable number of ones (1 to 256) in a programmable time interval of 16 to 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold.
Alarm Indication Signal (AIS)	FMR0.ALM = ´0´: less than 3 zeros in 250 µs and loss of frame alignment declared. FMR0.ALM = ´1´: Less than 3 zeros in each of two consecutive 250 µs periods	FMR0.ALM = ´0´: more than 2 zeros in 250 µs. FMR0.ALM = ´1´: More than 2 zeros in each of two 500 µs periods
Remote Defect Indication	"alarm indication to the remote" bit is binary ONE ("1") for z consecutive CAS multiframe periods, where z = 1 ...5. z is not provisionable. "Remote alarm indication" bit is binary ONE ("1") for z consecutive double frame periods, where z = 2,...5. z is not provisionable.	"alarm indication to the remote end" bit is binary ZERO ("0") for z consecutive CAS multiframe periods. "Remote alarm indication" bit is binary ZERO ("0") for z consecutive double frame periods.
Severely Errored Frames (SEF) Indication	Two or more frame bit errors in the timing window are detected.	Signal is in-frame and there are less than two frame bit errors in the timing window
Remote Alarm (RRA)	Bit 3 = ´1´ in time slot 0 not containing the FAS word	Set conditions no longer detected.
Remote Alarm in Time slot 16 (TS16RA)	Y-bit = ´1´ received in CAS multiframe alignment word	Y-bit = ´0´ received in CAS multiframe alignment word
Loss-of-Signal in Time slot 16 (TS16LOS)	All zeros for at least 16 consecutively received time slots 16	Receiving a one in time slot 16
Alarm Indication Signal in time slot 16 (TS16AIS)	Time slot 16 containing less than 4 zeros in each of two consecutive CAS multiframes periods	Time slot 16 containing more than 3 zeros in one CAS multiframe
Transmit Line Short (XLS)	More than 3 pulse periods with highly increased transmit line current on XL1/2	Transmit line current limiter inactive, see also **Chapter 3.7.6**
Transmit Ones-Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

4.5.1.1 Remote Defect Indication RDI (E1)

In E1 mode, Remote Defect Indication (RDI) is performed by the OctalFALC™ in compliance with ITU-T G.775 chapters 6.1 and 6.2 were the criteria for detection and clearance is described, see **Table 35**.

Controlling of the number (z) of multiframe periods or double frame periods is done by the register bits RDICR.RDIS(1:0) and RDICR.RDIC(1:0).

Detection of RDI is shown in the status register bit FRS1.RDI. Note that FRS1.RDI is a status bit, not an interrupt status bit.

4.5.2 Automatic Modes (E1)

In E1 mode the following automatic modes are performed by the OctalFALC™ :

- Automatic remote alarm access: If the receiver has lost its synchronization a remote alarm can be sent automatically, if enabled by bit FMR2.AXRA to the distant end. The remote alarm bit is set automatically in the outgoing data stream, if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is removed.
- Automatic E-bit access: By setting bit XSP.AXS status information of received submultiframes is automatically inserted at the E-bit position of the outgoing CRC Multiframe without any further interventions of the microprocessor.
- Automatic AIS to system interface: In asynchronous state the synchronizer enforces an AIS to the receive system interface automatically. However, received data can be switched through transparently, if bit FMR2.DAIS is set.
- Automatic clock source switching (see also : In slave mode (LIM0.MAS = ´0´) the DCO-R synchronizes to the recovered route clock. In case of loss-of-signal (LOS) the DCO-R switches to Master mode automatically. If bit CMR1.DCS is set, automatic switching from the recovered route clock to SYNC is disabled. See also **Table 16**.
- Automatic transmit clock switching, see **Chapter 3.7.3**.
- Automatic freeze signaling: Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a loss-of-signal or a loss of CAS multiframe alignment or a receive slip occurs. The internal signaling buffer RS(16:1) is frozen. Optionally automatic freeze signaling is disabled by setting bit SIC3.DAF.
- Automatic local and remote loop switching based on In-Band loop codes, see **Chapter 4.5.6**.

4.5.3 Error Counter (E1)

The OctalFALC™ offers six error counters where each of them has a length of 16 bit. They record code violations, framing bit errors, CRC4-bit errors and CRC4 error events which are flagged in the different S_a6-bit combinations or the number of received multiframes in asynchronous state or the change of frame alignment (COFA). Counting of the multiframes in the asynchronous state and the COFA parameter is done in a 6/2 bit counter and is shared with CEC3L/H. Each of the error counters is buffered. Buffer updating is done in two modes:

- One-second accumulation
- On demand by handshake with writing to the DEC register

In the one-second mode an internal/external one-second timer updates these buffers and resets the counter to accumulate the error events in the next one-second period. The error counter cannot overflow. Error events occurring during an error counter reset are not lost.

4.5.4 Errored Second (E1)

The OctalFALC™ supports the error performance monitoring by detecting the following alarms or error events in the received data: framing errors, CRC errors, code violations, loss of frame alignment, loss-of-signal, alarm indication signal, E-bit error, receive and transmit slips. With a programmable interrupt mask register ESM all these alarms or error events can generate an errored second interrupt (ISR3.ES) if enabled.

4.5.5 One-Second Timer (E1)

A one-second timer interrupt can be generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The one-second timer signal is output on port SEC/FSC if coonfigured by

GPC1.CSFP(1:0) (GPC1_E). Optionally synchronization to an external second timer is possible which has to be provided on pin SEC/FSC. Selecting the external second timer is done with GCR.SES.

In compatibility mode of the OctalFALC™ (pin COMP = ´1´) the register GPC1 (global port configuration register 1) is used in every of the both pseudo QuadFALC® s to configure the sources of FSC out of the 4 channels. So with these one GPC1 register per pseudo QuadFALC® its only possible to control a 4:1 multiplexer. Due to the fact that there are eight channels in the OctalFALC™ a 8:1 multiplexing is necessarry to control the source channel of the FSC/SEC pin. **Figure 70** shows the principle of the solution using an additional 2:1 multiplexer.

The 2:1 multiplexer is controlled by the register bits GPC1.CSFP(1:0) of the second Pseudo QuadFALC®: If the SEC/FSC pin is configured as output by these bits, the second Pseudo QuadFALC® is the source of SEC/FSC. Enable of the SEC/FSC pin as output is performed by the register bits GPC1.CSFP(1:0) of the first and the second Pseudo QuadFALC® were all are logical ored..

For COMP = ´0´ the global GPC2 register is used instead of the both GPC1 registers in compatibility mode.

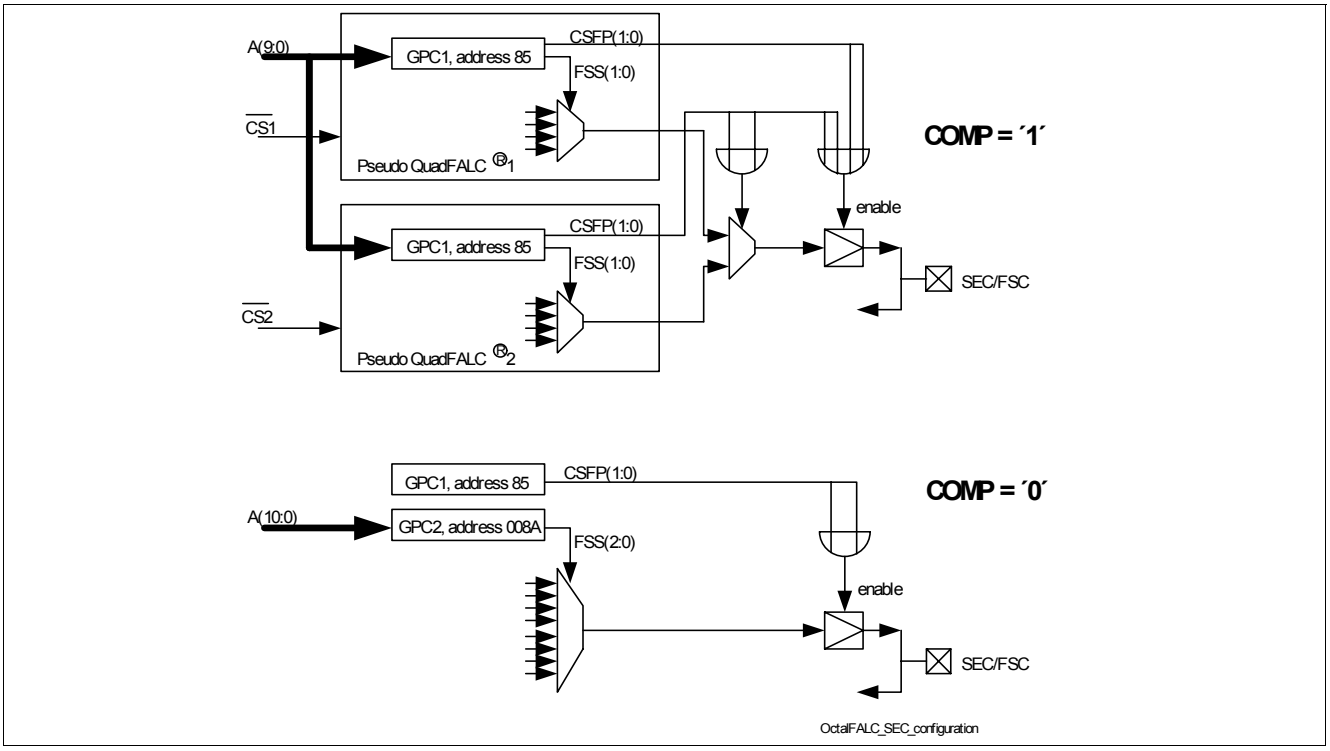


Figure 44 Principle of Configuring the SEC/FSC Pin

4.5.6 In-Band Loop Generation, Detection and Loop Switching (E1)

In-band Signaling is an unchannelized signaling method. All data bits of all time slots of a frame can be used by the In-band signaling information.

Detection and generation of In-band Loop code is supported by the OctalFALC™ on the line side and on the system side independent from another.

The OctalFALC™ generates and detects framed or unframed In-band codes. The so called loop-up code (for loop activation) and loop-down code (for loop deactivation) are recognized. If the 1. bit of a frame (frame bit) is used for In-Band signaling it is the so called “unframed” signaling, otherwise it is called “framed” signaling. The selection between framed or unframed in-band loop code is done by LCR1.FLLB.

The maximum allowed bit error rate within the loop codes can be up to 10^{-2} for proper detection of the loop codes. One “In-band loop sequence” consists of a bitsequence of 51200 consequtive bits. The In-band loop code detection is based on the examination of such “In-band loop sequences”.

The following In-band loop code functionality is performed by the OctalFALC™:

- The necessary reception time of In-band loop codes until an automatic loop switching is performed is configured for the system side by the register bits INBLDTR.INBLDT(1:0) (**INBLDTR_E**). Configuring for the line side is done by INBLDTR.INBLDR(1:0). If for example INBLDTR.INBLDR(1:0) = ´00_b´ a time of 16 “In-band loop sequences” (16 x 51200 bits) is selected for the line side.
- The interrupt status register bits ISR6.(3:0) reflects the type of detected In-band loop code. Masking can be done by IMR6(3:0). The status bits are set after one “In-band loop sequence” is detected (no dependency on INBLDTR).
- Transmission of In-Band loop codes is enabled by programming FMR3.XLD/XLU. Transmission of codes is done by the OctalFALC™ for at least 5 seconds.
- The OctalFALC™ also offers the ability to generate and detect user defined In-band loop-up and loop-down patterns (LCR1.LLBP = ´1´) (**LCR1_E**). Programming of these patterns is done in registers LCR2 and LCR3 (**LCR3_E**). The pattern length is individually programmable in length from 5to 8 bits by LCR1.LAC(1:0) and LCR1.LDC(1:0). A shorter pattern can be inplemented by configuring a repeating pattern in the LCR2 and LCR3.
- Automatic loop switching (activation and deactivation, for remote loop, see **Chapter 4.7.2** and local loop, see **Chapter 4.7.4**) based on In-band Loop codes can be done. Two kinds of line loop back (LLB) codes are defined in ANSI-T1.403, 1999 in chapter 9.4.1.1 and 9.4.1.2. respectively. Automatic loop switching must be enabled through configuration register bits ALS.SILS for the In-Band Loop codes coming from the system side and ALS.LILS for the In-Band Loop codes coming from the line side respecively. Masking of ISR6.(3:0) for interrupt can be done by register bits IMR6.(3:0). The interrupt status register bits ISR6.(3:0) (**ISR6_E**) will be set to ´1´ if an appropriate In-Band code were detected, independent if automatic loop switching is enabled. (Because the controller knows if automatic loop switching is enabled, it knows if a loop is activated or not.) Code detection status only for the line side is displayed in status register bits RSP.LLBDD and RSP.LLBAD.

Detection and generation of In-Band Loop code is supported on line and system side independent from each other.

Framed and unframed In-Band loop code can be generated and detected.

Automatic loop switching is logically OR´d with the appropriate loop switching by register bits.

If a remote loop is activated by an automatic loop switching the register bit LIM0.JATT controls also if the jitter attunator is active or not, see also **Figure 31**.

If ALS.LILS is set (**ALS_E**), the remote loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) is detected from the line side and if the local loop is not activated by LIM0.LL = ´1´. The remote loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) is detected from the line side. (But if the remote loop is addtionally activated by LIM0.RL = ´1´ the remote loop is still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

If ALS.SILS is set, the local loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) is detected from the system side. The local loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) is detected from the system side. (But if the local loop is addtionally activated by LIM0.LL = ´1´ the local loop will be still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

ALS.SILS and ALS.LILS both must not be set to ´1´ simultaneous.

If ALS.SILS or ALS.LILS are set after an In-Band loop code was detected, no automatic loop switching is performed.

If ALS.LILS is cleared, an automatic activated remote loop is deactivated..

If ALS.SILS is cleared, an automatic activated local loop is deactivated.

The kind of detected In-Band loop code is indicated in the interrupt status register bits ISR6.(3:0).

To avoid lock up of the OctalFALC™ an activation of the remote loop is not possible by In-band loop codes if the local loop (see **Chapter 4.7.4**) is closed (LIM0.LL is set).

4.5.7 Time Slot 0 Transparent Mode (E1)

The transparent modes are useful for loop-backs or for routing data unchanged through the OctalFALC™.

In receive direction, transparency for ternary or dual-/single-rail unipolar data is always achieved if the receiver is in the synchronous state. In asynchronous state data is transparently switched through if bit FMR2.DAIS is set.

However, correct time slot assignment cannot be guaranteed due to missing frame alignment between line and system side. Setting of bit LOOP.RTM disconnects control of the internal elastic store from the receiver. The elastic buffer is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of resynchronization of the receiver. Together with FMR2.DAIS this function can be used to realize undisturbed transparent reception.

Transparency in transmit direction can be achieved by activating the time slot 0 transparent mode (bit XSP.TT0 or TSWM.(7:0)). If XSP.TT0 = ´1´ all internal information of the OctalFALC™ (framing, CRC, S_a/S_i-bit signaling, remote alarm) is ignored. With register TSWM the S_i-bits, A-bit or the S_a-bits can be enabled selectively to send data transparently from port XDI to the far end. For complete transparency the internal signaling controller, idle code generation and AIS alarm generation, single channel and payload loop-back have to be disabled.

4.6 System Interface in E1 Mode

The OctalFALC™ offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The system interface of the OctalFALC™ consists of

- The eight system interfaces of the eight channels, see **Figure 45**. It also includes the multi function ports, see **Chapter 3.8** .
- The system interface multiplexer/demultiplexer, see **Chapter 4.6.1** with **Figure 46**: It multiplexes the data RDO and RSIG received from four or eight channels into one or two common data streams and it demultiplexes the data XDI and XSIG from one or two common data streams into four or eight channels.

Configuring of the system interface consists on

- Configuration of the timing of the system interfaces of the eight channels, see **Chapter 4.6.2** and **Chapter 4.6.3**
- Configuration of the multi function ports of the eight channels, see **Chapter 3.8**
- Configuration of the multiplex mode of the system multiplexer/demultiplexer, see **Chapter 4.6.1**.

The interfaces of every of the channels to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The interfaces of every of the channels to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The receive highway is clocked on pin SCLKR, while the interface to the transmit system highway is independently clocked either on pin SCLKX or on the clock of the receive highway. The frequency of these working clocks - so called as “internal receive clock” and “internal transmit clock” - and the data rate of 2.048/4.096/8.192/16.384 Mbit/s for the receive and transmit system interface is programmable by SIC1.SSC(1:0), and SIC1.SSD1, FMR1.SSD0. If the source of the internal receive clock is the DCO-R output or the recovered receive clock, SCLKR must be configured as output by setting PC5.CSRP. If the source is SCLKR, these pin must be configured as input. Selectable system clock and data rates and their valid combinations are shown in the table below.

Table 36 System Clocking and Data Rates (E1)

System Highway Data Rate	System Interface Clock Rate 2.048 MHz	System Interface Clock Rate 4.096 MHz	System Interface Clock Rate 8.192 MHz	System Interface Clock Rate 16.384 MHz
2.048 Mbit/s	x	x	x	x
4.096 Mbit/s	--	x	x	x
8.192 Mbit/s	--	--	x	x
16.384 Mbit/s	--	--	--	x

x = valid, -- = invalid

Generally the receive/transmit data and marker on the system interface are clocked off/latched on on the rising or falling edge of the SCLKR/SCLKX clock:

- Selection of the edge for the receive/transmit data and marker is done by the register bits SIC3.RESR/X (**SIC3_E**).

- Selection of the edge for the sync pulses $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ in relation to the edge of the receive/transmit data and marker can be done individually by the register bits SIC4.SYPRCE/SYPXCE (**SIC4_E**): Either the same edge or the opposite edge in relation to the used edge of the data and markers is possible.

Some clocking rates allow transmission of time slots in different channel phases. Each channel phase which shall be active on ports RDO, XDI, RP(A:C) and XP(A:B) is programmable by SIC2.SICS(2:0) (**SIC2_E**), the remaining channel phases are cleared or ignored.

The signals on pin $\overline{\text{SYPR}}$ together with the assigned time slot offset in register RC0 and RC1 define the beginning of a frame on the receive system highway.The signal on pin $\overline{\text{SYPX}}$ or XMFS together with the assigned time slot offset in register XC0 and XC1 define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ or XMFS is possible in the range of 0 to 125 µs. The minimum shift of varying the time slot 0 begin can be programmed between 1 bit and 1/8 bit depending of the system clocking and data rate, e.g. with a clocking/data rate of 2.048 MHz shifting is done bit by bit, while running the OctalFALC™ with 16.384 MHz and 2.048 Mbit/s data rate it is done by 1/8 bit.

A receive frame marker RFM can be activated during any bit position of the entire frame. The pin function RFM is selected by PC(3:1).RPC(3:0) = ´0001_b´. The RFM selection disables the internal time slot assigner, no offset programming is performed. The receive frame marker is active high for one 2.048 MHz cycle and is clocked off with the rising or falling edge of the clock which is in/output on port SCLKR (see SIC3.RESR/X).

Compared to the receive path the inverse functions are performed for the transmit direction.

Latching of XDI and XSIG is controlled by the system clock (SCLKX) and the synchronization pulse ($\overline{\text{SYPX}}$/XMFS) in combination with the programmed offset values for the transmit time slot/clock slot counters XC(1:0). The frequency of the working clock of 2.048/4.096/8.192/16.384 MHz for the transmit system interface is programmable by SIC1.SSC(1:0) (**SIC1_E**). Refer also to **Table 36**.

The incoming bit stream on ports XDI and XSIG can be multiplexed internally on a time slot basis, if enabled by SIC3.TTRF = ´1´. The data received on port XSIG can be sampled if the transmit signaling marker XSIGM is active high. Data on port XDI is sampled if XSIGM is low for the corresponding time slot. Programming the XSIGM marker is done with registers TTR(4:1).

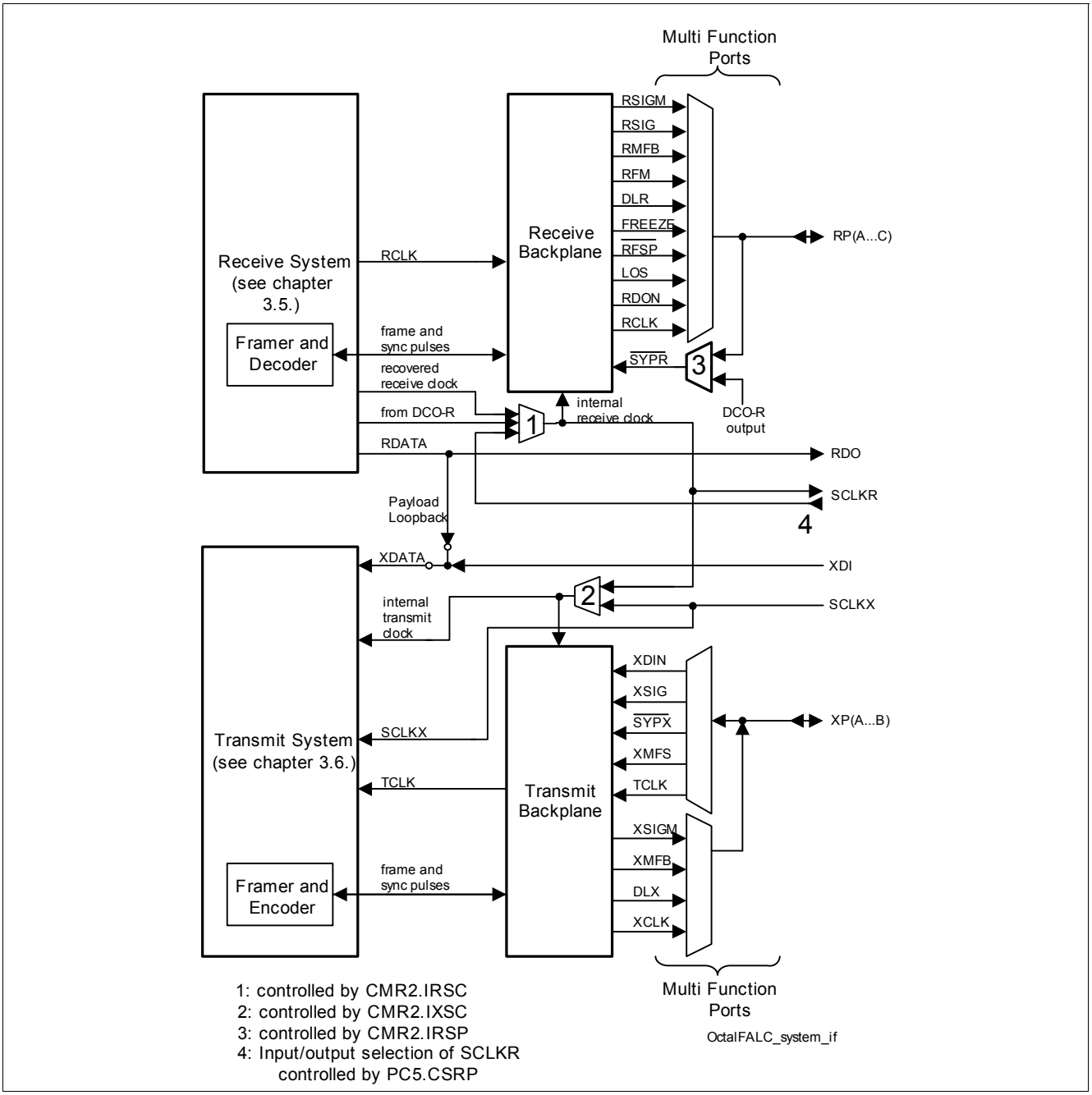


Figure 45 System Interface of one Channel

4.6.1 System Multiplexer/Demultiplexer (E1)

The system multiplexer/demultiplexer of the OctalFALC™ is shown in **Figure 46**.

In receive direction multiplexing of the received data RDO(1:8) of the eight channels into either two data streams at RDO1 and RDO5 or into one data stream at RDO1 is performed. In the same way the signals RSIG(1:8) are multiplexed either into two signaling streams using the multi function ports RPB1, and RPB5 or into one signaling stream using RPB1.

In transmit direction demultiplexing either from two data streams at XDI1 and XDI5 or from one data stream at XDI1 onto the transmit data XDI(1:8) of the eight channels is performed. In the same way multiplexing either from two signaling streams using the multi function ports XPB1,5 or from one signaling stream using XPB1 onto the signals XSIG(1:8) is performed.

All other signals which are configured at the multi function ports were not multiplexed/demultiplexed, see **Figure 46**.

The following modes are supported, see **Table 37** and **Figure 47** where only the pins RDO are shown.

- 8-to-1 Multiplex Mode at 16 Mbit/s. Multiplexing is done on port 1 (RPB1, XPB1). Output pins of the other ports are set to tristate input pins of the other ports are unused .
- Dual 4-to-1 Multiplex Mode at 8 Mbit/s. Multiplexing is done on port 1 (RPB1, XPB1) and port 5 (RPB5, XPB5). Output pins of the other ports are undefined, input pins of the other ports are unused.
- Dual 4-to-1 Multiplex Mode at 16 Mbit/s. Multiplexing is done on port 1 and port 5 where four phases are unused on every port. Disjunct phases must be used on both ports. 16 Mbit/s multiplexing is done by external logical or on the PCB. Output RDO is driven to low level for inactive phases. Output pins of the other ports are undefined, input pins of the other ports are unused.

Switching into Multiplex Modes is done by setting of the register bit GPC1.SMM.

Switching between 8-to-1 Multiplex Mode (using only one port) and QuadFALC® compatible 4:1 Multiplex Modes (using two or more ports) is done by the register bit GPC6.SSI16 (**GPC6_E**)..

Multiplexing of RSIG is done in the same way as shown for RDO in **Figure 47** . Demultiplexing of XDI and XSIG is done vice versa.

To perform the system interface mode the following configuration of the multi function ports must be identical for all channels.

- SYPR has to be provided on RPA (PC1.RPC(3:0) = ´0000_b´).
- SYPX or XMFS has to be provided on XPA (PC1.XPC(3:0) = ´0000_b´).
- XSIG has to be provided on XPB (PC2.XPC(3:0) = ´0010_b´).
- RSIG must be output on RPB (PC2.RPC(3:0) = ´0100_b´).

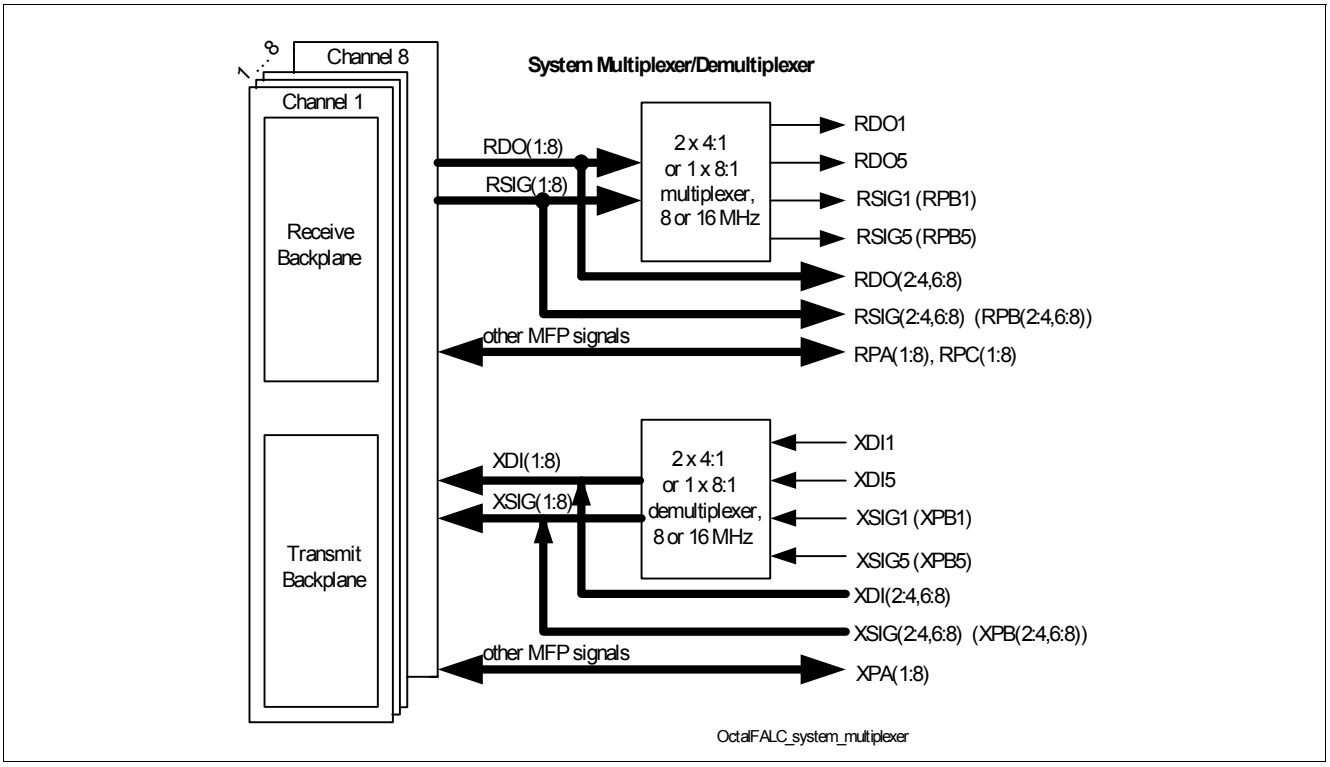


Figure 46 System Multiplexer/Demultiplexer

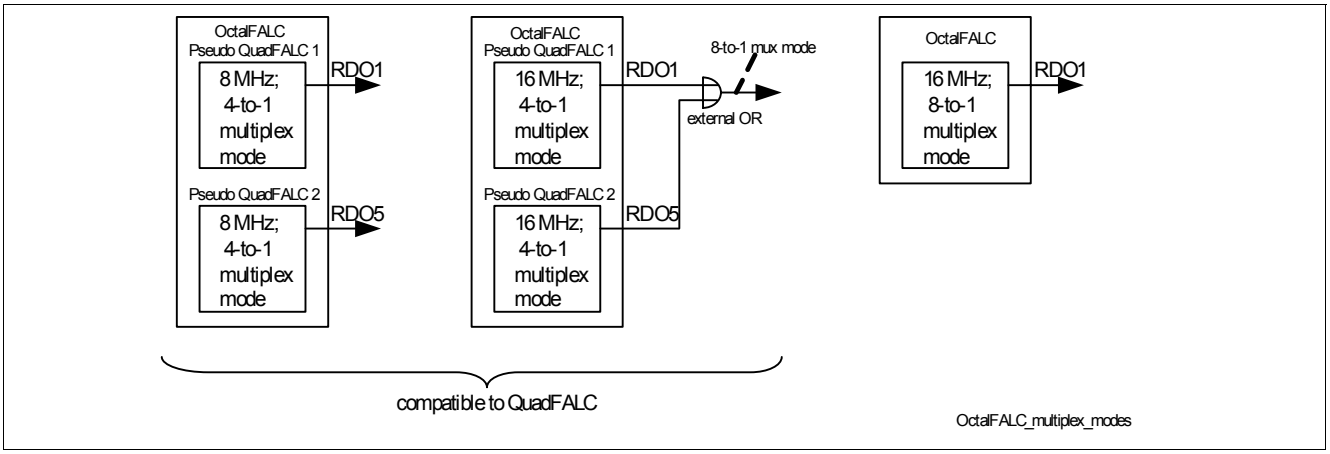


Figure 47 System Multiplexe Modes, shown for RDO only

Table 37 System Multiplex Modes

GPC1.SMM	GPC6.SSI16	Multiplex Mode
0	0	No multiplexing/demultiplexing
0	1	Not defined
1	0	4:1 multiplexing/demultiplexing with 8.192 Mbit/s or 16.364 Mbit/s dependent on SIC1.SSD1 and SIC1.SSC(1:0) For COMP = ´1´: setting of 4:1 multiplexing/demultiplexing can be done individually in both pseudo QuadFALC® s dependent on the both GPC1.SMM bits. For COMP = ´0´: 4:1 multiplexing/demultiplexing is performed in both of the pseudo QuadFALC® s dependent on the one GPC1.SMM bit
1	1	8:1 multiplexing/demultiplexing with 16.384 Mbit/s For COMP = ´1´: GPC1.SMM bits of both pseudo QuadFALC® s must be set to ´1. (for COMP = ´0´: only the one GPC1.SMM bit must be set)

4.6.2 Receive System Interface (E1)

The timing of the receive system interface is shown in **Figure 48**.

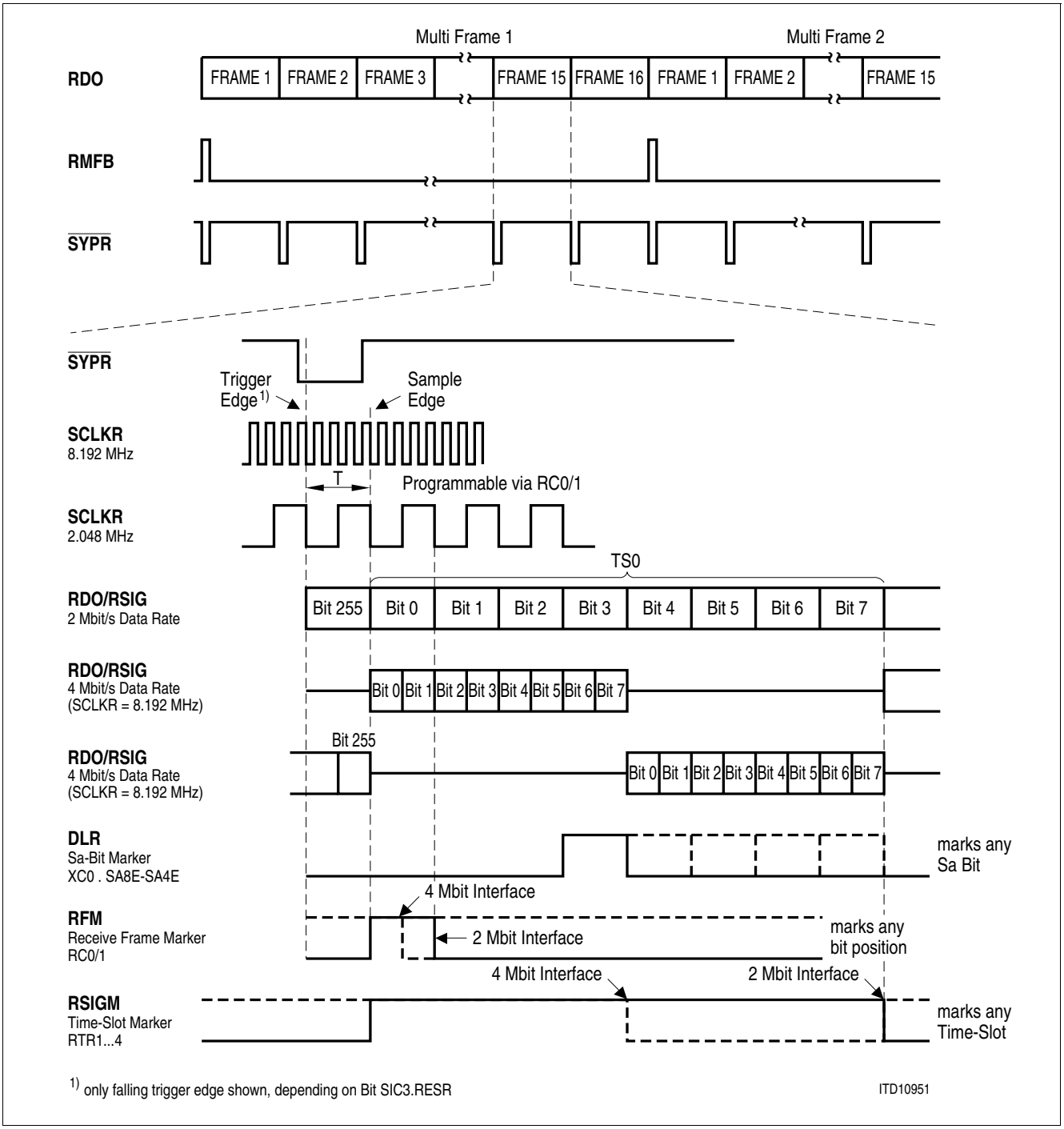


Figure 48 Receive System Interface Clocking of one Channel (E1)

4.6.2.1 Receive Offset Programming (E1)

Depending on the selection of the synchronization signals ($\overline{\text{SYPR}}$ or RFM), different calculation formulas are used to define the position of the synchronization pulses. These formulas are given below, see **Figure 54** to **Figure 52** for explanation. The pulse length of RFM is always the basic E1 bit width (488 ns), independent of the selected system highway clock and data frequency. The figures and offset calculations are valid for SIC4.SYPRCE = ´0´.

$\overline{\text{SYPR}}$ Offset Calculation

T : Time between beginning of $\overline{\text{SYPR}}$ pulse and beginning of next frame (time slot 0, bit 0), measured in number of SCLKR clock intervals maximum delay: T_{max} = (256 ° SC/SD) - 1

SD : Basic data rate; 2.048 Mbit/s

SC : System clock rate; 2.048, 4.096, 8.192, or 16.384 MHz

X : Programming value to be written to registers RC0 and RC1 (see Page 239).

$0 \leq T \leq 4$: X = 4 - T

$5 \leq T \leq T_{max}$: X = 2052 - T

RFM Offset Calculation

MP : Marker position of RFM, counting in SCLKR clock cycles (0 = bit 1, time slot 0, channel phase 0)
SC = 2.048 MHz: $0 \leq MP \leq 255$
SC = 4.096 MHz: $0 \leq MP \leq 511$
SC = 8.192 MHz: $0 \leq MP \leq 1023$
SC = 16.384 MHz: $0 \leq MP \leq 2047$

SD : Basic data rate; 2.048 Mbit/s

SC : System clock rate; 2.048, 4.096, 8.192, or 16.384 MHz

X : Programming value to be written to registers RC0 and RC1 (see Page 239).

$0 \leq MP \leq 2045$: X = MP + 2

$2046 \leq MP \leq 2047$: X = MP - 2046

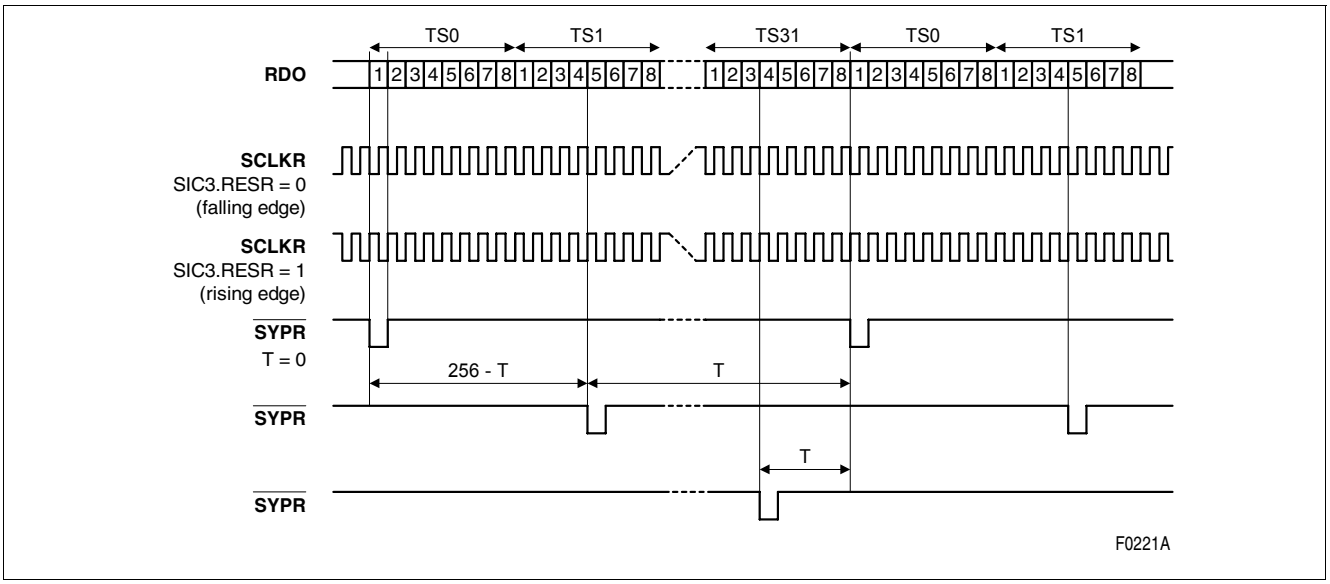


Figure 49 $\overline{\text{SYPR}}$ Offset Programming (2.048 Mbit/s, 2.048 MHz)

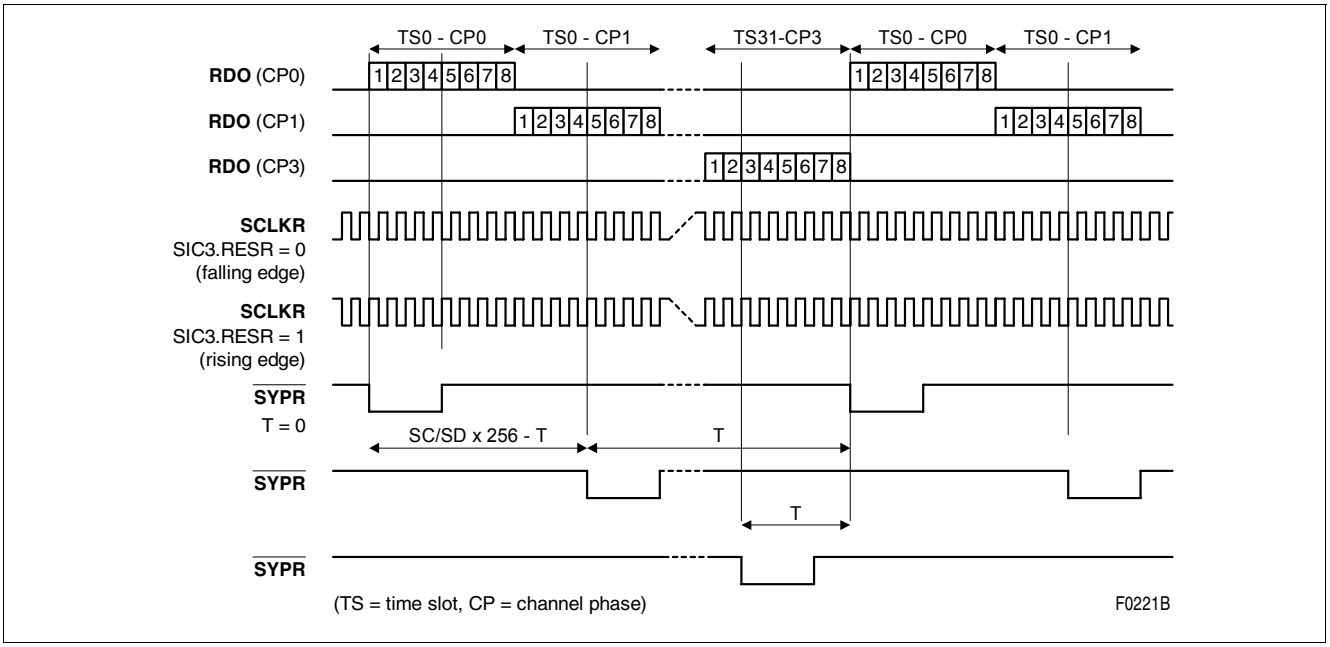


Figure 50 $\overline{\text{SYPR}}$ Offset Programming (8.192 Mbit/s, 8.192 MHz)

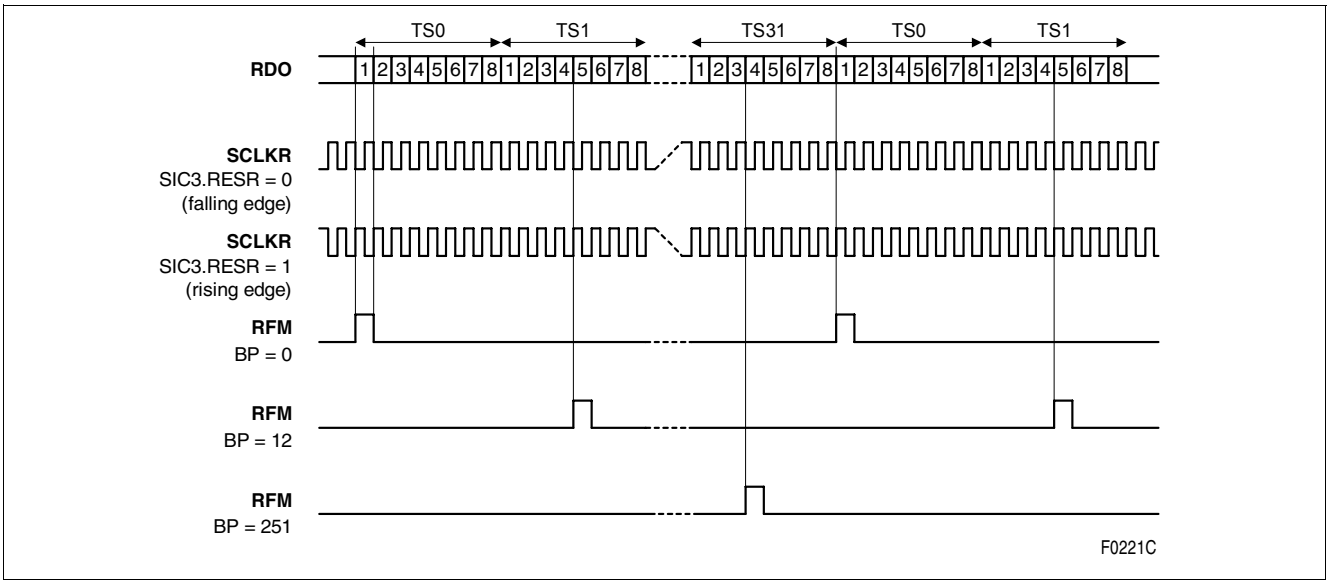


Figure 51 RFM Offset Programming (2.048 Mbit/s, 2.048 MHz)

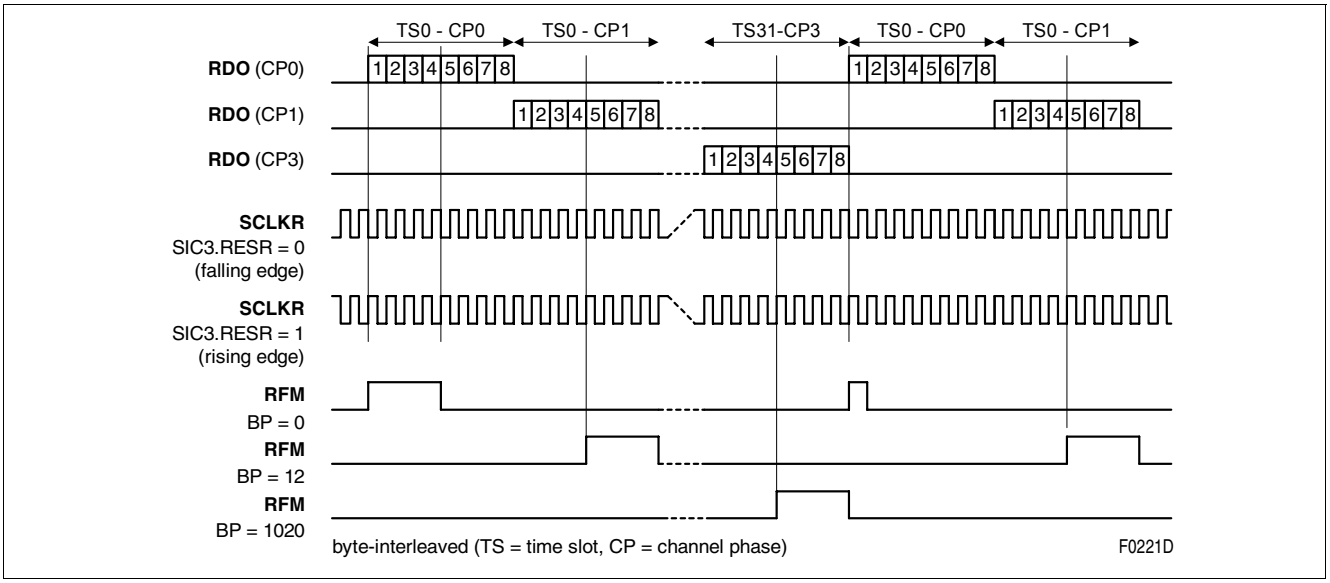


Figure 52 RFM Offset Programming (8.192 Mbit/s, 8.192 MHz)

4.6.3 Transmit System Interface (E1)

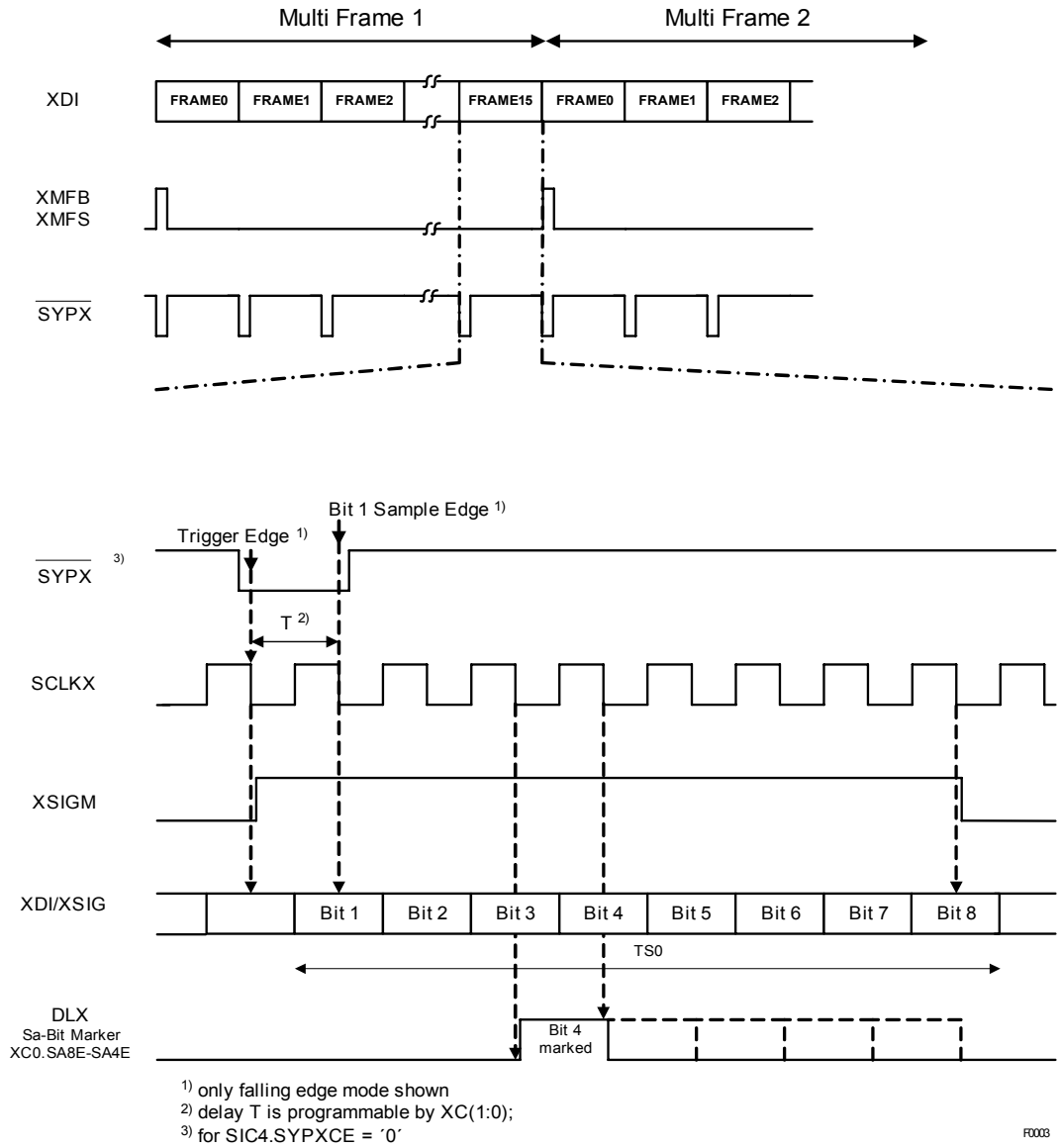


Figure 53 Transmit System Interface Clocking: 2.048 MHz (E1)

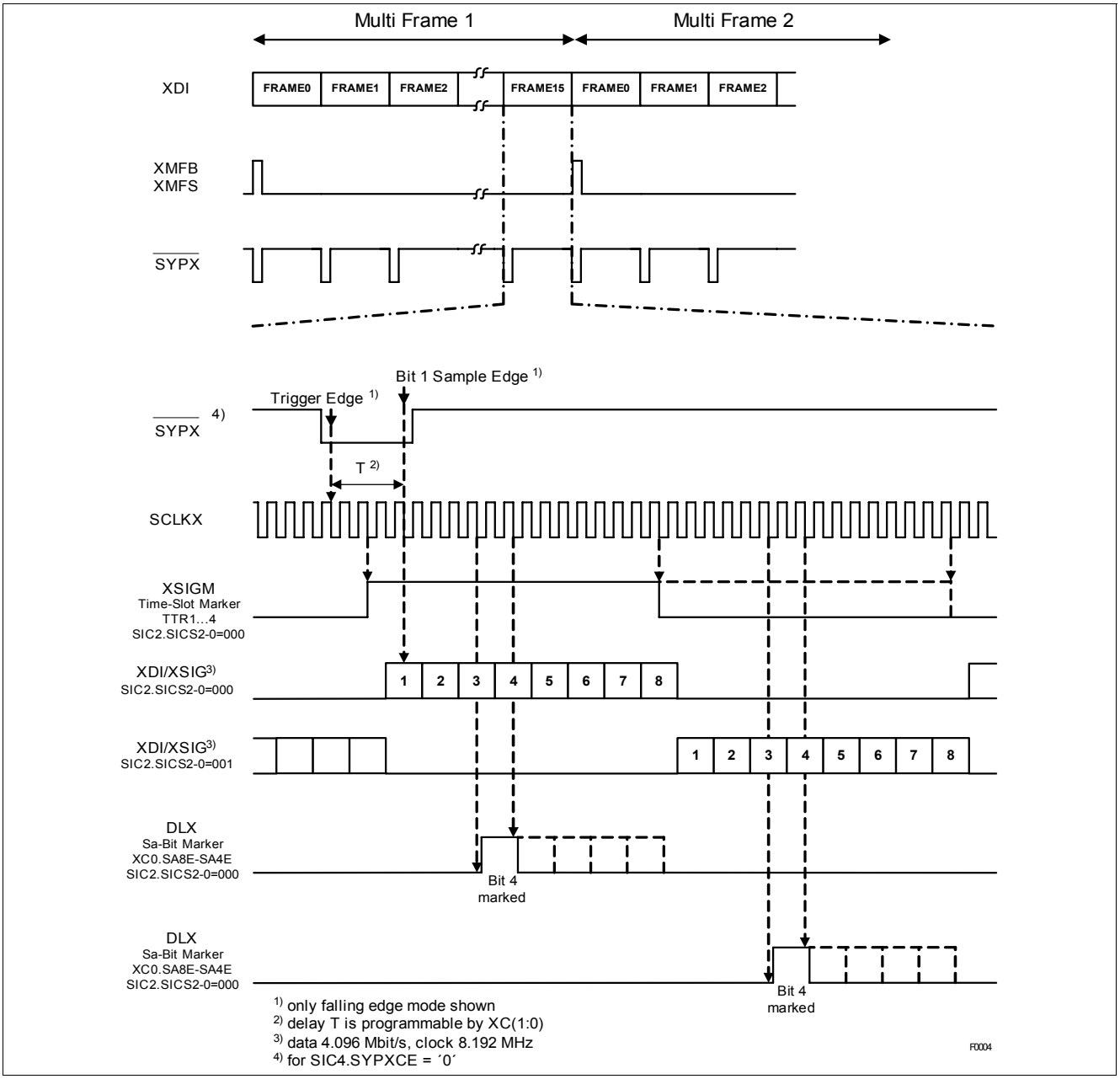


Figure 54 Transmit System Interface Clocking: 8.192 MHz/4.096 Mbit/s (E1)

4.6.3.1 Transmit Offset Programming (E1)

The figures and calculated offsets are valid for SIC4.SYPXCE = ´0´.

$\overline{\text{SYPX}}$ Offset Calculation

T : Time between beginning of $\overline{\text{SYPX}}$ pulse and beginning of next frame (time slot 0, bit 0), measured in number of SCLKX clock intervals maximum delay: T_{max} = (256 ° SC/SD) - 1

SD : Basic data rate; 2.048 Mbit/s

SC : System clock rate; 2.048, 4.096, 8.192, or 16.384 MHz

X : Programming value to be written to registers XC0 and XC1 (see Page 237).

$0 \leq T \leq 4$: $X = 4 - T$

$5 \leq T \leq T_{max}$: $X = 256 \circ SC/SD - T + 4$

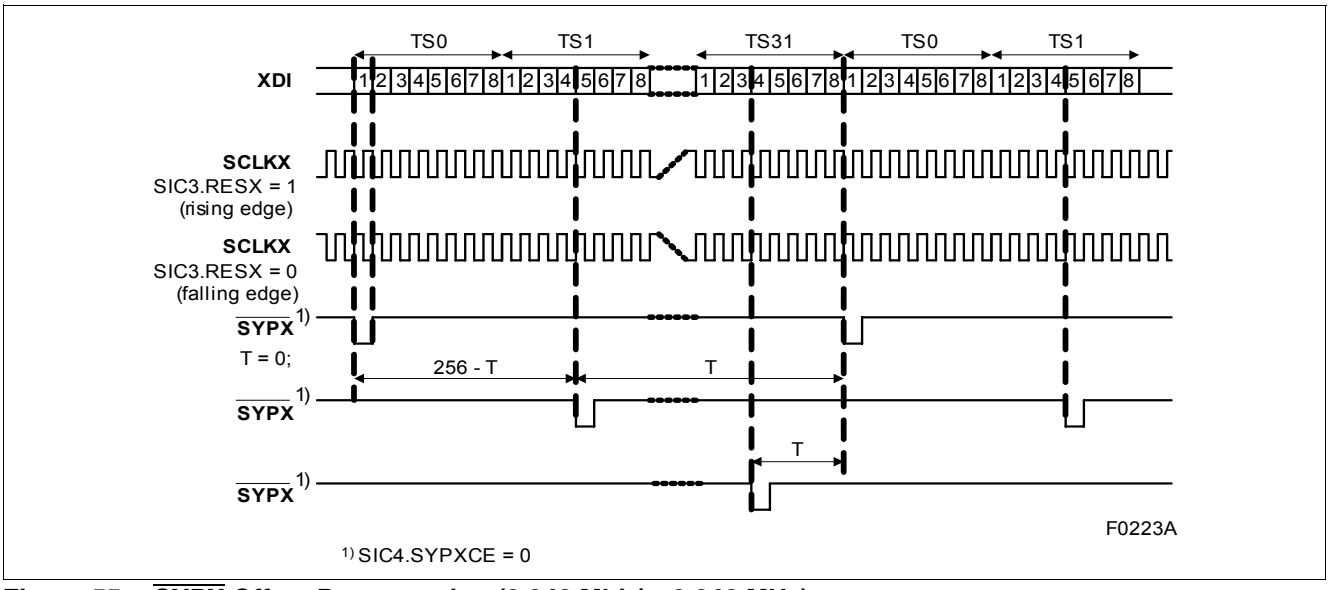


Figure 55 $\overline{\text{SYPX}}$ Offset Programming (2.048 Mbit/s, 2.048 MHz)

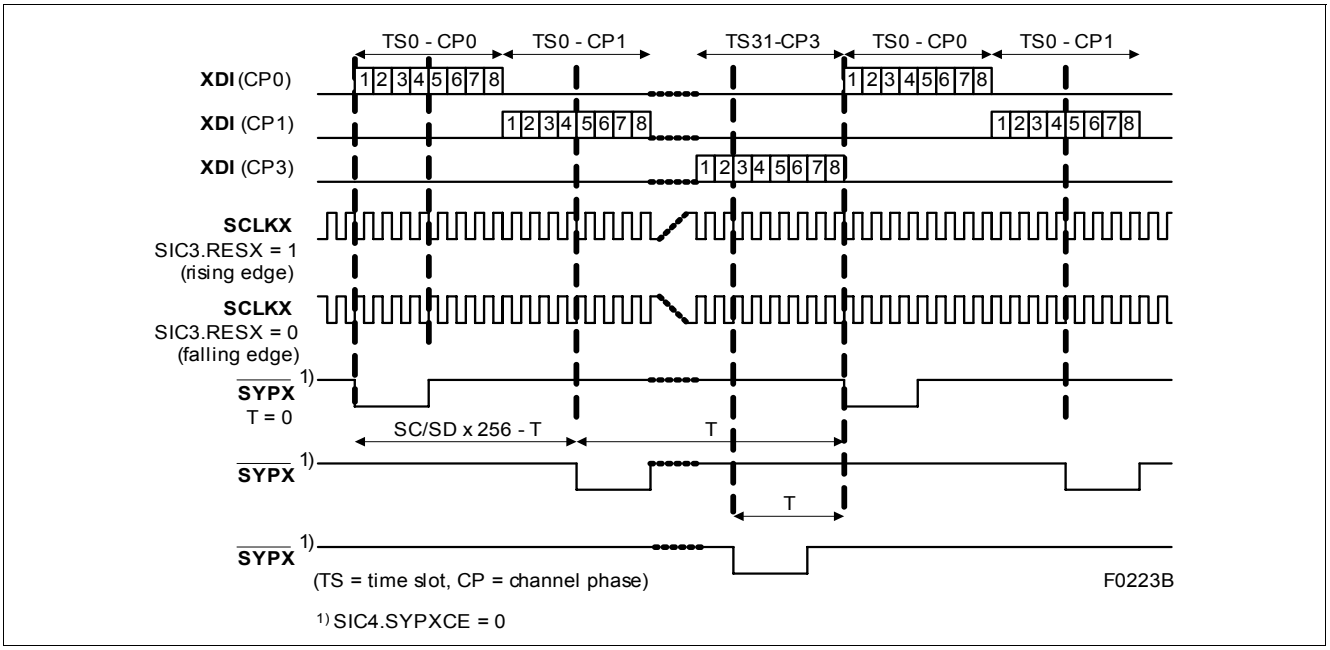


Figure 56 $\overline{\text{SYPX}}$ Offset Programming (8.192 Mbit/s, 8.192 MHz)

4.6.4 Time Slot Assigner (E1)

HDLC channel 1 offers the flexibility to connect data during certain time slots, as defined by registers RTR(4:1) and TTR(4:1) (**RTR1_E**, **TTR1_E**), to the RFIFO and XFIFO, respectively. Any combinations of time slots can be programmed for the receive and transmit directions. If CCR1.EITS = ´1´ (**CCR1_E**) the selected time slots (RTR(4:1)) are stored in the RFIFO of the signaling controller and the XFIFO contents is inserted into the transmit path as controlled by registers TTR(4:1).

For HDLC channels 2 and 3, one out of 31 time slots can be selected for each channel, but in common for transmit and receive direction.

Within selected time slots single bit positions can be masked to be used/not used for HDLC transmission for all HDLC channels. Additionally, the use of even, odd or both frames can be selected for each HDLC channel individually.

Table 38 Time Slot Assigner HDLC Channel 1 (E1)

Receive Time Slot Register Bit	Transmit Time Slot Register Bit	Time Slot	Receive Time Slot Register Bit	Transmit Time Slot Register Bit	Time Slot
RTR 1.7	TTR 1.7	0	RTR 3.7	TTR 3.7	16
RTR 1.6	TTR 1.6	1	RTR 3.6	TTR 3.6	17
RTR 1.5	TTR 1.5	2	RTR 3.5	TTR 3.5	18
RTR 1.4	TTR 1.4	3	RTR 3.4	TTR 3.4	19
RTR 1.3	TTR 1.3	4	RTR 3.3	TTR 3.3	20
RTR 1.2	TTR 1.2	5	RTR 3.2	TTR 3.2	21
RTR 1.1	TTR 1.1	6	RTR 3.1	TTR 3.1	22
RTR 1.0	TTR 1.0	7	RTR 3.0	TTR 3.0	23
RTR 2.7	TTR 2.7	8	RTR 4.7	TTR 4.7	24
RTR 2.6	TTR 2.6	9	RTR 4.6	TTR 4.6	25
RTR 2.5	TTR 2.5	10	RTR 4.5	TTR 4.5	26
RTR 2.4	TTR 2.4	11	RTR 4.4	TTR 4.4	27
RTR 2.3	TTR 2.3	12	RTR 4.3	TTR 4.3	28
RTR 2.2	TTR 2.2	13	RTR 4.2	TTR 4.2	29
RTR 2.1	TTR 2.1	14	RTR 4.1	TTR 4.1	30
RTR 2.0	TTR 2.0	15	RTR 4.0	TTR 4.0	31

4.7 Test Functions (E1)

The following chapters describe the different test function of the OctalFALC™.

4.7.1 Pseudo-Random Binary Sequence Generation and Monitor (E1)

The OctalFALC™ has the ability to generate and monitor pseudo-random binary sequences (PRBS). The generated PRBS pattern is transmitted to the remote end on pins XL1/2 or XDOP/N and can be inverted optionally. Generation and monitoring of PRBS pattern is done according to ITU-T O.150 and ITU-T O.151.

The PRBS monitor monitores the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non-inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter (CEC2). Synchronization is reached within 400 ms with a probability of 99.9% at a bit error rate of up to 10^{-1}.

Different PRBS modes which are using different bits and time slots in a E1/T1/J1 frame can be selected, see **Table 40**.

In the “unframed” mode all bits of all slots in a E1 frame are used for PRBS.

In the “framed” mode the frame byte (time slot 0) of an E1 frame is not used for PRBS respectively.

Selection of the PRBS modes “unframed” and “framed”is done by TPC0.PRM = ´00_b´ and TPC0.FRA.

For TPC0.PRM(1:0) not ´00_b´ (**TPC0_E**), each time slot of an E1 frame can be selected indiviually to send and receive a PRBS signal. Selection is done by the registers PRBSTS1 to PRBSTS4. Here the used time slot numbers are the same as used normally for numbering of the time slots: In E1 frames time slot 0 (TS0) up to time slot 31 (TS31), were TS0 is the frame byte (time slot number 0 indicates the frame byte).

If a time slot is used or not for PRBS transmission and reception is controlled by the registers PRBSTS1..4 (**PRBSTS1_E**). The number of used time slots for PRBS is refered to as “N”. The range of N is 1, ..., 32 for E1 because of the frame bit. The time slot selection 0 up to 31 for E1 by PBBSTS(1:4) is common for all eight ports respectively.

The N multiple time slots are selected arbitrarily for PRBS. The PRBS data stream has to be written into or read from the time slots consecutive respectively.

The selected time slot numbers are related to the mapping used on the system interface.

Note that deselection of time slot 0 (PRBSTS1.TS0 = ´0´) perfomes a “framed” mode.

For TPC0.PRM not ´00b´, normally all eight bits of the time slots are used for PRBS (“N × 64 kbit/s”). To allow CAS-BR in T1 mode, only 7 MSBs of the selected time slots can be optionally used for PRBS to avoid CAS disturbance (“N × 56 kbit/s”), the eight´s bit of all time slots (which is the CAS bit in T1) is not used for PRBS. Setting of this mode is performed by setting the register bits TPC0.PRM(1:0) to´11b´. Note that this mode can be used also in E1 mode, but makes no sense: In E1 CAS disturbance can be avoided by deselection of the appropriate time slot 16.

Note that in “N × 64 kbit/s” mode and if all time slots are selected by PRBSTS(1:4) all bits in the frame are used for PRBS (that is an “unframed” mode).

The PRBS pattern (polynoms) can be selected to be 2^{11}-1, 2^{15}-1, 2^{20}-1or 2^{23}-1 by the register bits TPC0.PRP(1:0) and LCR1.LLBP (**LCR1_E**), see **Table 39**. For definition of this polynoms see the Standards ITU-T O.150, O.151. and TR62441. The polynoms 2^{11}-1 and 2^{23}-1 can be selected only if TPC0.PRM unequal ´00b´.

Transmission of PRBS pattern is enabled by register bit LCR1.XPRBS. With the register bit LCR1.FLLB switching between not inverted and inverted transmit pattern can be done.

The receive monitoring of PRBS patterns is enabled by register bit LCR1.EPRM. In general, depending on bit LCR1.EPRM the source of the interrupt status bit ISR1.LLBSC changed, see register description. The type of detected PRBS pattern in the receiver is shown in the status register bits PRBSSTA.PRS. Every change of the bits PRS in PRBSSTA sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected if the mode “alarm simulation” is active.

The detection of all_zero or all_ones pattern is done over 12, 16, 21 or 24 consecutive bits, depending on the selected PRBS polynom (2^{11}-1, 2^{15}-1, 2^{20}-1or 2^{23}-1 respectively). The detection of all_zero or all_ones is independent on LCR1.FLLB.

The destinction between all-ones and all-zeros pattern is possible by combination of .

- The information about the first reached PRBS status after the PRBS monitor was enabled (“PRBS pattern detected” or “inverted PRBS pattern detected”) with
- The status information “all-zero pattern detected” or “all-ones pattern detected”

Because every bit error in the PRBS sequence increments the bit error counter BEC, no special status information like “PRBS detected with errors” is given here.

The time slot selection is related to the mapping used on the system interface.

Table 39 Supported PRBS Polynoms

TPC0.PRP(1:0)	TPC0.PRM	LCR1.LLBP	Kind of Polynom	Comment
00	01 or 11	X	2^{11} -1	
01	01 or 11	X	2^{15} -1	
10	01 or 11	X	2^{20} -1	
11	01 or 11	X	2^{23} -1	
XX	00	0	2^{15} -1	SW compatble to QuadFALC®
XX	00	1	2^{20} -1	

Table 40 Bit/Time Slot Selection of PRBS Pattern

TPC0.PRM	TPC0.FRA	Kind of Selection	Comment
00	0	Unframed	Settings in PRBSTS are not valid; SW compatble to QuadFALC®
00	1	Framed	
01	X	N x 64 kbit/s	“framed” mode if TS0 is deselected; CAS in E1 is not distubed if time slot16 is deselected
10	X	Reserved	
11	X	N x 56 kbit/s	Implies a “framed” mode

4.7.2 Remote Loop (E1)

In the remote loop-back mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON through the analog or digital transmitter, see **Figure 57** and **Figure 31**. As in normal mode they are also processed by the synchronizer and then sent to the system interface. The remote loop-back mode is activated by

- Control bit LIM1.RL or
- After detection of the appropriate In-band loop code, if enabled by ALS.LILS and if LIM0.LL = ´0´ (**LIM0_E**) (to avoid deadlocks), see **Chapter 4.5.6**.

Received data can be looped with or without the jitter attenuator (JATT buffer) dependent on LIM1.JATT (**LIM1_E**).

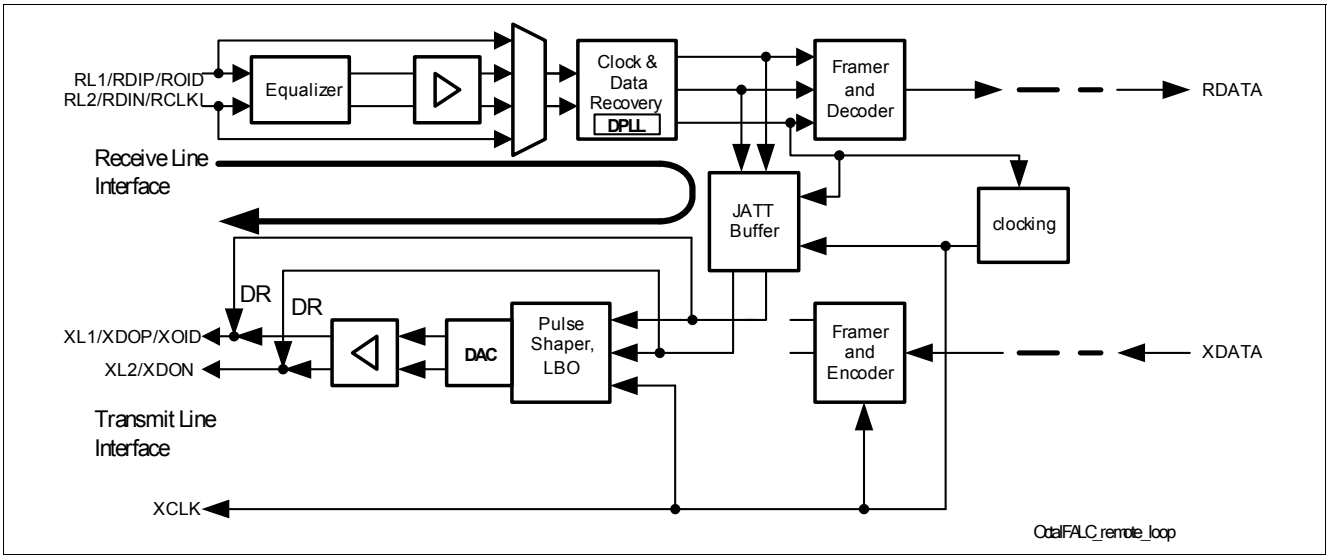


Figure 57 Remote Loop (E1)

DR means digital interface with dual rail mode.

4.7.3 Payload Loop-Back (E1)

To perform an effective circuit test a payload loop is implemented.

The payload loop-back is activated by setting FMR2.PLB (**FMR2_E**).

During activated payload loop-back the data stream is looped from the receiver section back to transmitter section. The looped data passes the complete receiver including the wander and jitter compensation in the receive elastic buffer and is output on pin RDO. Instead of the data an AIS signal (FMR2.SAIS) can be sent to the system interface.

The framing bits, CRC4 and spare bits are not looped, if XSP.TT0 = ´0´ (**XSP_E**). They are generated by the OctalFALC™ transmitter. If the PLB is enabled the transmitter and the data on pins XL1/2 or XDOP/XDON are clocked with SCLKR instead of SCLKX. If XSP.TT0 = ´1´ the received time slot 0 is sent back transparently to the line interface. Data on the following pins is ignored: XDI, XSIG, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally.

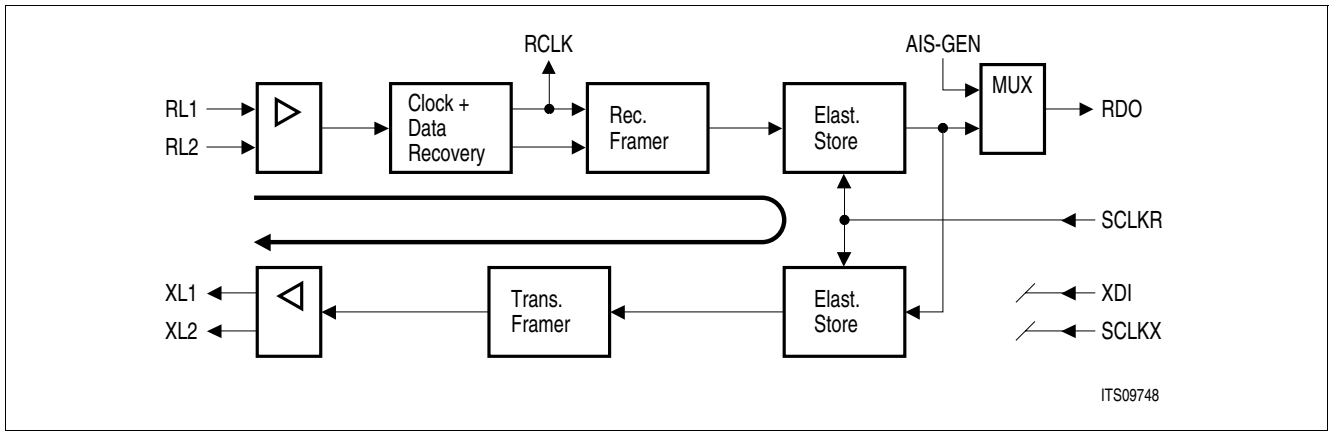


Figure 58 Payload Loop (E1)

4.7.4 Local Loop (E1)

The local loop-back is activated by

- The control bit LIM0.LL (**LIM0_E**).
- After detection of the appropriate In-band loop code, if enabled by ALS.SILS, see **Chapter 4.5.6**.

The local loop-back mode disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by the system interface is routed through the analog receiver back to the system interface. However, the bit stream is transmitted undisturbedly on the line. However, an AIS to the distant end can be enabled by setting FMR1.XAIS = ´1´ without influencing the data looped back to the system interface.

Note that enabling the local loop usually invokes an out-of-frame error until the receiver resynchronizes to the new framing. The serial codes for transmitter and receiver have to be identical.

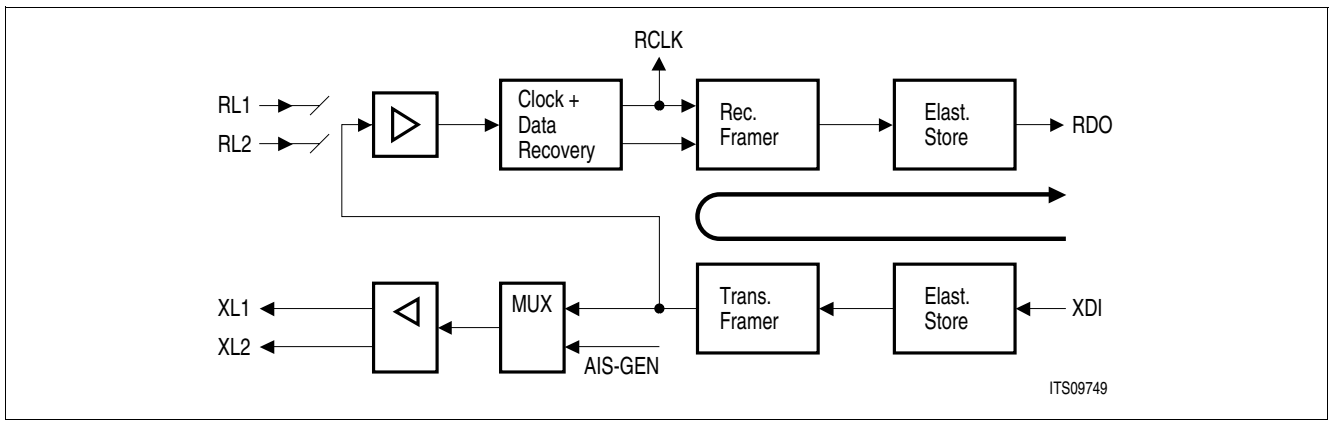


Figure 59 Local Loop (E1)

4.7.5 Single Channel Loop-Back (E1)

Each of the 32 time slots can be selected for loop-back from the system PCM input (XDI) to the system PCM output (RDO). This loop-back is programmed for one time slot at a time selected by register bits LOOP.CLA(4:0) (**LOOP_E**) and enabled by LOOP.ECLB. During loop-back, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time slot.

For the time slot test, sending sequences of test patterns like a 1 kHz check signal shall be avoided. Otherwise an increased occurrence of slips in the tested time slot disturbs testing. These slips do not influence the other time slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

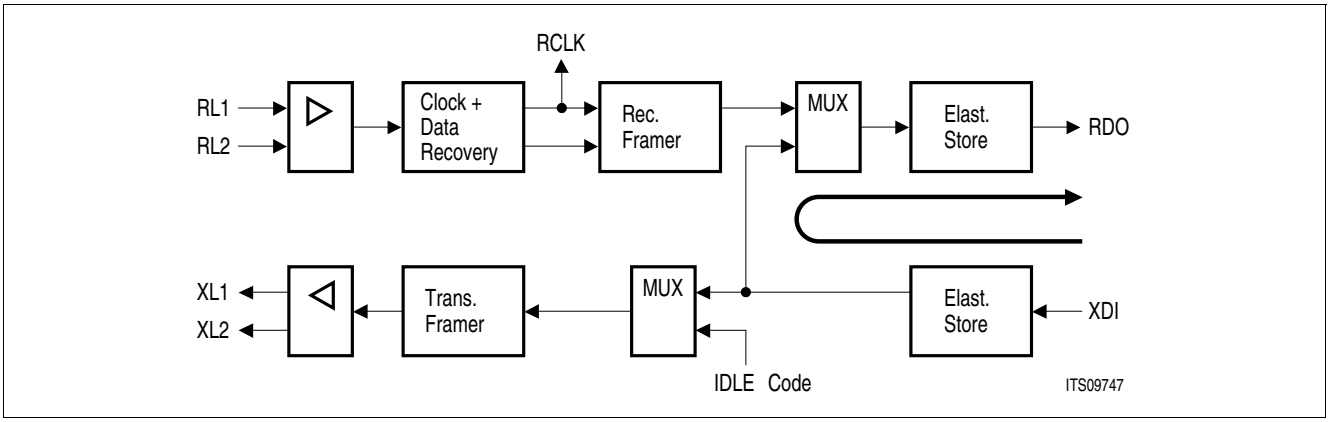


Figure 60 Single Channel Loop-Back (E1)

4.7.6 Alarm Simulation (E1)

Alarm simulation does not affect the normal operation of the device, i.e. all time slots remain available for transmission. However, possible *real* alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss-Of-Signal (LOS)
- Alarm Indication Signal (AIS)
- Loss of pulse frame
- Remote alarm indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter (HDB3 Code)
- CRC4 error counter
- E-Bit error counter
- CEC2 counter
- CEC3 counter

Some of the above indications are only simulated if the OctalFALC™ is configured to a mode where the alarm is applicable (e.g. no CRC4 error simulation when doubleframe format is enabled).

Setting of the bit FMR0.SIM initiates alarm simulation, interrupt status bits are set. Error counting and indication occurs while this bit is set. After it is reset all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms like AIS and LOS are cleared automatically. Interrupt status registers and error counters are automatically cleared on read.

4.7.7 Single Bit Defect Insertion (E1)

Single bit defects can be inserted into the transmit data stream for the following functions:

FAS defect, multiframe defect, CRC defect, CAS defect, PRBS defect and bipolar violation.

Defect insertion is controlled by register IERR (**IERR_E**).

5 Functional Description T1/J1

5.1 Receive Path in T1/J1 Mode

An overview about the receive path of one channel of the OctalFALC™ for all modes is given in **Figure 21**. Only special T1/J1 functionalities are described in this chapter

5.1.1 Receive Line Coding (T1/J1)

The B8ZS line code or the AMI (ZCS, zero code suppression) coding is provided for the data received from the ternary or the dual-rail interface. All code violations that do not correspond to zero substitution rules are detected. The detected errors increment the code violation counter (16 bits length). In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with B8ZS or AMI postprocessing is provided. If CMI code is selected the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. In case of NRZ coding data is latched with the falling edge RCLKI.

When using the optical interface with NRZ coding, the decoder is bypassed and no code violations are detected.

Additionally, the receive line interface contains the alarm detection for Alarm Indication Signal AIS (Blue Alarm) and the loss-of-signal LOS (Red Alarm).

The signal at the ternary interface is received at both ends of a transformer.

5.1.2 Loss-of-Signal Detection (T1/J1)

There are different definitions for detecting Loss-Of-Signal alarms (LOS) in the ITU-T G.775 and AT&T TR 54016. The OctalFALC™ covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable by register GCR.SCI.

- Detection: An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN or ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS = ´0´) (**LIM1_T**). The receive signal level Q is programmable by three control bits LIM1.RIL(2:0), see **Table 139**. The number N is set by an 8-bit register (PCD). The contents of the PCD register is multiplied by 16, which results in the number of pulse periods, i.e. the time which has to suspend until the alarm has to be detected. The programmable range is 16 to 4096 pulse periods.
- Recovery: In general the recovery procedure starts after detecting a logical ´1´ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL(2:0)) of the nominal pulse. The value in the 8-bit register PCR (**PCR_T**) defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions are programmed by register LIM2.

If a loss-of-signal condition is detected in long-haul mode, the data stream can optionally be cleared automatically to avoid bit errors before LOS is indicated. The selection is done by LIM1.CLOS = ´1´.

5.1.3 Receive Jitter Attenuation Performance (T1/J1)

The jitter attenuator meets the jitter transfer requirements of the PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431 and G.703 (refer to **Figure 61**).

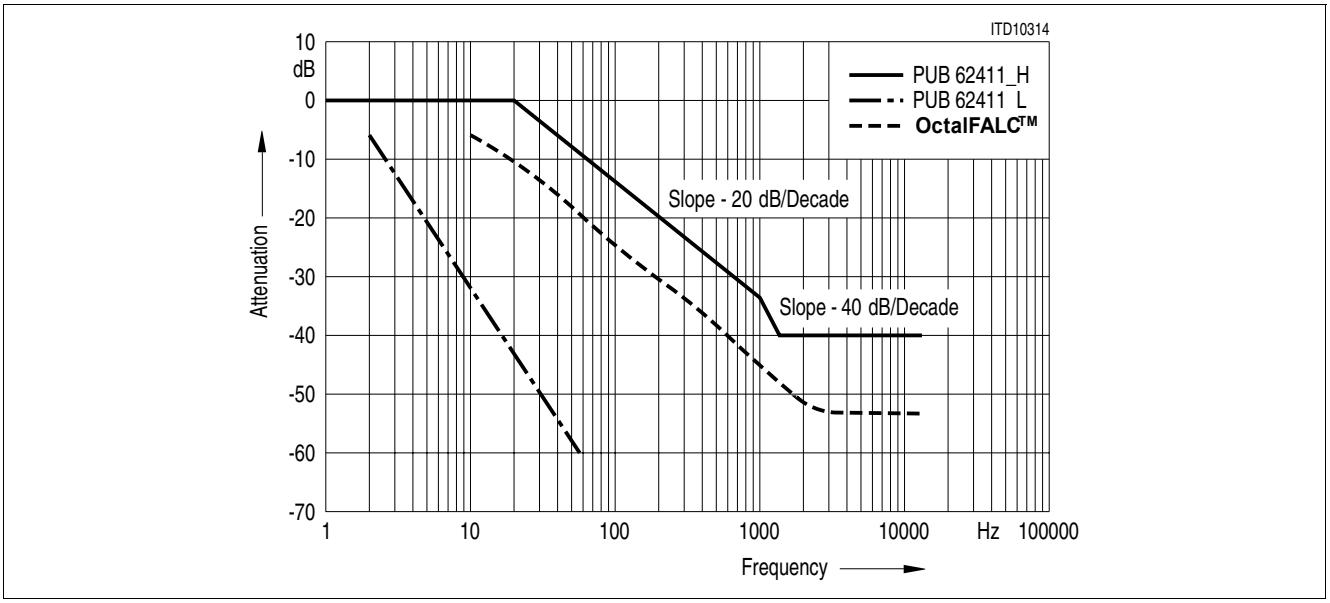


Figure 61 Jitter Attenuation Performance (T1/J1)

5.1.4 Jitter Tolerance (T1/J1)

The OctalFALC™ receiver's tolerance to input jitter complies with ITU, AT&T and Telcordia requirements for T1 applications.

Figure 62 shows the curves of different input jitter specifications stated below as well as the OctalFALC™ performance.

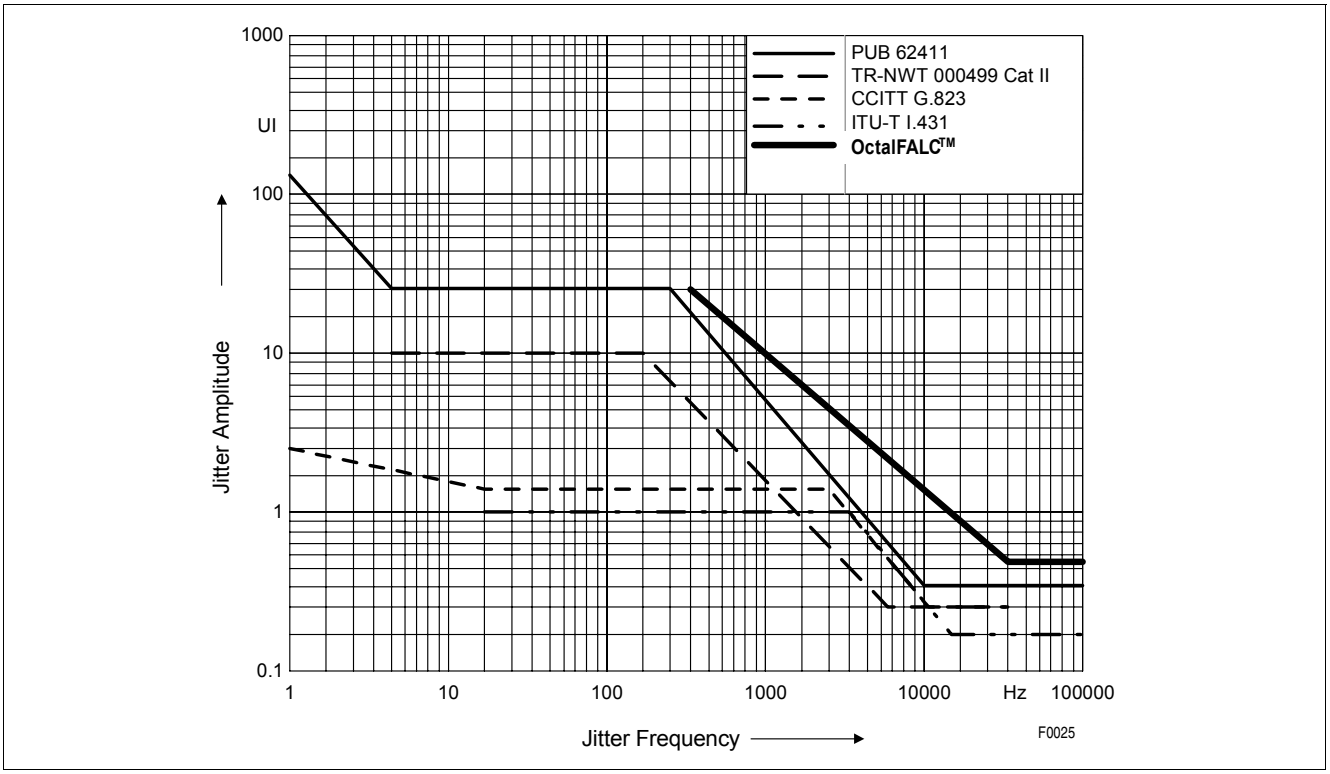


Figure 62 Jitter Tolerance (T1/J1)

5.1.5 Output Jitter (T1/J1)

According to the input jitter defined by PUB62411 the OctalFALC™ generates the output jitter, which is specified in **Table 41** below.

Table 41 Output Jitter (T1/J1)

Specification	Measurement Filter Bandwidth		Output Jitter [UI peak to peak]
	Lower Cutoff	Upper Cutoff	
PUB 62411	10 Hz	8 kHz	< 0.015
	8 kHz	40 kHz	< 0.015
	10 Hz	40 kHz	< 0.015
	Broadband		< 0.02

5.1.6 Framer/Synchronizer (T1/J1)

The following functions are performed:

- Synchronization on pulse frame and multiframe
- Error indication when synchronization is lost. In this case, AIS is sent to the system side automatically and remote alarm to the remote end if enabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This is done automatically by the OctalFALC™ or user controlled over the asynchronous, SPI or SCI interface.
- Detection of remote alarm (yellow alarm) indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Detection of framed or unframed in-band loop-up/-down code
- Generation of various maskable interrupt statuses of the receiver functions.
- Generation of control signals to synchronize the CRC checker, and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC multiframe according to the CRC6 procedure (refer to ITU-T G.704). These bits are compared with those check bits that are received during the next CRC multiframe. If there is at least one mismatch, the CRC error counter (16 bit) is incremented.

5.1.7 Receive Elastic Buffer (T1/J1)

The received bit stream is stored in the receive elastic buffer. The size of the elastic buffer is configured independently for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS(1:0) (**SIC1_T**), see **Table 42**:

Table 42 Receive Elastic Buffer Modes (T1/J1)

SIC1.RBS(1:0)	System Interface clocking rate	Channel translation mode	Frame buffer size	Maximum of wander [UI = 648 ns]	Average delay after performing a slip
00	Modulo 2.048 MHz	0	Two frame buffer or 386 bits	142	1 frame or 193 bits
		1		78	
	Modulo 1.544 MHz	--		140	
01	Modulo 2.048 MHz	0	One frame buffer or 193bits	70	96 bits
		1		50	
	Modulo 1.544 MHz	--		74	

Table 42 Receive Elastic Buffer Modes (T1/J1) (cont'd)

SIC1.RBS(1:0)	System Interface clocking rate	Channel translation mode	Frame buffer size	Maximum of wander [UI = 648 ns]	Average delay after performing a slip
10	Modulo 2.048 MHz	0	Short buffer or 96 bits	28	48 bits
		Not Supported		--	
	Modulo 1.544 MHz	---		38	
11	Bypass of the receive elastic buffer				

The functions are:

- Clock adoption between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, time slot serial data which is circularly written to the elastic buffer using internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the system clock sourced by SCLKR or by the receive jitter attenuator and the synchronization pulse ($\overline{SYPR}$) together with the programmed offset values for the receive time slot/clock slot counters. After conversion into a serial data stream, the data is sent out on port RDO. If the receive buffer is bypassed programming of the time slot offset is disabled and data is clocked off with RCLK instead of SCLKR.

The 24 received time slots (T1/J1) can be translated into the 32 system time slots (E1) in two different channel translation modes controlled by FMR1.CTM (**FMR1_T**). Unequipped time slots are set to ´FF_H´. See **Table 43**.

Table 43 Channel Translation Modes (DS1/J1)

Channels (received time slots)		Time Slots on system side	Channels (received time slots)		Time Slots on system side
Channel Translation Mode 0	Channel Translation Mode 1		Channel Translation Mode 0	Channel Translation Mode 1	
FS/DL	FS/DL	0	Unequipped	16	16
1	1	1	13	17	17
2	2	2	14	18	18
3	3	3	15	19	19
Unequipped	4	4	Unequipped	20	20
4	5	5	16	21	21
5	6	6	17	22	22
6	7	7	18	23	23
Unequipped	8	8	Unequipped	24	24
7	9	9	19	Unequipped	25
8	10	10	20	Unequipped	26
9	11	11	21	Unequipped	27
Unequipped	12	12	Unequipped	Unequipped	28
10	13	13	22	Unequipped	29
11	14	14	23	Unequipped	30
12	15	15	24	Unequipped	31

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 96 or 48 bits respectively.

In bypass mode the time slot assigner is disabled. In this case $\overline{\text{SYPR}}$ programmed as input is ignored and the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

Table 44 gives an overview of the receive buffer operating modes (**SIC1_T**).

Table 44 Receive Buffer Operation Modes (T1/J1)

SIC1.RBS(1:0)	Buffer Size	TS Offset Programming (RC(1:0)) + SYPR = input	Slip Performing
11	Bypass	Disabled	No
10	Short buffer	Not recommended, recommended: $\overline{\text{SYPR}}$ = output (usage of the RFM with CMR2.IRSP = ´0´)	Yes
01	1 frame		Yes
00	2 frames	Enabled	Yes

Figure 63 gives an idea of operation of the receive elastic buffer: A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface, i.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated by the interrupt status bits ISR3.RSP and ISR3.RSN (**ISR3_T**).

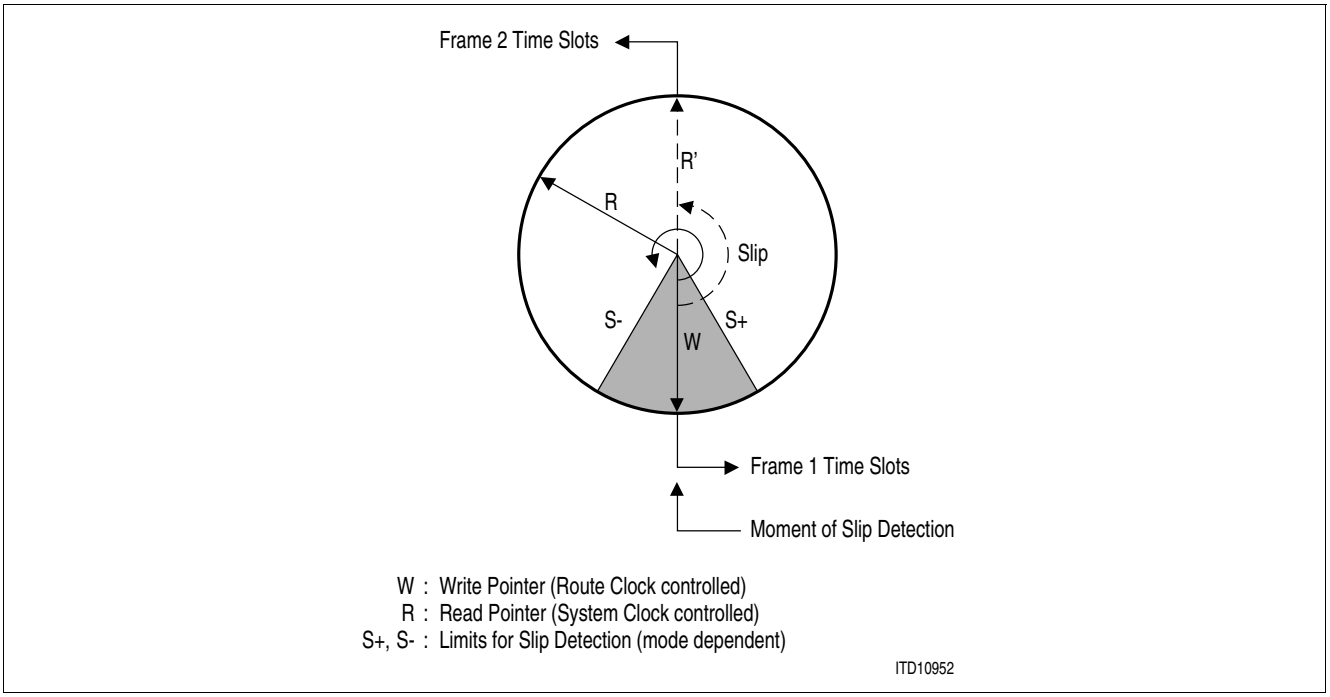


Figure 63 The Receive Elastic Buffer as Circularly Organized Memory

5.2 Transmit Path in T1/J1 Mode

An overview about the transmit path of one channel of the OctalFALC™ for all modes is given in **Figure 29**. Only special T1/J1 functionalities are described in this chapter.

5.2.1 Transmit Elastic Buffer (T1/J1)

The transmit elastic store with a size of max. 386 bit (two frames) serves as a temporary store for the PCM data to adapt the system clock (SCLKX) to the internally generated clock for the transmit data, and to retranslate time slot structure used in the system to that of the line side. Its optimal start position is initiated when programming the transmit time slot offset values. A difference in the effective data rates of system side and transmit side lead to an overflow or underflow of the transmit memory. Thus, errors in data transmission to the remote end occur. This error condition (transmit slip) is reported to the microprocessor by interrupt status registers. The received bit stream from pin XDI is optionally stored in the transmit elastic buffer. The memory is organized as the receive elastic buffer. Programming of the transmit buffer size is done by SIC1.XBS(1:0) (**SIC1_T**):

- XBS(1:0) = ´00_b´: bypass of the transmit elastic buffer
- XBS(1:0) = ´01_b´: one frame buffer or 193 bits Maximum of wander amplitude (peak-to-peak): (1 UI = 648 ns) System interface clocking rate: modulo 2.048 MHz: Maximum of wander: 70 UI in channel translation mode 0 Maximum of wander: 45 UI in channel translation mode 1 System interface clocking rate: modulo 1.544 MHz: Maximum of wander: 74 UI average delay after performing a slip: 96 bits
- XBS(1:0) = ´10_b´: two frame buffer or 386 bits System interface clocking rate: modulo 2.048 MHz: 142 UI in channel translation mode 0 78 UI in channel translation mode 1 System interface clocking rate: modulo 1.544 MHz: Maximum of wander: 140 UI average delay after performing a slip: 193 bits
- XBS(1:0) = ´11_b´: short buffer or 96 bits: System interface clocking rate: modulo 2.048 MHz: Maximum of wander: 28 UI in channel translation mode 0; channel translation mode 1 not supported System interface clocking rate: modulo 1.544 MHz: Maximum of wander: 38 UI average delay after performing a slip: 48 bits

The functions of the transmit buffer are:

- Clock adoption between system clock (SCLKX/R) and internally generated transmit route clock (XCLK) or externally sourced TCLK.
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit route frame

- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX/R and $\overline{\text{SYPX}}$/XMFS in combination with the programmed offset values for the transmit time slot/clock slot counters. Reading of stored data is controlled by the clock generated by DCO-X circuitry or the externally generated TCLK and the transmit framer. With the de-jittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is automatically done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN.

A reinitialization of the transmit memory is done by reprogramming the transmit time slot counter XC1 and with the next $\overline{\text{SYPX}}$ pulse. After that, this memory has its optimal start position.

The frequency of the working clock for the transmit system interface is programmable by SIC1.SSC(1:0) and SIC2.SSC2 in a range of 1.544 to 12.352 MHz/2.048 to 16.384 MHz, see **Table 57**. Generally the data or marker on the system interface are clocked off or latched on the rising or falling edge of the SCLKX clock, controlled by SIC3.RESX and SIC4.SYPXCE (**SIC3_T**, **SIC4_T**). Some clocking rates allow transmission of time slots/marker in different channel phases. Each channel phase which shall be latched on ports XDI and XP(A:B) is programmable by bits SIC2.SICS(2:0), the remaining channel phases are cleared or ignored respectively.

The following table gives an overview of the transmit buffer operating modes (**SIC1_T**).

Table 45 Transmit Buffer Operating Modes (T1/J1)

SIC1.XBS(1:0)	Buffer Size	TS Offset programming	Slip performance
00	Bypass	Enabled	No
11	Short buffer	Enabled	Yes
01	1 frame	Enabled	Yes
10	2 frames	Enabled	Yes

5.3 Signaling Controller (T1/J1)

The signaling controller can be programmed to operate in various signaling modes. The OctalFALC™ performs the following signaling and data link methods.

5.3.1 HDLC or LAPD Access (T1/J1)

The OctalFALC™ offers three independent HDLC/BOM controller for each of the eight channels. All of them provide the following features:

- Receive FIFO for each channel, configurable up to 128 bytes, see also **Chapter 3.4.3**
- 128 byte transmit FIFO for each channel
- Transmission in one of 24 time slots (time slot number programmable for each channel individually)
- Transmission in even frames only, odd frames only or both (programmable for each channel individually)
- Bit positions to be used in selected time slots are maskable (any bit position can be enabled for each channel individually)
- HDLC or transparent mode
- Flag detection
- CRC checking
- Bit-stuffing
- Flexible address recognition (1 byte, 2 bytes)
- C/R bit processing (according to LAPD protocol)

In addition to this, HDLC channel 1 provides:

- SS7 support
- BOM (bit oriented message) support
- Flexibility to insert and extract data during certain time slots, any combination of time slots can be programmed independently for the receive and transmit direction

The receive FIFO structure is described in **Chapter 3.4.3**.

Operating in HDLC or BOM mode “flags” or “idle” are transmitted as interframe timefill. The OctalFALC™ offers the flexibility to insert data during certain time slots. Any combinations of time slots can be programmed separately for the receive and transmit direction if using HDLC channel 1. HDLC channel 2 and 3 support one programmable time slot common for receive and transmit direction each.

Each of these HDLC controllers can be attached to either the line side (so called as “standard configuration”, see **Figure 38**) or the system side (“inverse configuration”, see **Figure 39**). Inverse HDLC mode is selected by setting MODE.HDLCI = ´1´, MODE2.HDLCI2 = ´1´ or MODE3.HDLCI3 = ´1´ (for each of the three HDLC controllers and each of the eight channels individually). Note that a detection of a Out-Band loop message (BOM code) on the line side is only possible if the HDLC/BOM controller 1 is attached to the line side; a detection of a BOM code on the system side is only possible in the “inverse” mode of the HDLC controller.

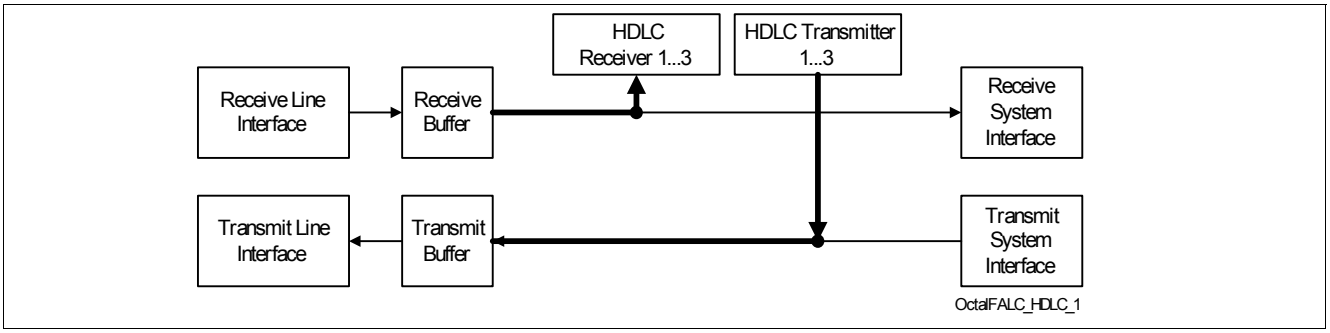


Figure 64 HDLC Controller Standard Configuration

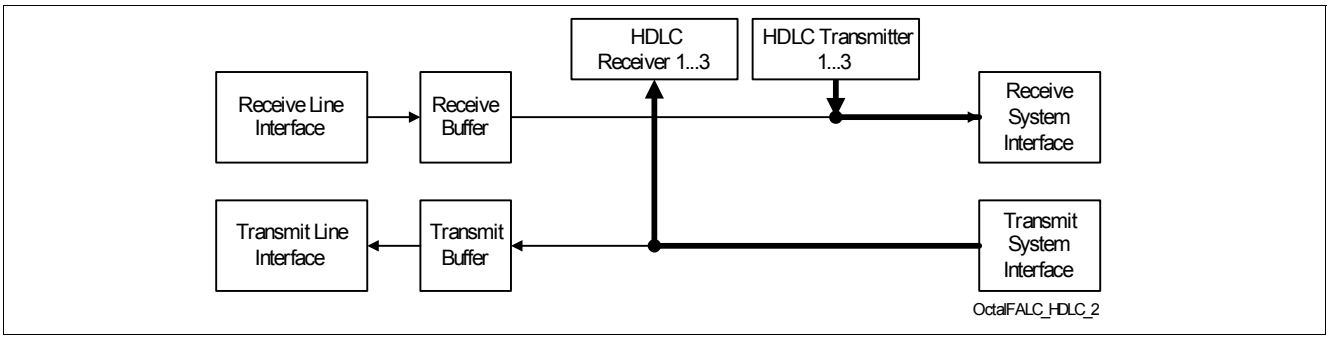


Figure 65 HDLC Controller Inverse Configuration

The BOM receiver of the HDLC/BOM controller 1 is enabled by setting MODE.BRAC and CCR1.EITS.

Switching between HDLC and BOM (if both MODE.BRAC and MODE.HRAC are set) is described in **Chapter 5.3.4**.

Each HDLC/BOM controller can be reset individually without disturbing the transmission on the remaining channels. Use CMDR.SRES for HDLC channel 1, CMDR3.SRES2 for HDLC channel 2 and CMDR4.SRES3 for HDLC channel 3, respectively (**CMDR_T**, **CMDR3_T**, **CMR4_T**).

Note that CMDR.RRES resets the whole RX path and therefor all HDLC channels.

After a XDU interrupt on a HDLC controller, the appropriate transmit signalling controller must be reset.

After an RDO interrupt on a HDLC controller, the receive HDLC controller needs no reset. So a receive HDLC controller reset per channel is not necessary.

In case of common channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 is supported. The signaling controller of the OctalFALC™ performs the flag detection, CRC checking, address comparison and zero bit removing. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the OctalFALC™ performs a 1 or 2-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value ´FE_H´ or ´FC_H´ (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison. Buffering of receive data is done in a 64 byte deep RFIFO.

In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without flag recognition, CRC checking or bit stuffing. This allows user specific protocol variations.

5.3.2 Support of Signaling System #7 (T1/J1)

HDLC controller 1 of each of the eight channels of the OctalFALC™ supports the signaling system #7 (SS7) which is described in ITU-Q.703. The following description assumes, that the reader is familiar with the SS7 protocol definition.

SS7 support must be activated by configuring the register bits MODE.MDS(2:0) (**MODE_T**). The SS7 protocol is supported by the following hardware features in receive mode:

- All Signaling Units (SU) are stored in the receive FIFO (RFIFO)
- Detecting of flags from the incoming data stream
- Bit stuffing (zero deletion)
- Checking of seven or more consecutive ones in the receive data stream
- Checking if the received Signaling Unit is a multiple of eight bits and at least six octets including the opening flag
- Calculation of the CRC16 checksum: In receive direction the calculated checksum is compared to the received one; errors are reported in register RSIS.
- Checking if the signal information field of a received signaling unit consists of more than 272 octets, in this case the current signaling unit is discarded.

In order to reduce the micro controller load, fill In signaling units (FISUs) are processed automatically. By examining the length indicator of a received signal unit the OctalFALC™ decides whether a FISU has been received. Consecutively received FISUs are compared and optionally not stored in the receive FIFO (RFIFO, up to 2 x 64 bytes), if the contents is equal to the previous one. The same applies to link status signaling units, if bit CCR5.CSF is set. The different types of signaling units as message signaling unit (MSU), link status signaling unit (LSSU) and fill in signaling units (FISU) are indicated in the RSIS register, which is automatically added to the RFIFO with each received signaling unit. The complete signaling unit except start and end flags is stored in the receive FIFO. The functions of bits CCR2.RCRC and CCR2.RADD (**CCR2_T**) are still valid in SS7 mode. Errored signaling units are handled automatically according to ITU-T Q.703 as shown in **Figure 40**. SU counter (su) and errored SU counter (Cs) are reset by setting CMDR2.RSUC. The error threshold T can be selected to be 64 (default) or 32 by setting/clearing bit CCR5.SUET (**CCR5_T**). If the defined error limit is exceeded, an interrupt (ISR1.SUEX) is generated, if not masked by IMR1.SUEX = ´1´.

Note: If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).

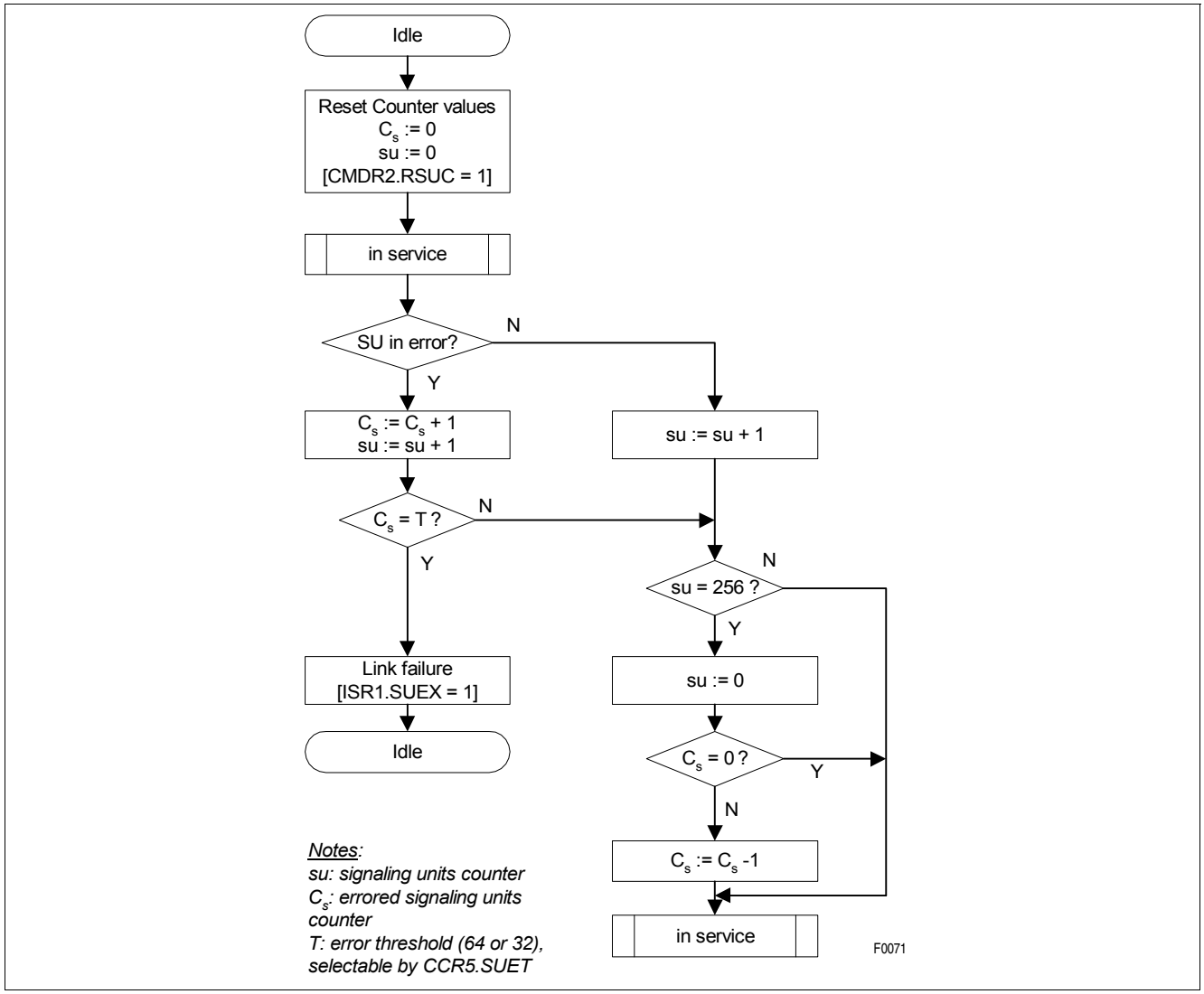


Figure 66 Automatic Handling of Errored Signaling Units

Data stored in the transmit FIFO (XFIFO) is sent automatically. The SS7 protocol is supported by the following hardware features in transmit direction:

- Transmission of flags at the beginning of each Signaling Unit
- Bit stuffing (zero insertion)
- Calculation of the CRC16 checksum: The transmitter adds the checksum to each Signaling Unit.

Each signaling unit written to the transmit FIFO (XFIFO) is sent once or repeatedly including flags, CRC checksum and stuffed bits. After e.g. an MSU has been transmitted completely, the OctalFALC™ optionally starts sending of FISUs containing the forward sequence number (FSN) and the backward sequence number (BSN) of the previously transmitted signaling unit. Setting bit CCR5.AFX causes Fill In Signaling Units (FISUs) to be sent continuously, if no HDLC or Signaling Unit (SU) is to be transmitted from XFIFO. During update of XFIFO, automatic transmission is interrupted and resumed after update is completed. The internally generated FISUs contain FSN and BSN of the last transmitted signaling unit written to XFIFO. Using CMDR.XREP = ´1´, the contents of XFIFO can be sent continuously. Clearing of CMDR.XRES/SRES stops the automatic repetition of transmission. This function is also available for HDLC frames, so no flag generation, CRC byte generation and bit stuffing is necessary. Example: After an MSU has been sent repetitively and XREP has been cleared, FISUs are sent automatically

5.3.3 CAS Bit-Robbing (T1/J1)

The channel associated signaling information (CAS) is carried on the line in the LSB of every sixth frame for each time slot. CAS operation mode of the OctalFALC™ is enabled in T1/J1 mode by setting of register bit FMR5.EIBR. Two basic modes can be select for receive and transmit direction independent from another:.

- Serial CAS: If RSIG is configured on one of the multifunction ports RPA, RPB or RPC, the received CAS information is given out on RSIG automatically, see **Chapter 5.3.3.1**. The CAS information is also stored in registers RS(12:1) (**RS1_T**) aligned to the CAS multiframe boundary. If XSIG is configured on one of the multifunction ports XPA or XPB, the transmitted CAS information is taken from XSIG automatically and the information in the registers XS(12:1) (**XS1_T**) is ignored, see **Chapter 5.3.3.2**.
- Parallel CAS: If RSIG is not configured on one of the multifunction ports RPA, RPB or RPC, the received CAS information is stored in registers RS(12:1) aligned to the CAS multiframe boundary, see **Chapter 5.3.3.3**. If XSIG is not configured on one of the multifunction ports XPA or XPB, the transmitted CAS information is taken from the registers XS(12:1), see **Chapter 5.3.3.4**.

In all this basic modes the following configurations can be done:

- Internal multiplexing of data and signaling data can be disabled on a per time slot basis (“clear channel” capability), see **Chapter 5.5.6**. This is valid for both serial and parallel CAS mode.
- Forcing of all robbed bits to ´1´ can be done to be not performed in CAS “cleared channels” by setting of XC0.BRF01.
- Bit robbing idle function can be done by setting XC0.BRIF. In this case bit robbing information is not overwritten by the idle code in idle channels. The bit robbing idle function in serial CAS and F72 mode is not operational.

5.3.3.1 Serial Receive CAS Bit-Robbing (T1/J1)

The complete received CAS information is output on pin RSIG.

The received CAS signaling data is clocked out with the working clock of the receive highway (SCLKR) together with the receive synchronization pulse ($\overline{\text{SYPR}}$). Data on RSIG is transmitted in the last 4 bits per time slot and are time slot aligned to the data on RDO. In ESF format the A,B,C,D bits are placed in the bit positions 5 to 8 per time slot. In F12/72 format the A and B bits are repeated in the C and D bit positions. The first 4 bits per time slot can be optionally fixed high or low. The FS/DL time slot is transmitted on RDO and RSIG. During idle time slots no signaling information is transmitted. Data on RSIG are only valid if the freeze signaling status is inactive. With FMR2.SAIS all-ones data is transmitted on RDO and RSIG.

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a loss-of-signal, or a loss-of-frame-alignment or a receive slip occurs. The current freeze status is output on port FREEZE (RPA, RPB or RPC) and indicated by register SIS.SFS. If SIS.SFS is active updating of the registers RS(12:1) is disabled. Optionally automatic freeze signaling is disabled by setting bit SIC3.DAF.

After CAS resynchronization an interrupt is generated. Because at this time the signaling is still frozen, CAS data is not valid yet. Readout of CAS data has to be delayed until the next CAS multiframe is received.

5.3.3.2 Serial Transmit CAS Bit-Robbing (T1/J1)

In serial CAS mode the signaling data on pin XSIG is sampled with the working clock of the transmit system interface (SCLKX) together with the transmit synchronous pulse ($\overline{\text{SYPX}}$). Data on XSIG is latched in the bit positions 5 to 8 per time slot, bits 1 to 4 are ignored. The FS/DL-bit is sampled on port XSIG and inserted in the outgoing data stream. The received CAS multiframe is inserted frame aligned into the data stream on XDI. Data sourced by the internal signaling controller overwrites the external signaling data which must be valid during the last frame of a multiframe. Internal multiplexing of data and signaling data can be disabled on a per time slot basis (clear channel capability). This is also valid when using the internal and external signaling mode.

5.3.3.3 Parallel Receive CAS Bit-Robbing (T1/J1)

Received CAS information is stored in registers RS(12:1) aligned to the CAS multiframe boundary.

To relieve the micro controller load from always reading the complete RS(12:1) buffer every 3 ms the OctalFALC™ notifies the micro controller by interrupt ISR0.RSC only when signaling changes from one multiframe to the next.

This interrupt can be suppressed for “cleared channels” by setting register bit CCR1.RSCC. Additionally the OctalFALC™ generates a receive signaling data change pointer (RSP1/2) which directly points to the updated RS(12:1) register.

Internal multiplexing of data and signaling data can be disabled on a per time slot basis (clear channel capability). This is also valid when using the internal and external signaling mode.

5.3.3.4 Parallel Transmit CAS Bit-Robbing (T1/J1)

The CAS information is taken from the registers XS(12:1). So the CAS information is controllable by the micro controller over the asynchronous, SPI or SCI interlace. The signaling controller inserts the CAS bit stream on the transmit line side.

5.3.4 Bit Oriented Messages (BOM) in ESF-DL Channel (T1/J1)

The OctalFALC™ HDLC controller 1 of each of the eight channels supports the DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016. Bit oriented messaging (BOM) is an Out-band signaling method.

The OctalFALC™ HDLC controller 1 supports detection of loop back BOM messages and automatic loop switching. This is described in **Chapter 5.5.8**.

The BOM code has the following format: ´11111111 0xxxxxxx0_b´ were the first bit of every byte is the MSB and the last is the LSB. (´11111111_b´ is the BOM flag.) Sending is done as for HDLC, this means LSB first, so ´11111111_b´ first. Note that this is consistent to the note 1) in the ANSI T1.403 specification: “rightmost bit transmitted first”.

Note: The data written into the XFIFO and read out of the RFIFO have to be bitwise mirrored to get the corresponding bit oriented codes defined in the ANSI T1.403 specification.

The HDLC and bit oriented message (BOM) receiver of the HDLC/BOM controller 1 can be switched on independent from another by setting the register bits MODE.HRAC and MODE.BRAC respectively. If the OctalFALC™ is used for HDLC formats only, the BOM receiver has to be switched off.

Storing of received DL-bit information in the receive FIFO (RFIFO, up to 128 byte deep) of the signaling controller and transmitting the XFIFO contents in the DL-bit positions is enabled by CCR1.EDLX,EITS = ´10_b´ (**CCR1_T**). Bytes starting or ending with a ´1´ are not stored.

Three different BOM reception modes can be programmed by CCR1.BRM and CCR2.RBFE (**CCR1_T**, **CCR2_T**):

- 10 byte packet mode: CCR1.BRM = ´0´: After storing 10 BOM bytes into the RFIFO the receive status byte marking a BOM frame (RSIS.HFR) is added as the eleventh byte and an interrupt ISR0.RME is generated. The sampling of data bytes continues and interrupts are generated every tenth bytes until the HDLC flag is detected.
- Continuos reception: CCR1.BRM = ´1´ : Interrupts are generated every 64, 32, 16 4 or 2 bytes, dependent on the configured RFIFO depth (see **Chapter 3.4.3**). After detecting a HDLC flag, byte sampling is stopped, the content of the status register RSIS is stored in the RFIFO and an interrupt ISR0.RME is generated.
- Continuos reception with 7 out of 10 filter mode: CCR1.BRM = ´1´ and CCR2.RBFE = ´1´: If CCR2.RFBE is set, the BOM receiver accepts only BOM frames after detecting 7 out of 10 equal BOM pattern. The content of the status register RSIS will not be written into the receive FIFO.

Switching between these modes is possible at any time.

Automatic switching between HDLC and BOM (if both MODE.BRAC and MODE.HRAC are set) will be done in the following way:

- After reset the HDLC/BOM controller is in HDLC mode.
- After eight consecutive ones (´FF_H´) were received: switching to BOM mode (note that eight consecutive ones are also an HDLC abort)
- After one HDLC flag (´$7E_H$´) was received: switching to HDLC mode (directly, additional HDLC flags are not necessary)
- A sequence ´FF_H´, ´$7E_H$´ is treated as a HDLC start flag

The status bit SIS.BOM (**SIS_T**) reflects the actual mode of the HDLC/BOM controller.

Note that BOM codes ´7E$_H$´ should be avoid.

If a BOM message occurs “inside” of a HDLC protocol, the HDLC protocol (frame) is corrupted due to the occurrence of the ABORT sequence.

5.3.5 4 kbit/s Data Link Access in F72 Format (T1/J1)

The DL-channel protocol is supported as follows:

- Access is done on a multiframe basis through registers RDL(3:1),
- The DL-bit information from frame 26 to 72 is stored in the receive FIFO of the signaling controller.

5.3.6 Data Link Access in ESF/F24 and F72 Format (T1/J1)

The DL-channel protocol is supported as follows:

- Access is done on a multiframe basis through registers RDL(3:1) and XDL(3:1), see **Chapter 5.3.6.1**, or
- HDLC access or transparent transmission (non HDLC mode) from XFIFO of HDLC channel 1

The signaling information stored in the XFIFO is inserted in the DL-bits of frame 26 to 72 in F72 format or in every other frame in ESF format. Transmission can be done on a multiframe boundary (CCR1.XMFA = ´1´). Operating in HDLC or BOM mode “flags” or “idle” are transmitted as interframe timefill.

If enabled via CCR1.EDLX/EITS = ´10$_b$´, the DL-bit information is stored in the receive FIFO of the signaling controller. The DL-bits stored in the XFIFO are inserted into the outgoing data stream. If CCR1.EDLX is cleared, a HDLC frame or a transparent frame can be sent or received via the RFIFO/XFIFO.

Table 46 DL-Bit Access Modes (T1/J1)

CCR1.XFMA	CCR1.EDLX	CCR1.EITS	FMR1.EDL	DL-Bit Access Mode
X	1	0	0	RFIFO, XFIFO
X	0	X	1	RDL(3:1), XDL(3:1)
X	0	X	0	Transparent

5.3.6.1 DL-Bit Access in ESF Format (T1/J1)

Only in ESF format two modes for accessing of the received and transmit DL-bits on a multiframe basis through registers RDL(3:1) and XDL(3:1) are performed by the OctalFALC™: Selection is done by register bit FMR5.DLM (**FMR5_T**) common for the receive and the transmit direction. Receive and transmit direction works accordingly. A receive multiframe begin interrupt is provided to read the received data DL-bits out of the registers RDL(3:1). A transmit multiframe begin interrupt requests for writing new information to the DL-bit registers XDL(3:1). The contents of registers XDL(3:1) is subsequently sent out on the transmit multiframe basis if it is enabled via FMR1.EDL.

- Standard DL-bit access: FMR5.DLM = ´0´, see **Figure 67** for receive direction. Sampling of DL-bits is done on a multiframe basis and stored in the registers RDL(2:1). Reading of the registers must be done by the micro controller after every receive multiframe begin interrupt. Writing into the registers XDL(2:1) must be done by the micro controller after every transmit multiframe begin interrupt
- Improved DL-bit access (only possible in ESF format): FMR5.DLM = ´1´, see **Figure 68** for receive direction. Sampled DL-bits are stored in the registers RDL(3:1). Reading of the registers must be done by the micro controller only after every second receive multiframe begin interrupt. Writing into the registers XDL(3:1) must be done by the micro controller also only after every second transmit multiframe begin interrupt. This reduces the number of required register accesses by 25 %.

Using the improved access bit oriented messages (BOM) can be inserted continuously without additional micro controller access every multiframe.

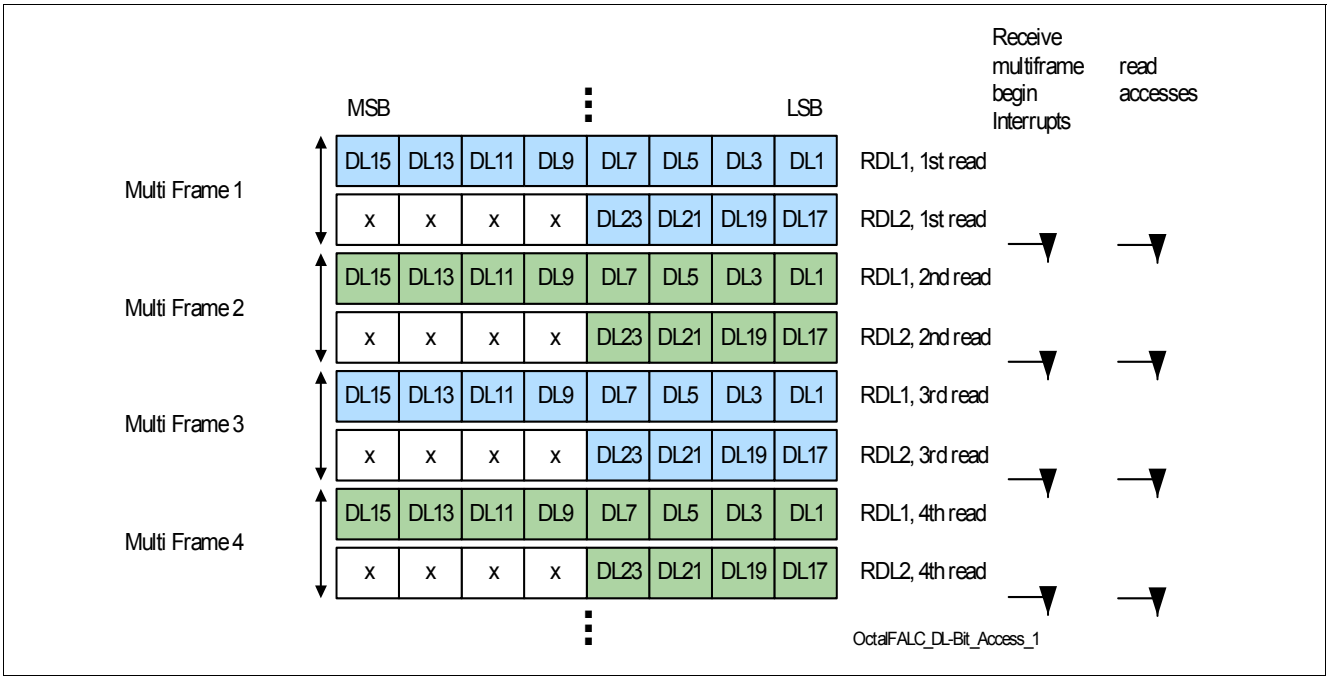


Figure 67 Standard DL-Bit Access in ESF Mode (T1/J1) in receive direction

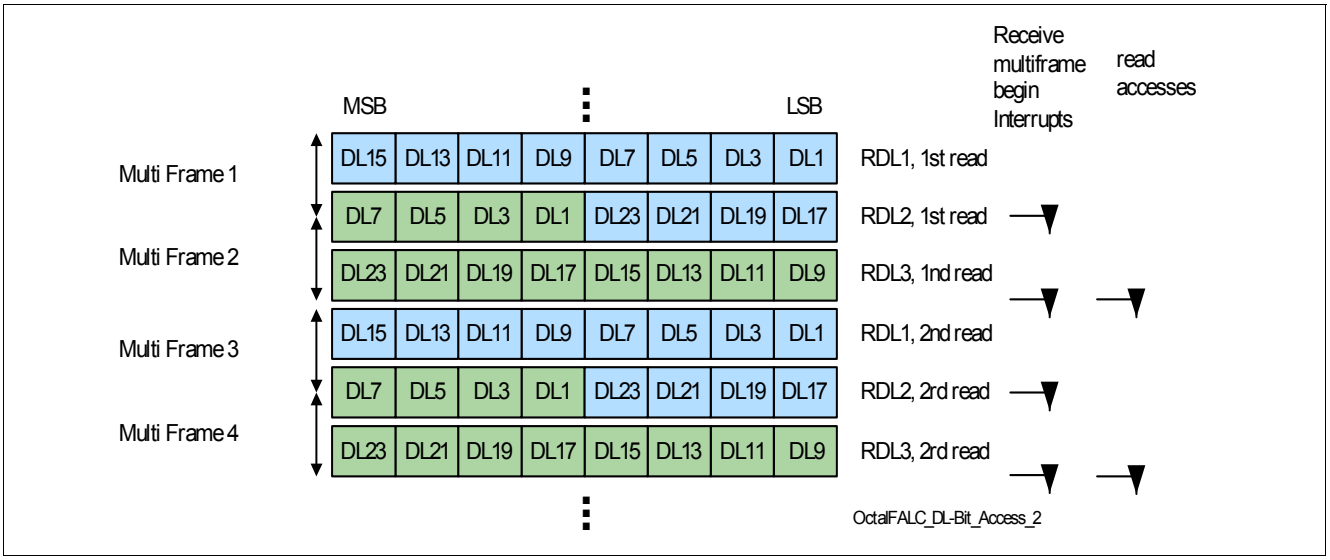


Figure 68 Improved DL-Bit Access in ESF Mode (T1/J1) in receive direction

5.3.7 Periodical Performance Report in ESF/F24 Format (T1/J1)

According to ANSI T1.403 the OctalFALC™ can automatically generate the **P**eriodical **P**erformance **R**eport (PPR) and

- Transmit it every second in the data link channel of the extended superframe format (ESF/F24 only). Automatic sending of this report can be enabled/disabled by the use of bit CCR5.EPR. A single report can be initiated manually at any time by setting CMDR2.XPPR. Then last PPR is send once and CMD2.XPPR is cleared automatically after sending was finished. and
- Store the actual performance parameters (of t_0) in the registers PPR0 and PPR1 (**PPR0_T**). New performance data is accessible immediately after the one-second interrupt is triggered and must be read before the next one-second interrupt occurs.

Performance information is sampled every second and the report contains data of the last four seconds as shown in the following tables.

Table 47 Structure of Periodical Performance Report (T1/J1)[1)]

Octet No.	8	7	6	5	4	3	2	1	Time
1	FLAG = ´01111110_b´								
2	SAPI = ´001110_b´						CR[2)]	EA=0	
3	TEI = ´0000000_b´							EA=1	
4	CONTROL = ´00000011_b´ = unacklowledged frame								
5	G3	LV	G4	U1	U2	G5	SL	G6	t0
6	FE	SE	LB	G1	R	G2	Nm	N1	
7	G3	LV	G4	U1	U2	G5	SL	G6	t0-1 s
8	FE	SE	LB	G1	R	G2	Nm	N1	
9	G3	LV	G4	U1	U2	G5	SL	G6	t0-2 s
10	FE	SE	LB	G1	R	G2	Nm	N1	
11	G3	LV	G4	U1	U2	G5	SL	G6	t0-3 s
12	FE	SE	LB	G1	R	G2	Nm	N1	
13	FCS								
14	FCS								
15	FLAG = ´01111110_b´								

1) The rightmost bit (bit 1) is transmitted first for all fields except for the two bytes of the FCS that are transmitted leftmost bit (bit 8) first.

2) Reflects state of bit CCR5.CR

Table 48 Bit Functions in Periodical Performance Report[1)]

Bit Value	Interpretation
G1 = 1	Number of CRC error events = 1
G2 = 1	1 < number of CRC error events $\leq$ 5
G3 = 1	5 < number of CRC error events $\leq$ 10
G4 = 1	10 < number of CRC error events $\leq$ 100
G5 = 1	100 < number of CRC error events $\leq$ 319
G6 = 1	Number of CRC error events $\geq$ 320
SE = 1	Severely errored framing event $\geq$ 1 (FE shall be ´0´)
FE = 1	Frame synchronization bit error event $\geq$ 1 (SE shall be ´0´)
LV = 1	Line code violation event $\geq$ 1
SL = 1	Slip event $\geq$ 1
LB = 1	Payload loop-back activated
U1	Not used (default value = ´0´)
U2	Not used (default value = ´0´)
R	Not used (default value = ´0´)
NmNi	One-second report modulo 4 counter

1) According to ANSI T1.403

5.4 Framer Operating Modes (T1/J1)

5.4.1 General (T1/J1)

The general parameters are:

FMR1.PMOD	:	1
PCM line bit rate	:	1.544 Mbit/s
Single frame length	:	193 bit, No. 1…193
Framing frequency	:	8 kHz
Organization	:	24 time slots, No. 1…24 with 8 bits each, No. 1…8 and one preceding F-bit

Summary of supported T1/J1 Framing Modes:

F4	:	4-frame multiframe
F12	:	12-frame multiframe (D4)
ESF	:	Extended Superframe (F24)
F72	:	72-frame multiframe (SLC96)

Selection of one of the four permissible framing formats is done by the register bits FMR4.FM(1:0) for the receiver and for the transmitter. (**FMR4_T**)

The operating mode of the OctalFALC™ is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The OctalFALC™ implements all of the standard and/or common framing structures PCM24 (T1/J1, 1.544 Mbit/s) carriers. The internal HDLC controller supports all signaling procedures including signaling frame synchronization/synthesis in all framing formats.

After reset, the OctalFALC™ must be programmed with FMR1.PMOD = ´1´ to enable the T1/J1 (PCM24) mode.

5.4.2 General Aspects of Synchronization (T1/J1)

Synchronization status is reported by bit FRS0.LFA (Loss Of Frame Alignment). Framing errors (pulse frame and multiframe) are counted by the Framing Error Counter FEC.

Asynchronous state is reached if 2 out of 4 (bit FMR4.SSC(1:0) = ´00_b´) (**FMR4_T**), or 2 out of 5 (bit FMR4.SSC(1:0) = ´01_b´), or 2 out of 6 (bit FMR4.SSC(1:0) = ´10_b´), or 4 consecutive multiframe pattern in ESF format are incorrect (bit FMR4.SSC(1:0) = ´11_b´). If auto mode is enabled, counting of framing errors is interrupted.

The resynchronization procedure is controlled by either one of the following procedures:

- FMR4.AUTO = ´1´: Automatically. Additionally, it can be triggered by the user by setting/resetting one of the bits FMR0.FRS (force resynchronization) or FMR0.EXLS (external loss of frame).
- FMR4.AUTO = ´0´: User controlled, exclusively, by the control bits described above in the non-auto mode .

5.4.3 Addition for F12 and F72 Format (T1/J1)

FT and FS bit conditions, i.e. pulse frame alignment and multiframe alignment can be handled separately if programmed by bit FMR2.SSP. Thus, a multiframe resynchronization can be automatically initiated after detecting 2 errors out of 4/5/6 consecutive multiframing bits without influencing the state of the terminal framing.

In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.

In asynchronous state, the function of FMR0.EXLS is the same as above. Setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. Otherwise a new frame search is started. This is useful in case the framing pattern that defines the pulse frame position is imitated periodically by a pattern in one of the speech/data channels.

The control bit FMR0.EXLS should be used first because it starts the synchronizer to search for a definite framing candidate.

To observe actions of the synchronizer, the Frame Search Restart Flag FRS0.FSRF is implemented. It toggles at the start of a new frame search if no candidate has been found at previous attempt.

When resynchronization is initiated, the following values apply for the time required to achieve the synchronous state in case there is one definite framing candidate within the data stream:

Table 49 Resynchronization Timing (T1/J1)

Frame Mode	Average [ms]	Maximum [ms]
F4	1.0	1.5
F12	3.5	4.5
ESF	3.4	6.125
F72	13.0	17.75

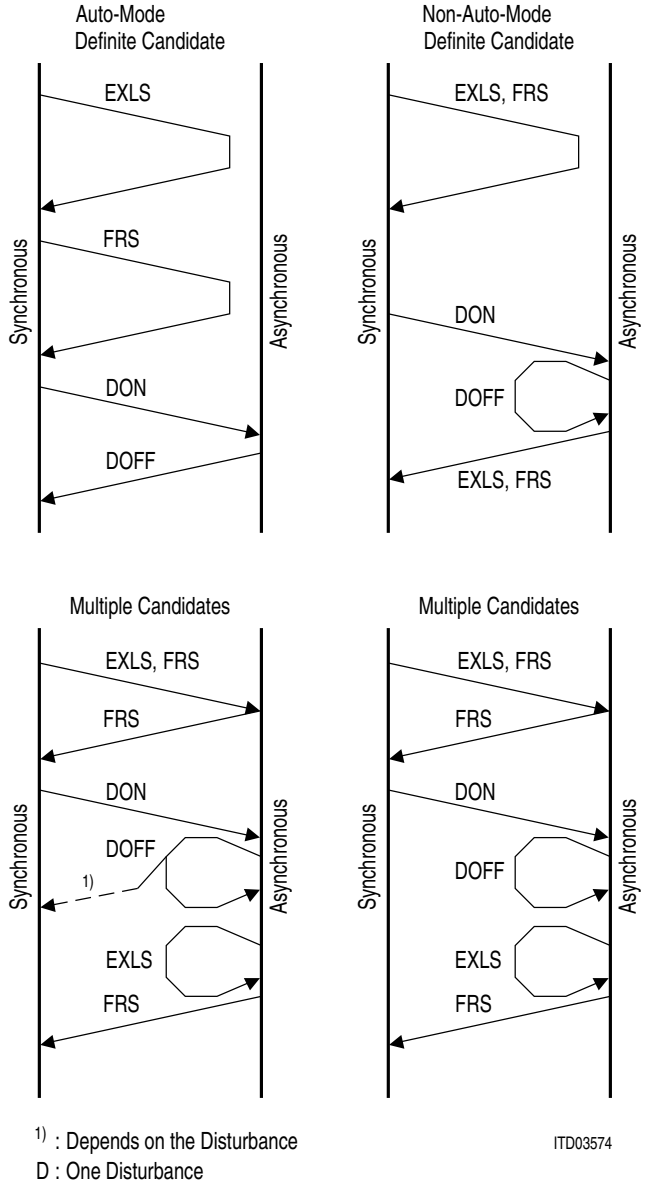


Figure 69 Influences on Synchronization Status (T1/J1)

Figure **Figure 69** gives an overview of influences on synchronization status for the case of different external actions. Activation of auto mode and non-auto mode is performed by bit FMR4.AUTO. Generally, for initiating resynchronization it is recommended to use bit: FMR0.EXLS first. In cases where the synchronizer remains in the asynchronous state, bit FMR0.FRS is used to enforce it to lock onto the next framing candidate, although it might be a simulated one.

5.4.4 4-Frame Multiframe (F4 Format, T1/J1)

The allocation of the FT-bits (bit 1 of frames 1 and 3) for frame alignment signal is shown in **Table 50**.

The FS-bit can be used for signaling. Remote alarm (yellow alarm) is indicated by setting bit 2 to ´0´ in each time slot.

Table 50 4-Frame Multiframe Structure (T1/J1)

Frame Number	FT	FS
1	1	Service bit
2	–	
3	0	Service bit
4	–	

5.4.4.1 Synchronization Procedure (T1/J1)

For multiframe synchronization, the terminal framing bits (FT-bits) are observed. The synchronous state is reached if at least one terminal framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

5.4.5 12-Frame Multiframe (D4 or SF Format, T1/J1)

Normally, this kind of multiframe structure only makes sense when using the CAS robbed-bit signaling. The multiframe alignment signal is located at the FS-bit position of every other frame (refer to **Table 51**).

Table 51 12-Frame Multiframe Structure (T1/J1)

Frame Number	FT	FS	Signaling Channel Designation
1	1	–	A B
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	

There are two possibilities of remote alarm (yellow alarm) indication:

- Bit 2 = ´0´ in each time slot of a frame, selected with bit FMR0.SRAF = ´0´
- The last bit of the multiframe alignment signal (bit 1 of frame 12) changes from ´0´ to ´1´, selected with bit FMR0.SRAF = ´1´.

5.4.5.1 Synchronization Procedure (T1/J1)

In the synchronous state terminal framing (FT-bits) and multiframing (FS-bits) are observed, independently. Further reaction on framing errors depends on the selected synchronization/resynchronization procedure by register bit FMR2.SSP (**FMR2_T**):

- FMR2.SSP = ´0´: terminal frame and multiframe synchronization are combined. Two errors within 4/5/6 framing bits (by bits FMR4.SSC(1:0)) of one of the above leads to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit FRS0.LFA, loss of multiframe alignment is reported by bit FRS0.LMFA. The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulse framing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = ´1´: terminal frame and multiframe synchronization are separated Two errors within 4/5/6 terminal framing bits lead to the same reaction as described above for the “combined” mode. Two errors within 4/5/6 multiframing bits lead to the asynchronous state only for the multiframing. Loss of multiframe alignment

is reported by bit FRS0.LMFA. The state of terminal framing is not influenced. Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

5.4.6 Extended Superframe (F24 or ESF Format, T1/J1)

The use of the first bit of each frame for the multiframe alignment word (FAS) , the data link bits (DL), and the CRC bits is shown in **Table 52**:

Table 52 Extended Superframe Structure (F24, ESF; T1/J1)

Multiframe Frame Number	F-Bits				Signaling Channel Designation
	Multiframe Bit Number	Assignments			
		FAS	DL	CRC	
1	0	–	m	–	
2	193	–	–	e1	
3	386	–	m	–	
4	579	0	–	–	
5	772	–	m	–	
6	965	–	–	e2	A
7	1158	–	m	–	
8	1351	0	–	–	
9	1544	–	m	–	
10	1737	–	–	e3	
11	1930	–	m	–	
12	2123	1	–	–	B
13	2316	–	m	–	
14	2509	–	–	e4	
15	2702	–	m	–	
16	2895	0	–	–	
17	3088	–	m	–	
18	3231	–	–	e5	C
19	3474	–	m	–	
20	3667	1	–	–	
21	3860	–	m	–	
22	4053	–	–	e6	
23	4246	–	m	–	
24	4439	1	–	–	D

5.4.6.1 Synchronization Procedures (T1/J1)

For multiframe synchronization the FAS-bits are observed. Synchronous state is reached if at least one framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

In the synchronous state the framing bits (FAS-bits) are observed. The following conditions selected by the register bits FMR4.SSC(1:0) (**FMR4_T**) lead to the asynchronous state:

- Two errors within 4/5/6 framing bits
- Two or more erroneous framing bits within one ESF multiframe
- More than 320 CRC6 errors per second interval (FMR5.SSC2)
- 4 incorrect (1 out of 6) consecutive multiframes independent of CRC6 errors. There are four multiframe synchronization modes selectable using FMR2.MCSP and FMR2.SSP.
- FMR2.MCSP/SSP = ´00_b´: In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached again, if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state. In asynchronous state, setting bit FMR0.FRS induces the synchronizer to lock onto

the next available framing candidate if there is one. At the same time the internal framing pattern memory is cleared and other possible framing candidates are lost.

- FMR2.MCSP/SSP = ´01_b´: Synchronization is achieved when 3 consecutive multiframe pattern are correctly found independent of the occurrence of CRC6 errors. If only one or two consecutive multiframe pattern were detected the OctalFALC™ stays in the asynchronous state, searching for a possible additionally available framing pattern. This procedure is repeated until the framer has found three consecutive multiframe pattern in a row.
- FMR2.MCSP/SSP = ´10_b´: This mode has been added in order to be able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS leads to synchronization on the next candidate available. However, only the previously assumed candidate is discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer has locked on the right pattern (no extensive CRC errors). The synchronizer is reset completely and initiates a new frame search, if there is no multiframing found. In this case bit FRS0.FSRF toggles.
- FMR2.MCSP/SSP = ´11_b´: Synchronization including automatic CRC6 checking Synchronization is achieved when framing pattern are correctly found and the CRC6 checksum is received without an error. If the CRC6 check failed on the assumed framing pattern the OctalFALC™ stays in the asynchronous state, searching for a possible available framing pattern. This procedure is repeated until the framer has locked on the right pattern. This automatic synchronization mode has been added in order to reduce the microprocessor load.

5.4.6.2 Remote Alarm (yellow alarm) Generation/Detection (T1/J1)

Remote alarm (yellow alarm) is indicated by the periodical pattern "1111 1111 0000 0000 …$_b$" in the DL-bits (T1 mode, RC0.SJR = ´0´). Remote alarm is declared even in the presence of a bit error rate of up to 10^{-3}. The alarm is reset when the yellow alarm pattern no longer is detected.

Depending on bit RC0.SJR = ´1´ the OctalFALC™ generates and detects the remote alarm according to JT G. 704. In the DL-bit position 16 continuous "1" are transmitted if FMR0.SRAF = ´0´ and FMR4.XRA = ´1´.

5.4.6.3 CRC6 Generation and Checking (T1/J1)

Generation and checking of CRC6 bits transmitted/received in the E(6:1) bit positions is done according to ITU-T G.706. The CRC6 checking algorithm is enabled by bit FMR1.CRC. If not enabled, all check bits in the transmit direction are set. In the synchronous state received CRC6 errors are accumulated in a 16-bit error counter and are additionally indicated by an interrupt status.

- CRC6 inversion

If enabled by bit RC0.CRCI, all CRC bits of one outgoing extended multiframe are automatically inverted in case a CRC error is flagged for the previous received multiframe. Setting the bit RC0.XCRCI inverts the CRC bits before transmitted to the distant end. This function is logically ored with RC0.CRCI.

- CRC6 generation/checking according to JT G.706

Setting of RC0.SJR the OctalFALC™ generates and checks the CRC6 bits according to JT G.706. The CRC6 checksum is calculated including the FS/DL-bits. In synchronous state CRC6 errors increment an error counter.

5.4.7 72-Frame Multiframe (SLC96 Format, T1/J1)

The 72-multiframe is an alternate use of the FS-bit pattern and is used for carrying data link information. This is done by stealing some of redundant multiframing bits after the transmission of the 12-bit framing header, see **Table 53**. The position of A and B signaling channels (robbed bit signaling) is defined by zero-to-one and one-to-zero transitions of the FS-bits and is continued when the FS-bits are replaced by the data link bits.

Remote alarm (yellow alarm) is indicated by setting bit 2 to zero in each time slot. An additional use of the D-bits for alarm indication is user defined and must be done externally.

5.4.7.1 Synchronization Procedure (T1/J1)

In the synchronous state terminal framing (FT-bits) and multiframing (FS-bits of the framing header) are observed independently. Further reaction on framing errors depends on the selected synchronization/resynchronization procedure by the register bit FMR2.SSP (**FMR2_T**):

- FMR2.SSP = ´0´: terminal frame and multiframe synchronization are combined Two errors within 4/5/6 framing bits (by bits FMR4.SSC(1:0)) of one of the above lead to the asynchronous state for terminal framing **and** multiframing. Additionally to The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulse framing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = ´1´: terminal frame and multiframe synchronization are separated Two errors within 4/5/6 terminal framing bits lead to the same reaction as described above for the “combined” mode. Two errors within 4/5/6 multiframing bits lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported by bit FRS0.LMFA. The state of terminal framing is not influenced. Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 53 72-Frame Multiframe Structure (T1/J1)

Frame Number	FT	FS	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	B

Table 53 72-Frame Multiframe Structure (T1/J1) (cont'd)

Frame Number	FT	FS	Signaling Channel Designation
13	1	–	
14	–	0	
15	0	–	
16	–	0	
17	1	–	
18	–	1	A
19	0	–	
20	–	1	
21	1	–	
22	–	1	
23	0	–	
24	–	D	B
25	1	–	
26	–	D	
27	.	.	
28	.	.	
.	1	–	
66	–	D	A
67	0	–	
68	–	D	
69	1	–	
70	–	D	
71	0	–	
72	–	0	B

5.4.8 Summary of Frame Conditions (T1/J1)

The summary is shown in **Table 54**:

Table 54 Summary Frame Recover/Out of Frame Conditions (T1/J1)

Format	Frame Recover Condition	Out of Frame Condition
F4	Only one FT pattern found, optional forcing on next available FT framing candidate	2 out of 4/5/6 incorrect FT-bits

Table 54 Summary Frame Recover/Out of Frame Conditions (T1/J1) (cont'd)

Format	Frame Recover Condition	Out of Frame Condition
F12 (D4) and F72 (SLC96)	FMR2.SSP = ´0´: Combined FT + FS framing search: First searching for FT pattern with optional forcing on next available framing candidates and then for 2 consecutive correct FS pattern[1]. FMR2.SSP = ´1´: Separated FT + FS pattern search: Loss of FT framing starts first search for FT and then for 2 consecutive correct FS pattern1). Loss of FS framing starts only the FS pattern1) search.	FMR2.SSP = ´0´: 2 out of 4/5/6 incorrect FT- or FS-bits FMR2.SSP = ´1´: 2 out of 4/5/6 incorrect FT-bits searched in FT and FS framing bits, 2 out of 4/5/6 incorrect FS-bits searched only the FS framing.
F24 (ESF)	FMR2.MCSP/SSP = ´00_b´: only one FAS pattern found, optional forcing on next available FAS framing candidate with discarding of all remaining framing candidates. FMR2.MCSP/SSP = ´01_b´: 3 consecutive correct multiframing found independent of CRC6 errors. FMR2.MCSP/SSP = ´10_b´: choosing multiple framing pattern step by step, optional forcing on next available FAS framing pattern with discarding only of the previous assumed framing candidate. FMR2.MCSP/SSP = ´11_b´: FAS framing correctly found and CRC6 check error free.	2 out of 4/5 incorrect FAS-bits or 2 out of 6 incorrect FAS-bits per multiframe or 4 consecutive incorrect multiframing pattern or more than 320 CRC6 errors per second interval

1) In F12 (D4) format bit 1 in frame 12 is excluded from the synchronization process.

5.5 Additional Receive Framer Functions (T1/J1)

The additional framer functions are described in the following chapters:

5.5.1 Error Performance Monitoring and Alarm Handling (T1/J1)

- Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled by bit FMR1.XAIS.
- Loss-Of-Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.
- Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA and ISR2.RA/RAR. Transmission is enabled by bit FMR4.XRA. The automatic transmit remote alarm feature in case of LFA can be enabled by setting FMR2.AXRA.
- Severely Errored Frames, see also **Chapter 5.5.1.1**.
- Excessive Zeros: Detection is flagged by bit FRS1.EXZD.
- Pulse-Density Violation: Detection is flagged by bit FRS1.PDEN and ISR0.PDEN.
- Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC, see also **Chapter 3.7.6**
- Transmit ´Ones´-Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC.

Table 55 Summary of Alarm Detection and Release (T1/J1)

Alarm	Detection Condition	Clear Condition
Red Alarm or Loss-Of-Signal (LOS)	No transitions (logical zeros) in a programmable time interval of 16 to 4096 consecutive pulse periods. Programmable receive input signal threshold	Programmable number of ones (1 to 256) in a programmable time interval of 16 to 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold. or The pulse-density is fulfilled and no more than 15 contiguous zeros during the recovery interval are detected.
Blue Alarm or Alarm Indication Signal (AIS)	FMR4.AIS3 = ´0´: less than 3 zeros in 12 frames or 24 frames (ESF), FMR4.AIS3 = ´1´: less than 4 zeros in 12 frames or less than 6 zeros in 24 frames (ESF)	Active for at least one multiframe. FMR4.AIS3 = ´0´: more than 2 zeros in 12 or 24 frames (ESF), FMR4.AIS3 = ´1´: more than 3 zeros in 12 frames or more than 5 zeros in 24 frames (ESF)
Yellow Alarm or Remote Alarm (RRA)[1)]	RC1.RRAM = ´0´: bit 2 = ´0´ in 255 consecutive time slots or FS-bit = ´1´ of frame12 in F12 (D4) format or 8 x 1, 8 x 0 in the DL channel (ESF) RC1.RRAM = ´1´: bit 2 = ´0´ in every time slot per frame or FS-bit = 1 of frame12 in F12 (D4) format or 8 x 1, 8 x 0 in the DL channel (ESF)	RC1.RRAM = ´0´: set conditions no longer detected. RC1.RRAM = ´1´: bit 2 = ´0´ not detected in 3 consecutive frames or FS-bit not detected in 3 consecutive multiframes or 8 x 1, 8 x 0 not detected for 3 times in a row (ESF).
Severely Errored Frames (SEF) Indication	Two or more frame bit errors in the timing window are detected.	Signal is in-frame and there are less than two frame bit errors in the timing window
Excessive Zeros (EXZD)	More than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros	Latched Status: cleared on read
Pulse-Density Violation (PDEN)	Less than N ones in each and every time window of 8 x(N+1) time slots with N taking all values of 1 to 23 or more than 15 consecutive zeros	Latched Status: cleared on read
Transmit Line Short (XLS)	More than 3 pulse periods with highly increased transmit line current on XL1/2	Transmit line current limiter inactive
Transmit ´Ones´-Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

1) RRA detection operates in the presence of 10^{-3} bit error rate.

5.5.1.1 Severely Errored Frame Indication SEF (T1/J1)

An SEF interrupt statusbit ISR7.SEFEI (**ISR7_T**) and an appropriate mask register bit IMR7.SEFEI is provided, which shows if severely errored frames (SEF) were detected according to ANSI-T1.231 chapter 6.1.2.2.2.

An SEF defect is determined by examining contiguous time windows for frame bit errors. For SF the window size is 0.75 ms, and only the F_T bits are examined. For ESF the window size is 3 ms, and only the frame pattern sequence (FPS) bits are examined.

Note that an AIS-CI and an AIS signal (alarm indication signal) or a signal that is OOF (out of frame) will typically cause an SEF defect.

For indication and clear condition see **Table 55**.

5.5.2 Automatic Modes (T1/J1))

In T1/J1 mode the following automatic modes are performed by the OctalFALC™:

- Automatic remote alarm (Yellow Alarm) access: If the receiver has lost its synchronization (FRS0.LFA) a remote alarm (yellow alarm) is sent to the distant end automatically, if enabled by bit FMR2.AXRA. In synchronous state the remote alarm bit is removed.
- Automatic AIS to system interface: In asynchronous state the synchronizer enforces an AIS to the receive system interface automatically. However, received data is switched through transparently if bit FMR2.DAIS is set.
- Automatic clock source switching: In slave mode (LIM0.MAS = ´0´) the DCO-R synchronizes on the recovered route clock. In case of loss-of-signal (LOS) the DCO-R switches to master mode automatically. If bit CMR1.DCS is set, automatic switching from recovered route clock to SYNC is disabled, see also **Table 16**.
- Automatic transmit clock switching, see **Chapter 3.7.3**.
- Automatic freeze signaling: Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is activated automatically, if a loss-of-signal or a loss of multiframe alignment or a receive slip occurs. The internal signaling buffer RS(12:1) is frozen. Optionally automatic freeze signaling is disabled by setting bit SIC3.DAF = ´1´.
- Automatic local and remote loop switching based on In-Band loop codes, see **Chapter 5.5.7**.
- Automatic payload and remote loop switching based on Out-Band loop codes, see **Chapter 5.5.8**.

5.5.3 Error Counter (T1/J1)

The OctalFALC™ offers six error counters where each of them has a length of 16 bit. They record code violations, framing bit errors, CRC6 bit errors, errored blocks and the number of received multiframes in asynchronous state or the changes of frame alignment (COFA):

- Frame Errror Counter (FEC), see **Chapter 5.5.3.1**.
- COFA event counter
- PRBS Bit Error Counter (BEC)
- CRC Error Counter (CEC)
- Errored Block counter.
- Code violation counter.

Counting of the counters can be disabled by appropriate bits in the register DEC (**DEC_T**).

Counting of the multiframes in asynchronous state and of the COFA parameter is done in a 6/2-bit counter. Each of the error counters is buffered. Buffer update is done in two modes:

- One-second accumulation
- On demand using handshake with writing to the DEC register.

In the one-second mode an internal/external one-second timer updates these buffers and resets the counter to accumulate the error events in the next one-second period. The error counter cannot overflow. Error events occurring during error counter reset are not be lost.

5.5.3.1 Frame Error Counter FEC (T1/J1)

The kind of count up behaviour of the frame error counter FEC can be controlled in the OctalFALC™ by the register bit DEC.FECC (**DEC_T**) because there are differences in the ANSI standard T1- 403 between 1995 and 1999:

- FEC count up will be done also if a severely error occurs as it is described in ANSI-T1-403 1995: DEC.FECC = ´0´.
- FEC count up is not done if a simultaneous severely error occurs as described in ANSI-T1-403 1999: DEC.FECC = ´1´.

Note that the FEC status is stored in the registers FECH and FECL.

5.5.4 Errored Second (T1/J1)

The OctalFALC™ supports the error performance monitoring by detecting the following alarms or error events in the received data: framing errors, CRC errors, code violations, loss of frame alignment, loss-of-signal, alarm indication signal, receive and transmit slips. With a programmable interrupt mask register ESM all these alarms or error events can generate an Errored Second Interrupt (ISR3.ES) if enabled.

5.5.5 One-Second Timer (T1/J1)

A one-second timer interrupt can be generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The one-second timer signal is output on port SEC/FSC (GPC1.CSFP1/0). Optionally synchronization to an external second timer is possible which has to be provided on pin SEC/FSC. Selecting the external second timer is done with GCR.SES.

In compatibility mode of the OctalFALC™ (pin COMP = ´1´) the register GPC1 (global port configuration register 1, **GPC1_T**) is used in every of the both pseudo QuadFALC® s to configure the sources of FSC out of the 4 channels. So with these one GPC1 register per pseudo QuadFALC® its only possible to control a 4:1 multiplexer. But really eight channels exists in the OctalFALC™ and therefor 8:1 multiplexing must be performed, because only one FSC/SEC pin exists in the OctalFALC™. **Figure 70** shows the principle of the solution using an additional 2:1 multiplexer.

The 2:1 multiplexer is controlled by the register bits GPC1.CSFP(1:0) of the second Pseudo QuadFALC®: If the SEC/FSC pin is configured as output by these bits, the second Pseudo QuadFALC® is the source of SEC/FSC. Enable of the SEC/FSC pin as output is performed by the register bits GPC1.CSFP(1:0) of the first and the second Pseudo QuadFALC® were all are logical ored.

For COMP = ´0´ the one global GPC2 register is used instead of the both GPC1 registers in compatibility mode.

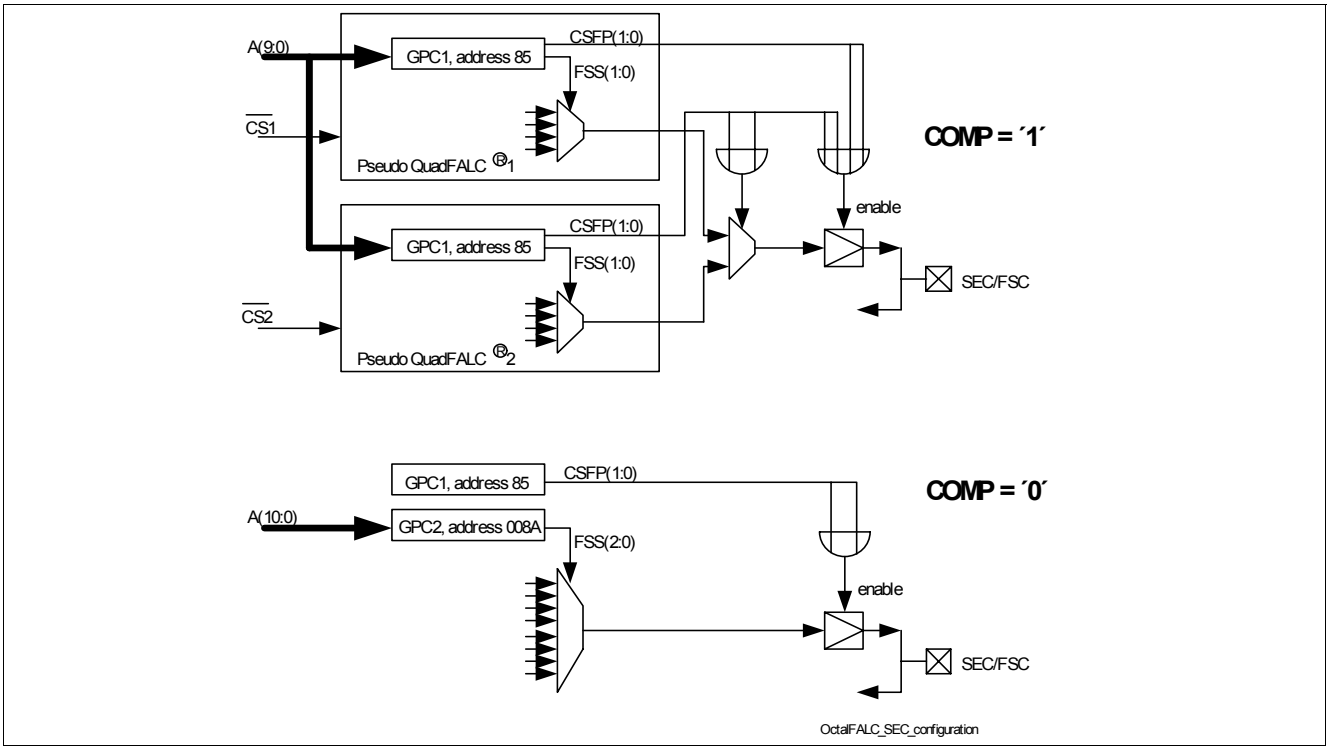


Figure 70 Principle of Configuring the SEC/FSC Pin

5.5.6 Clear Channel Capability (T1/J1)

For support of common T1 applications, clear channels can be specified through the 3-byte register bank CCB(1:3). In this mode the contents of selected transmit time slots are not overwritten by internally or externally sourced bit-robbing and zero code suppression (B7 stuffing) information. See also **Chapter 5.3.3**.

5.5.7 In-Band Loop Generation, Detection and Loop Switching (T1/J1)

In-band Signaling is an unchannelized signaling method. All data bits of all time slots of a frame can be used by the In-band signaling information.

Detection and generation of In-band Loop code is supported by the OctalFALC™ on the line side and on the system side independent from another.

The OctalFALC™ generates and detects framed or unframed In-band codes. The so called loop-up code (for loop activation) and loop-down code (for loop deactivation) are recognized. If the 1. bit of a frame (frame bit) is used for In-Band signaling it is the so called “unframed” signaling, otherwise it is called “framed” signaling. The selection between framed or unframed in-band loop code is done by LCR1.FLLB.

The maximum allowed bit error rate within the loop codes can be up to 10^{-2} for proper detection of the loop codes. One “In-band loop sequence” consists of a bitsequence of 51200 consequtive bits. The In-band loop code detection is based on the examination of such “In-band loop sequences”.

The following In-band loop code functionality is performed by the OctalFALC™:

- The necessary reception time of In-band loop codes until an automatic loop switching is performed is configured for the system side by the register bits INBLDTR.INBLDT(1:0) (**INBLDTR_T**). Configuring for the line side is done by INBLDTR.INBLDR(1:0). If for example INBLDTR.INBLDR(1:0) = ´00_b´ a time of 16 “In-band loop sequences” (16 x 51200 bits) is selected for the line side.
- The interrupt status register bits ISR6.(3:0) reflects the type of detected In-band loop code. Masking can be done by IMR6(3:0). The status bits are set after one “In-band loop sequence” is detected (no dependency on INBLDTR).
- Transmission of In-Band loop codes is enabled by programming FMR3.XLD/XLU. Transmission of codes is done by the OctalFALC™ for at least 5 seconds.
- The OctalFALC™ also offers the ability to generate and detect user defined In-band loop-up and loop-down patterns (LCR1.LLBP = ´1´) (**LCR1_T**). Programming of these patterns is done in registers LCR2 and LCR3 (**LCR2_T**). The pattern length is individually programmable in length from 5 to 8 bits by LCR1.LAC(1:0) and LCR1.LDC(1:0). A shorter pattern can be inplemented by configuring a repeating pattern in the LCR2 and LCR3.
- Automatic loop switching (activation and deactivation, for remote loop, see **Chapter 5.7.2** and local loop, see **Chapter 5.7.4**) based on In-band Loop codes can be done. Two kinds of line loop back (LLB) codes are defined in ANSI-T1.403, 1999 in chapter 9.4.1.1 and 9.4.1.2. respectively. Automatic loop switching must be enabled through configuration register bits ALS.SILS (**ALS_T**) for the In-Band Loop codes coming from the system side and ALS.LILS for the In-Band Loop codes coming from the line side respectively. Masking of ISR6.(3:0) for interrupt can be done by register bits IMR6.(3:0). The interrupt status register bits ISR6.(3:0) will be set to ´1´ if an appropriate In-Band code were detected, independent if automatic loop switching is enabled. (Because the controller knows if automatic loop switching is enabled, it knows if a loop is activated or not.) Code detection status only for the line side is displayed in status register bits RSP.LLBDD and RSP.LLBAD.

Detection and generation of In-Band Loop code is supported on line and system side independent from each other.

Framed and unframed In-Band loop code can be generated and detected.

Automatic loop switching is logically OR´d with the appropriate loop switching by register bits.

If a remote loop is activated by an automatic loop switching the register bit LIM0.JATT controls also if the jitter attenuator is active or not.

If ALS.LILS is set, the remote loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) was detected from the line side and if the local loop is not activated by LIM0.LL = ´1´. The remote loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) was detected from the line side. (But if the remote loop is additionally activated by LIM0.RL = ´1´ the remote loop is still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

If ALS.SILS is set, the local loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) is detected from the system side. The local loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) is detected from the system side. (But if the local loop is additionally activated by LIM0.LL = ´1´ the local loop is still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

ALS.SILS and ALS.LILS both must not be set to ´1´ simultaneous.

If ALS.SILS or ALS.LILS are set after an In-Band loop code is detected, no automatic loop switching is performed.

If ALS.LILS is cleared, an automatic activated remote loop is deactivated.

If ALS.SILS is cleared, an automatic activated local loop is deactivated.

The detected type of In-Band loop code is indicated in the interrupt status register bits ISR6.(3:0).

To avoid lock up of the OctalFALC™ an activation of the remote loop is not possible by In-band loop codes if the local loop (see **Chapter 5.7.4**) is closed (LIM0.LL is set).

5.5.8 Bit Oriented Messages (BOM): Generation, Detection and Loop Switching (T1/J1)

The OctalFALC™ performes the following functionalities regarding the Out-band loop codes (bit oriented messages, BOM) on all eight channels independent from each other:

- Detection of Out-band loop codes (BOM), see **Chapter 5.3.4**.
- Generation of Out-band loop codes (BOM) by setting of the appropriate DL-bits by the micro controller, see **Chapter 5.3.6.1**.
- Automatic loop switching (activation and deactivation, for remote loop, see **Chapter 4.7.2** and payload loop, see **Chapter 4.7.3**) based on detected Out-band loop codes.

Loop switching (“Out-band loop switching”) is possible by enabling of the BOM receiver 1 signaling (MODE.BRAC = ´1´ and CCR1.EITS = ´1´) and detection of the following Out-Band loop messages related to ANSI-T1.403, 1999, table4:

Table 56 Out-band loop messages for loop switching (T1/J1)

Function	Message (BOM Code)
Line loopback activate	´00001110 11111111$_b$´
Line loopback deactivate	´00111000 11111111$_b$´
Payload loopback activate	´00010100 11111111$_b$´
Payload loopback deactivate	´00110010 11111111$_b$´
Universal loopback deactivate	´00100100 11111111$_b$´

If the register bit CCR2.RBFE is set, BOM messages are accepted if at least seven consecutive and identical BOM messages were received.

Dependent on the BOM mode (configured by register bits CCR1.BRM and CCR2.RBFE) the content of register RSIS will be written as last byte into the receive FIFO.

Automatic loop switching by BOM messages is logically ored with the appropriate loop switching by register bits.

If ALS.SOLS (**ALS_T**) is set, the payload loop is activated after the “payload loopback activate“ code was detected from the line side or the system side and if the local loop is not activated by LIM0.LL = ´1´. The payload loop is deactivated after an appropriate deactivation Out-Band loop code was detected from the line side or the system side. (But if the payload loop is additionally activated by FMR2.PLB = ´1´ the payload loop is still active, because automatic loop switching is logically ored with the appropriate loop switching by register bits.)

If ALS.LOLS is set, the remote loop is activated after the “line loopback activate” code was detected from the line side or the system side and if the local loop is not activated by LIM0.LL = ´1´. The remote loop is deactivated after the “line loopback deactivate” code was detected from the line side or the system side. (But if the remote loop is additionally activated by LIM0.RL = ´1´ the remote loop is still active, because automatic loop switching is logically ored with the appropriate loop switching by register bits.)

If the remote loop is activated by an automatic loop switching the register bit LIM0.JATT controls also if the jitter attenuator is active or not.

ALS.SOLS and ALS.LOLS both can be set to ´1´ simultaneous.

Because BOM messages coming from the system side are not included in the E1/T1/J1 standards, receive of these BOM messages and the possibility of automatic loop switching (ALS.SOLS) are features of the OctalFALC™. It has to be handle carefully to avoid deadlocks.

If ALS.SOLS or ALS.LOLS are set after an Out-Band loop code was detected, no automatic loop switching is performed.

If ALS.LOLS is cleared, an automatic activated remote loop is deactivated.

If ALS.SOLS is cleared, an automatic activated payload loop is deactivated.

The kind of performed automatic loop switching caused by the appropriate detected Out-band message is shown in the register bits ISR6.(7:4). Masking of ISR6.(7:4) for controlling of the interrupt can be done by register bits IMR6.(7:4). If an Out-band message were detected, the appropriate register bits ISR6.(7:4) will be set to ´1´, independent if automatic loop switching has been enabled. (Because the micro controller knows if automatic loop switching is enabled, it knows if a loop is activated or not.)

A detection of an Out-band loop message (BOM) “universal loopback deactivate” sets both bits ISR6.SOLSD and ISR6.LOLSD, independent if a loop is active (switched) or not. Dependent on ALS.LOLS or ALS.SOLS the remote or the payload loopback is switched off respectively.

A received BOM message causes setting of the interrupt bit ISR0.RME and is stored in the receive FIFO, marked with a BOM frame.

Note that detection of Out-band Loop messages (BOM codes) is only possible either on the line side or the system side, dependent on the configuration of the HDLC controller (see **Chapter 5.3.1**): If the HDLC/BOM controller 1 is attached to the line side (MODE.HDLCI = ´0´) only BOM messages coming from the line side can be detected. If the HDLC/BOM controller is attached to the system side (MODE.HDLCI = ´1´), so called “inverse configuration”) only BOM messages coming from the system side can be detected. BOM messages coming from the system side are not included in (ANSI-)standards, but can be handled by the OctalFALC™.

5.5.9 Transparent Mode (T1/J1)

The transparent modes are useful for loop-backs or for routing data unchanged through the OctalFALC™.

In receive direction, transparency for ternary or dual-/single-rail unipolar data is always achieved if the receiver is in the synchronous state. All bits in F-bit position of the incoming multiframe are forwarded to RDO and inserted in the FS/DL time slot or in the F-bit position. In asynchronous state the received data is switched through transparently if bit FMR2.DAIS (**FMR2_T**) is set. Setting of bit LOOP.RTM (**LOOP_T**) disconnects control of the elastic buffer from the receiver. The elastic buffer is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of resynchronization of the receiver. Together with FMR2.DAIS this function is used to realize undisturbed transparent reception.

Setting bit FMR4.TM switches the OctalFALC™ in transmit transparent mode:

In transmit direction bit 8 of the FS/DL time slot from the system highway (XDI) is inserted in the F-bit position of the outgoing frame. For complete transparency the internal signaling controller, idle code generation, AIS alarm generation, single channel and payload loop-back has to be disabled and cleared channels have to be defined by registers CCB(3:1).

5.5.10 Pulse-Density Detection (T1/J1)

The OctalFALC™ examines the receive data stream on the pulse-density requirement which is defined by ANSI T1. 403. More than 14 consecutive zeros or less than N ones in each and every time window of 8 x (N+1) data bits where N = 23 are detected. Violations of these rules are indicated by setting the status bit FRS1.PDEN and the interrupt status bit ISR0.PDEN. Generation of the interrupt status is programmed either with the detection or with any change of state of the pulse-density alarm (GCR.SCI).

5.6 System Interface in T1/J1 Mode

The OctalFALC™ offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The system interface of the OctalFALC™ consists on

- The eight system interfaces of the eight channels, see **Figure 71**. It also includes the multi function ports, see **Chapter 3.8** .

- The system interface multiplexer/demultiplexer, see **Chapter 5.6.1** with **Figure 72**: It multiplexes the received data RDO and RSIG of four or eight channels into one or two common data streams and it demultiplexes the data XDI and XSIG from one or two common data streams to four or eight channels.

Configuring of the whole system interface consists on

- Configuration of the timing of the system interfaces of the eight channels, see **Chapter 5.6.2** and **Chapter 5.6.3**
- Configuration of the multi function ports of the eight channels, see **Chapter 3.8**
- Configuration of the multiplex mode of the system multiplexer/demultiplexer, see **Chapter 5.6.1**.

The interfaces of every of the channels to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The interfaces of every of the channels to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The receive highway is clocked on pin SCLKR, while the interface to the transmit system highway is independently clocked either on pin SCLKX or on the clock of the receive highway. The frequency of these working clocks - so called as “internal receive clock” and internal transmit clock” - and the data rate of 2.048/4.096/8.192/16.384/ 1.544/3.088/6.192/12.352 Mbit/s for the receive and transmit system interface is programmable by SIC1.SSC(1:0), and SIC1.SSD1, FMR1.SSD0. If the source of the internal receive clock is the DCO-R output or the recovered receive clock, SCLKR must be configured as output by setting PC5.CSRP. If the source is SCLKR, these pin must be configured as input. Selectable system clock and data rates and their valid combinations are shown in **Table 57**.

Table 57 System Clocking and Data Rates (T1/J1)

System Highway Data Rate	System Interface Clock Rate 1.544/2.048 MHz	System Interface Clock Rate 3.088/4.096 MHz	System Interface Clock Rate 6.176/8.192 MHz	System Interface Clock Rate 12.352/16.384 MHz
1.544/2.048 Mbit/s	x	x	x	x
3.088/4.096 Mbit/s	--	x	x	x
6.176/8.192 Mbit/s	--	--	x	x
12.352/16.384 Mbit/s	--	--	--	x

x = valid, -- = invalid

Generally the receive/transmit data or marker on the system interface are clocked off/latched on the rising or falling edge of the SCLKR/SCLKX clock:

- Selection of the edge for the receive/transmit data and marker is done by the register bits SIC3.RESR/X (**SIC3_T**).
- Selection of the edge for the sync pulses $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ in relation to the edge of the receive/transmit data and marker can be done individually by the register bits SIC4.SYPRCE/SYPXCE (**SIC4_T**): Either the same edge or the opposite edge in relation to the used edge of the data and marker is possible.

Some clocking rates allow transmission of time slots in different channel phases. Each channel phase which shall be active on ports RDO, XDI, RP(A:C) and XP(A:B) is programmable by bit SIC2.SICS(2:0) (**SIC2_T**), the remaining channel phases are cleared or ignored.

The signals on pin $\overline{\text{SYPR}}$ in combination with the assigned time slot offset in register RC0 and RC1 define the beginning of a frame on the receive system highway. The signal on pin $\overline{\text{SYPX}}$ or XMFS together with the assigned time slot offset in register XC0 and XC1 define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ or XMFS is possible in the range of 0 to 125 µs. The minimum shift of varying the time slot 0 begin can be programmed between 1 bit and 1/8-bit depending of the system clocking and data rate, e.g. with a clocking/data rate of 2.048 MHz shifting is done bit by bit, while running the OctalFALC™ with 16.384 MHz and 2.048 Mbit/s data rate it is done by 1/8 bit.

A receive frame marker RFM can be activated during any bit position of the entire frame. The pin function RFM is selected by PC(3:1).RPC(3:0) = ´0001_b´. The RFM selection disables the internal time slot assigner, no offset

programming is performed. The receive frame marker is active high for one 1.544/2.048 MHz cycle and is clocked off with the rising or falling edge of the clock which is in/output on port SCLKR (see SIC3.RESX/R).

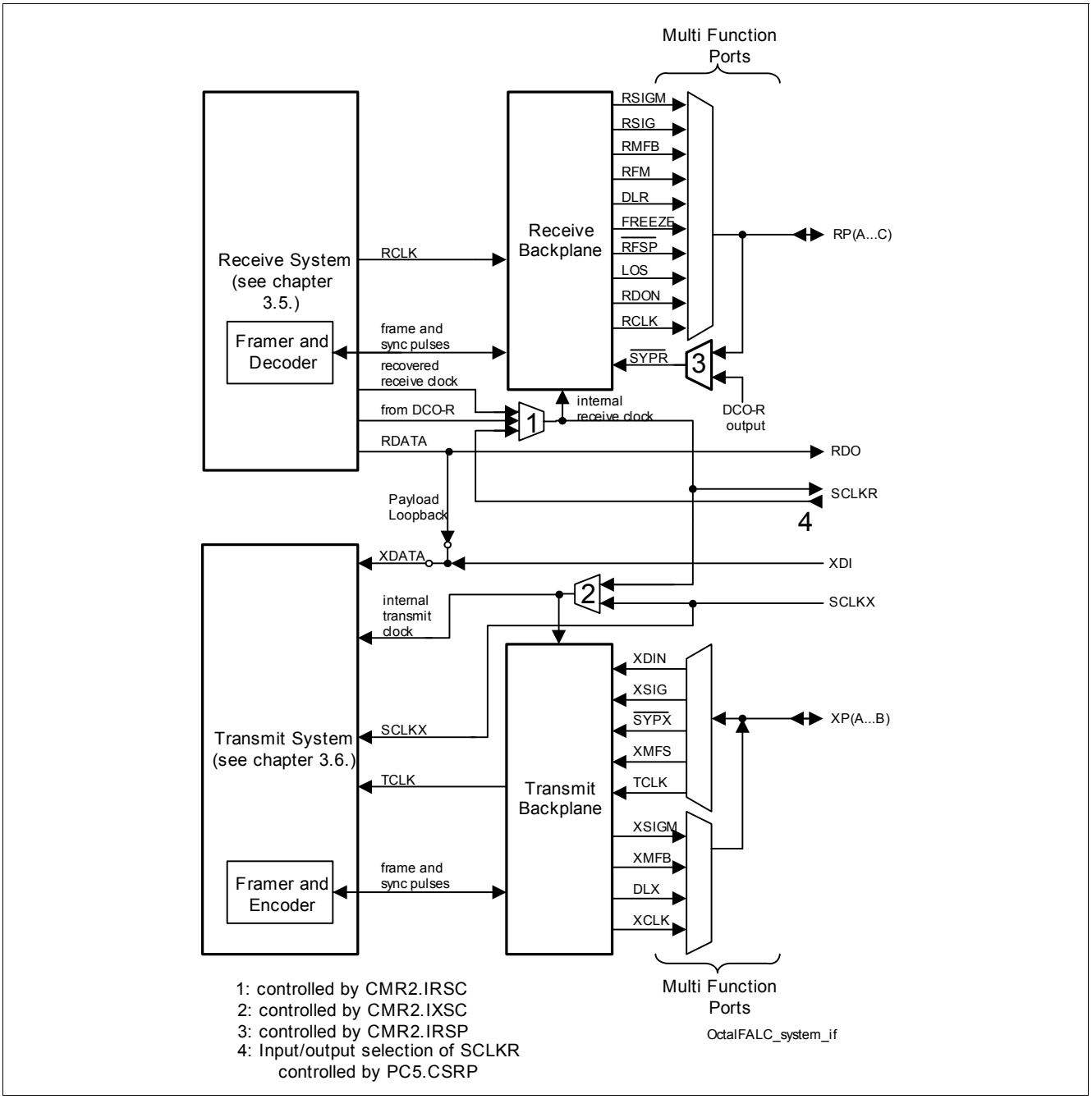


Figure 71 System Interface of one Channel

5.6.1 System Multiplexer/Demultiplexer (T1/J1)

The system multiplexer/demultiplexer of the OctalFALC™ is shown in **Figure 72**.

In receive direction multiplexing of the received data RDO(1:8) of the eight channels into either two data streams at RDO1 and RDO5 or into one data stream at RDO1 is performed. In the same way the signals RSIG(1:8) are multiplexed either into two signaling streams using the multi function ports RPB1, and RPB5 or into one signaling stream using RPB1.

In transmit direction demultiplexing either from two data streams at XDI1 and XDI5 or from one data stream at XDI1 onto the transmit data XDI(1:8) of the eight channels is performed. In the same way multiplexing either from

two signaling streams using the multi function ports XPB1,5 or from one signaling stream using XPB1 onto the signals XSIG(1:8) is performed.

All other signals which are configured at the multi function ports were not multiplexed/demultiplexed, see **Figure 72**.

The following modes are supported, see **Table 58** and **Figure 73** where only the pins RDO are shown.

- 8-to-1 Multiplex Mode at 16 Mbit/s. Multiplexing is done on port 1 (RPB1, XPB1). Output pins of the other ports are set to tristate input pins of the other ports are unused.
- Dual 4-to-1 Multiplex Mode at 8 Mbit/s. Multiplexing is done on port 1 (RPB1, XPB1) and port 5 (RPB5, XPB5). Output pins of the other ports are undefined, input pins of the other ports are unused.
- Dual 4-to-1 Multiplex Mode at 16 Mbit/s. Multiplexing is done on port 1 and port 5 where four phases are unused on every port. Disjunct phases must be used on both ports. 16 Mbit/s multiplexing is done by external logical or on the PCB. Output RDO is driven to low level for inactive phases. Output pins of the other ports are undefined, input pins of the other ports are unused.

Switching into Multiplex Modes is done by setting of the register bit GPC1.SMM (**GPC1_T**).

Switching between 8-to-1 Multiplex Mode (using only one port) and QuadFALC® compatible 4:1 Multiplex Modes (using two or more ports) is done by the register bit GPC6.SSI16 (**GPC6_T**).

Multiplexing of RSIG is done in the same way as shown for RDO in **Figure 73**. Demultiplexing of XDI and XSIG is done vice versa.

To perform the system interface mode the following configuration of the multi function ports must be identical for all channels.

- SYPR has to be provided on RPA (PC1.RPC1(2:0) = ´0000_b´).
- SYPX or XMFS has to be provided on XPA (PC1.XPC1(2:0) = ´0001_b´).
- XSIG has to be provided on XPB (PC2.XPC1(2:0) = ´0010_b´).
- RSIG must be output on RPB (PC2.RPC1(2:0) = ´0100_b´).

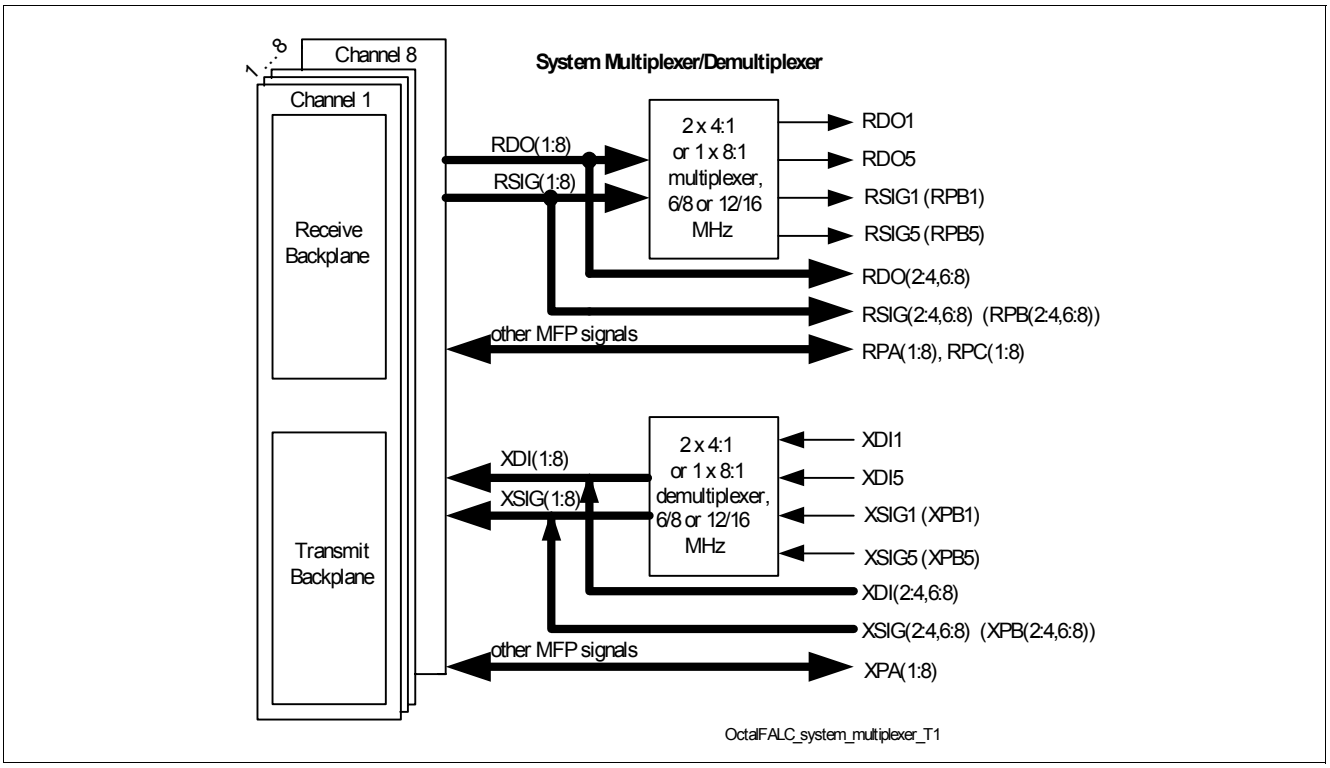


Figure 72 System Multiplexer/Demultiplexer (T1/J1)

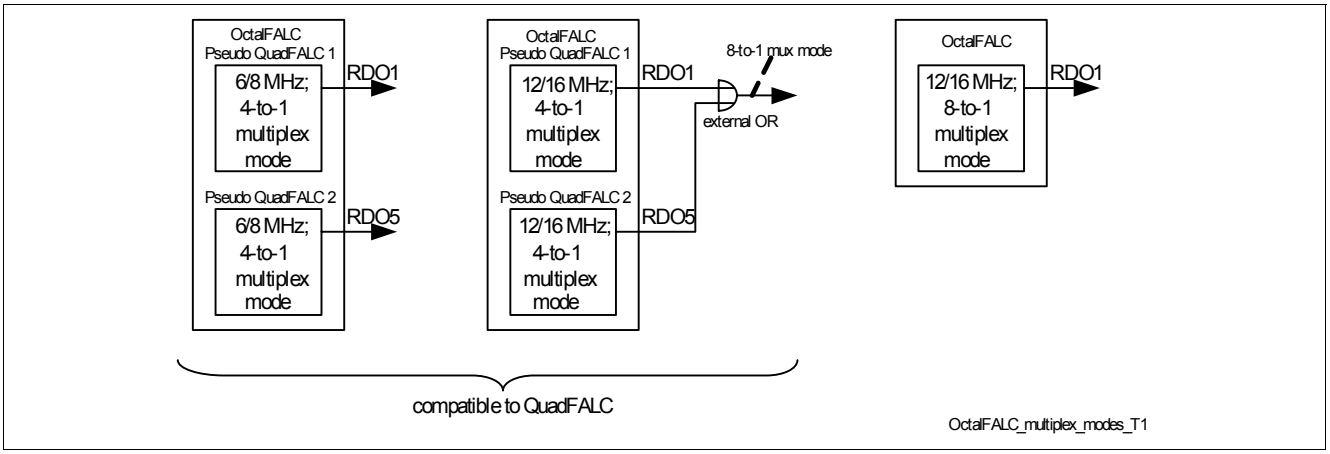


Figure 73 System Multiplex Modes in T1/J1, shown for RDO only

Table 58 System Multiplex Modes (T1/J1)

GPC1.SMM	GPC6.SSI16	Multiplex Mode
0	0	no multiplexing/demultiplexing
0	1	Not defined
1	0	4:1 multiplexing/demultiplexing with 6.176 Mbit/s or 12.325 Mbit/s dependent on SIC1.SSD1 and SIC1.SSC(1:0) For COMP = ´1´: setting of 4:1 multiplexing/demultiplexing can be done individually in both pseudo QuadFALC® s dependent on the both GPC1.SMM bits. for COMP = ´0´: 4:1 multiplexing/demultiplexing is performed in both of the pseudo QuadFALC® s dependent on the one GPC1.SMM bit
1	1	8:1 multiplexing/demultiplexing with 12.325 Mbit/s For COMP = ´1´: GPC1.SMM bits of both pseudo QuadFALC® s must be set to ´1´. (for COMP = ´0´: only the one GPC1.SMM bit must be set)

5.6.2 Receive System Interface (T1/J1)

The timing of the receive system interface is shown in **Figure 74**.

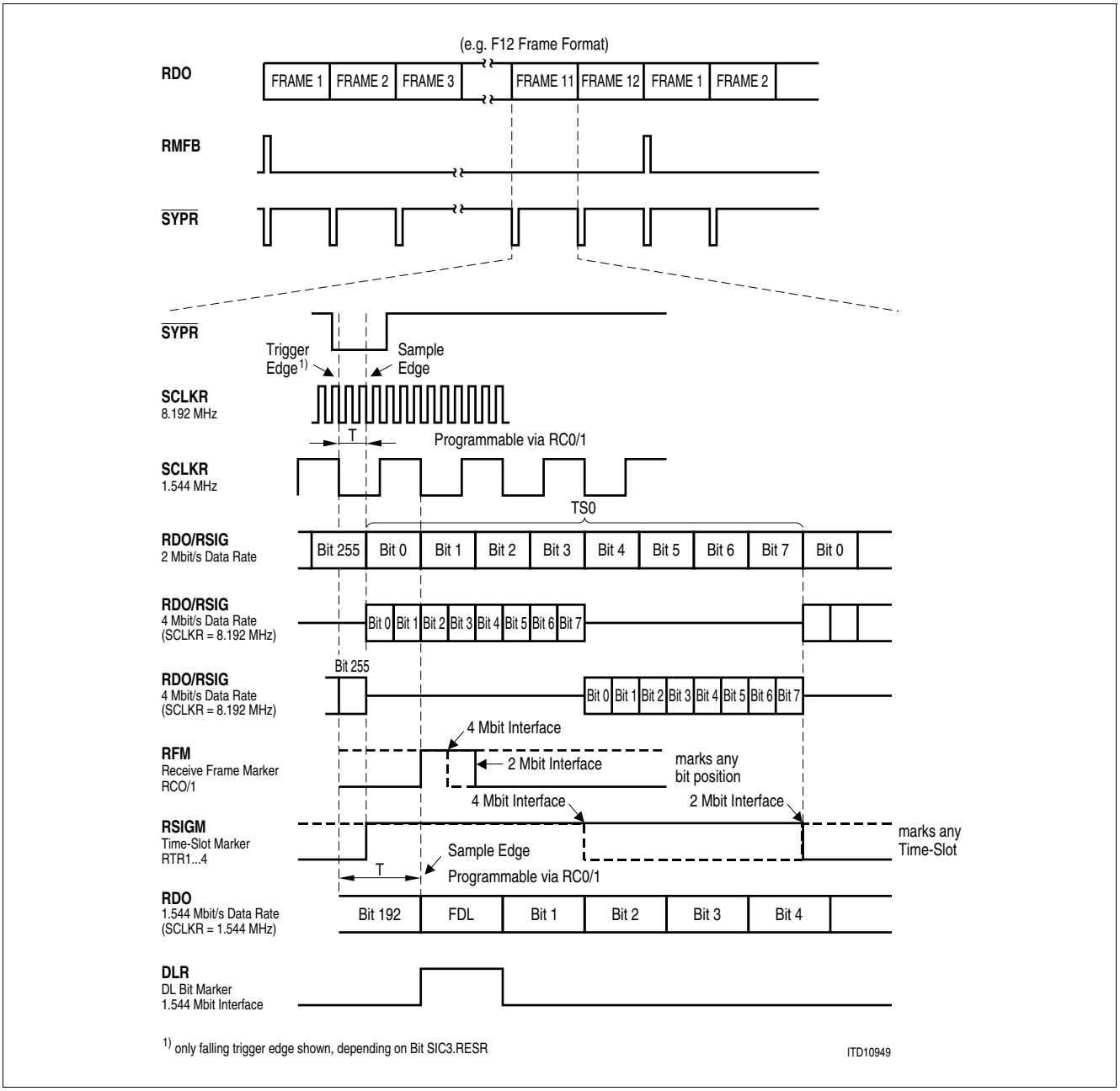


Figure 74 Receive System Interface Clocking (T1/J1)

5.6.2.1 Receive Offset Programming (T1/J1)

Depending on the selection of the synchronization signals ($\overline{\text{SYPR}}$ or RFM), different calculation formulas are used to define the position of the synchronization pulses. These formulas are given below, see Figure 61 to **Figure 78** for explanation. The pulse length of RFM is always the basic T1/J1 bit width (648 ns) in 1.544 MHz mode or the E1 bit width (488 ns) in 2.048 MHz mode. The figures and offset calculations are valid for SIC4.SYPRCE = ´0´ ($\overline{\text{SYPR}}$ related to the same edge of SCLKR as the data and marker).

This chapter describes the system highway operation in 1.544 MHz mode only. If the system highway is operated in 2.048 MHz mode, the description given in **Chapter 4.6.2.1** on **Page 143** applies.

$\overline{\text{SYPR}}$ Offset Calculation

T: Time between beginning of $\overline{\text{SYPR}}$ pulse and beginning of next frame (time slot 0, bit 0), measured in number of SCLKR clock intervals maximum delay: T_{max} = (193 x SC/SD) - 1

SD: Basic data rate; 1.544 Mbit/s

SC: System clock rate; 1.544, 3.088, 6.176, or 12.352 MHz

X: Programming value to be written to registers RC0 and RC1 (see Page 359).

0 ≤ T ≤ 4: **X = 4 - T + (7 ° SC/SD)**

5 ≤ T ≤ Tmax: **X = (200 ° SC/SD) + 4 - T**

RFM Offset Calculation

MP: Marker position of RFM, counting in SCLKR clock cycles (0 = F-bit)

SC = 1.544 MHz: 0 ≤ MP ≤ 192

SC = 3.088 MHz: 0 ≤ MP ≤ 385

SC = 6.176 MHz: 0 ≤ MP ≤ 771

SC = 12.352 MHz: 0 ≤ MP ≤ 1543

SD: Basic data rate; 1.544 Mbit/s

SC: System clock rate; 1.544, 3.088, 6.176, or 12.352 MHz

X: Programming value to be written to registers RC0 and RC1 (see Page 359).

0 ≤ MP ≤ 193 ° (SC/SD) - 3: **X = MP + 2 + (7 ° SC/SD)**

193 ° (SC/SD) - 2 ≤ MP ≤ 193 ° (SC/SD) - 1: **X = MP + 2 - (186 ° SC/SD)**

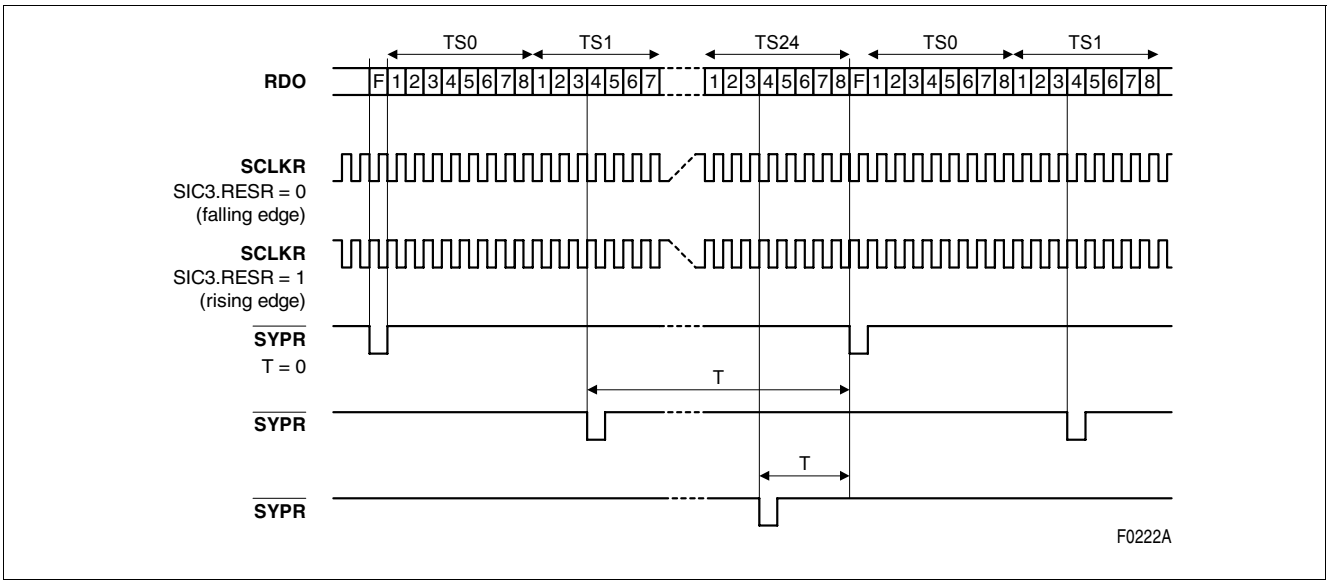


Figure 75 $\overline{\text{SYPR}}$ Offset Programming (1.544 Mbit/s, 1.544 MHz)

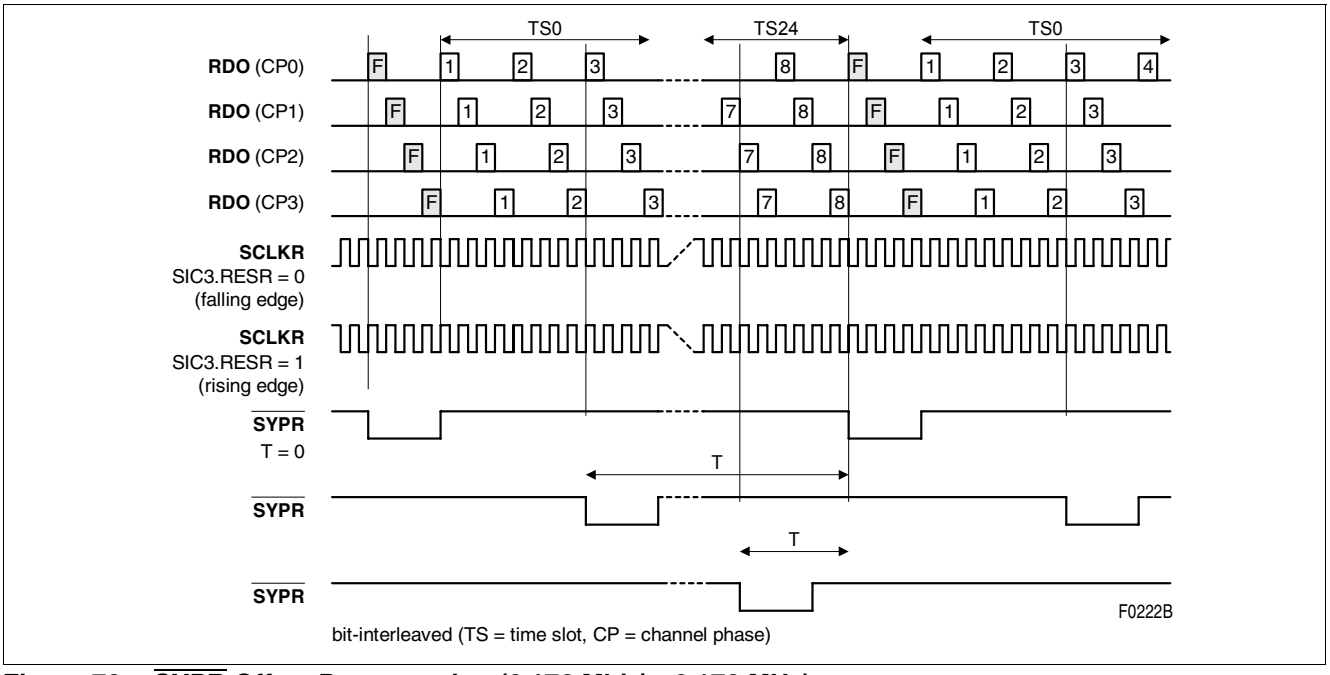


Figure 76 $\overline{\text{SYPR}}$ Offset Programming (6.176 Mbit/s, 6.176 MHz)

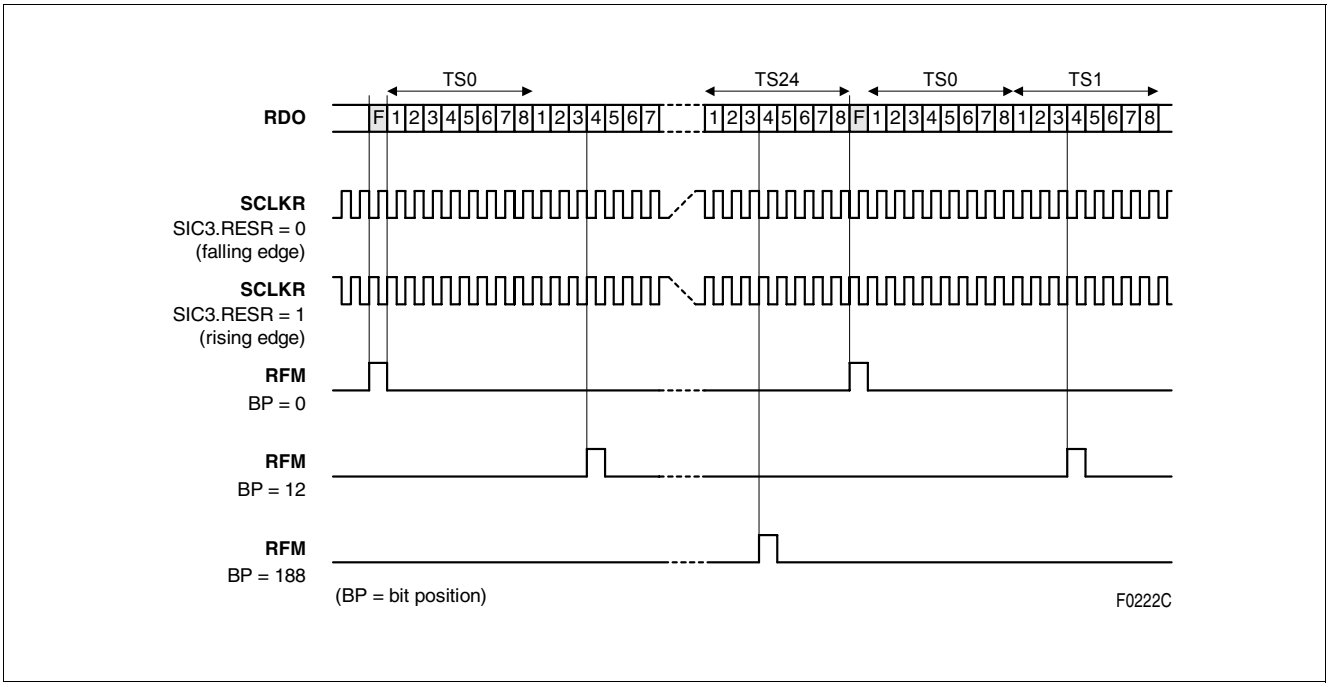


Figure 77 RFM Offset Programming (1.544 Mbit/s, 1.544 MHz)

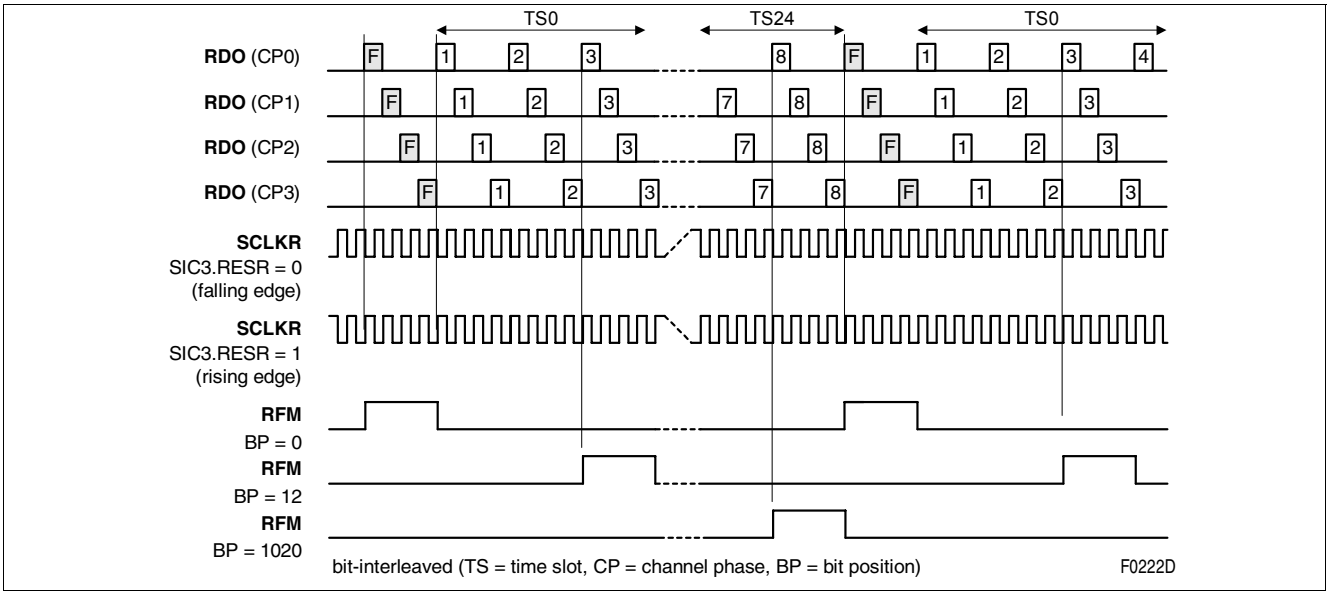


Figure 78 RFM Offset Programming (6.176 Mbit/s, 6.176 MHz)

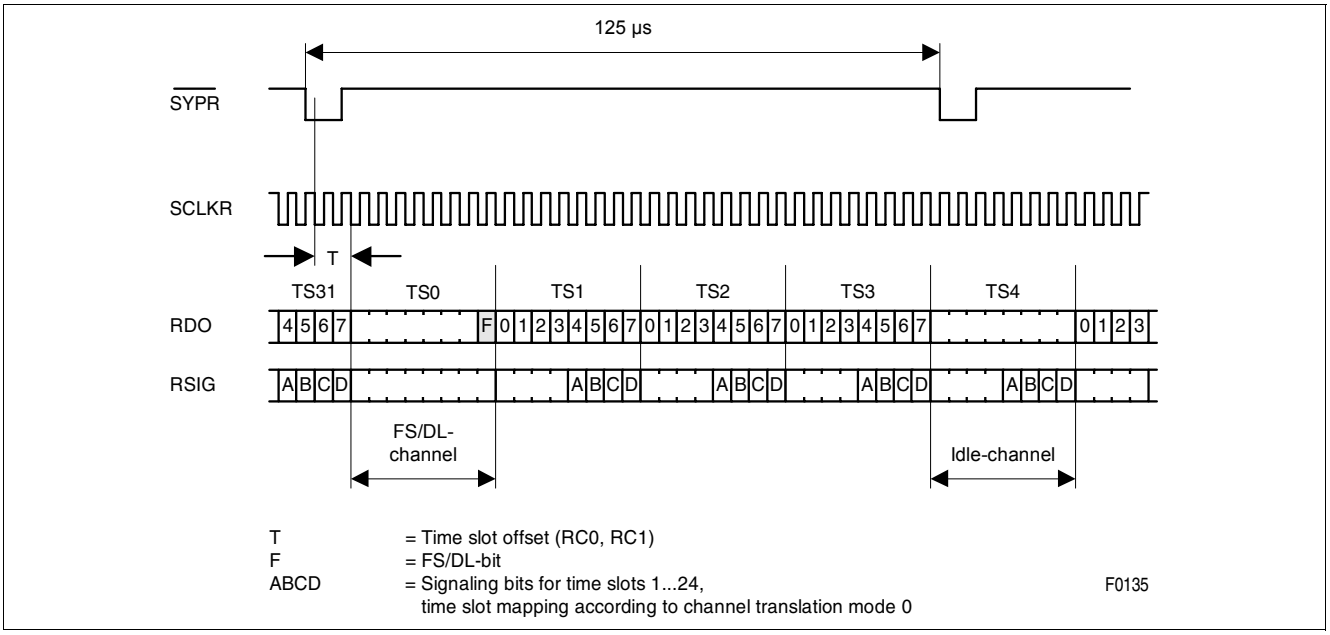


Figure 79 2.048 MHz Receive Signaling Highway (T1/J1)

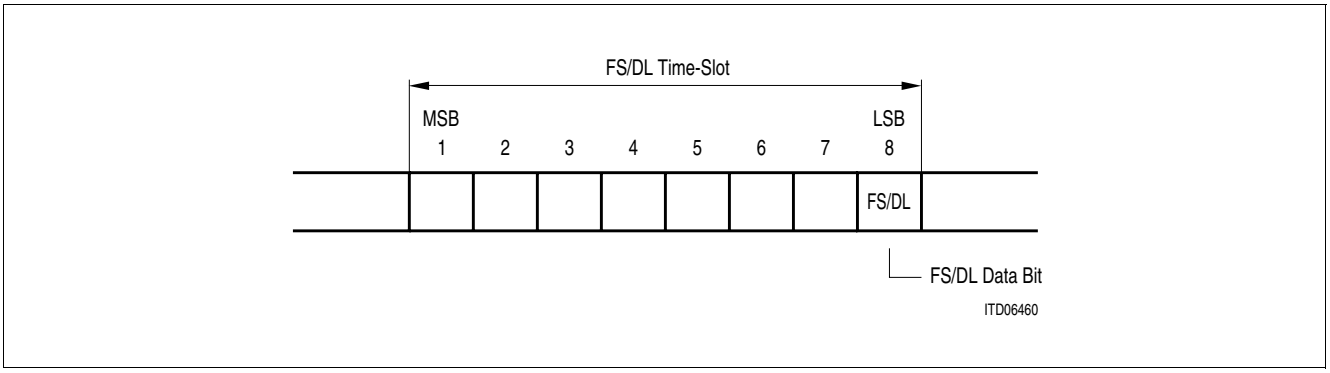


Figure 80 Receive FS/DL-Bits in Time Slot 0 on RDO (T1/J1)

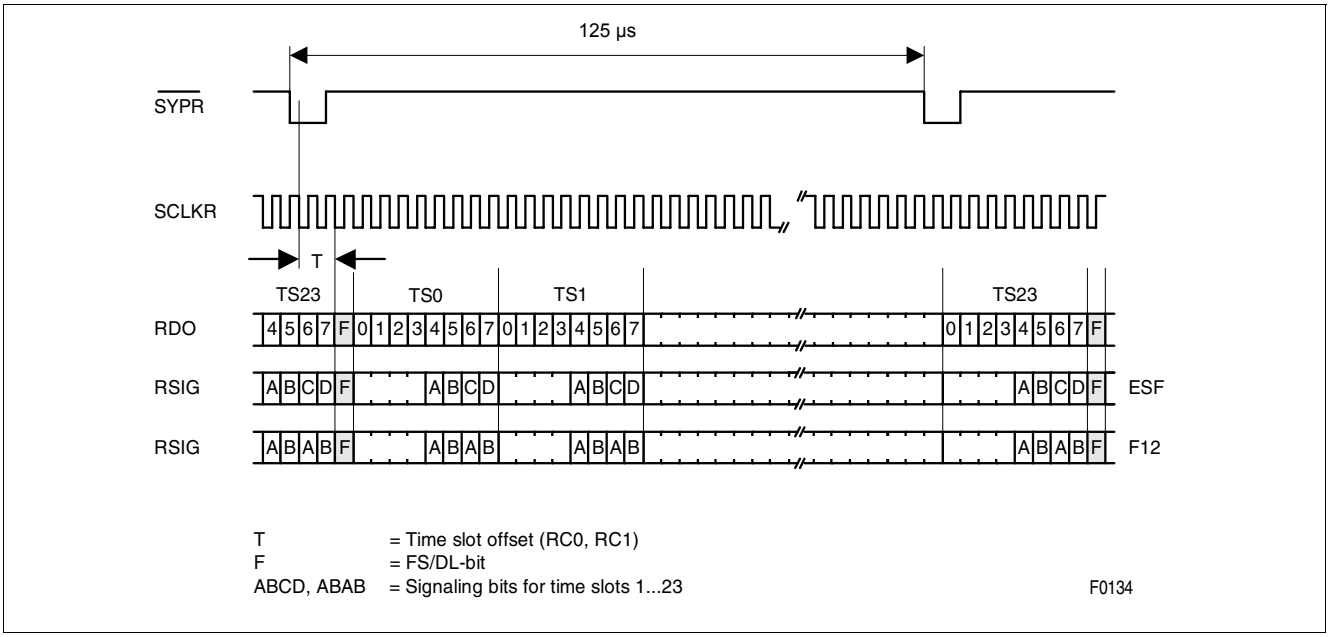


Figure 81 1.544 MHz Receive Signaling Highway (T1/J1)

5.6.3 Transmit System Interface (T1/J1)

Compared to the receive paths the inverse functions are performed for the transmit direction.

The figures and offset calculations are valid for SIC4.SYPXCE = ´0´ ($\overline{\text{SYPX}}$ related to the same edge of SCLKX as the data and marker).

The received bit stream on ports XDI and XSIG can be multiplexed internally on a time slot basis, if enabled by SIC3.TTRF = ´1´. The data received on port XSIG can be sampled if the transmit signaling marker XSIGM is active high. Data on port XDI is sampled if XSIGM is low for the corresponding time slot. Programming the XSIGM marker is done with registers TTR(4:1).TS(0:7) (**TTR1_T**).

Note: XSIG is required in the last frame of a multiframe only and ignored in all other frames.

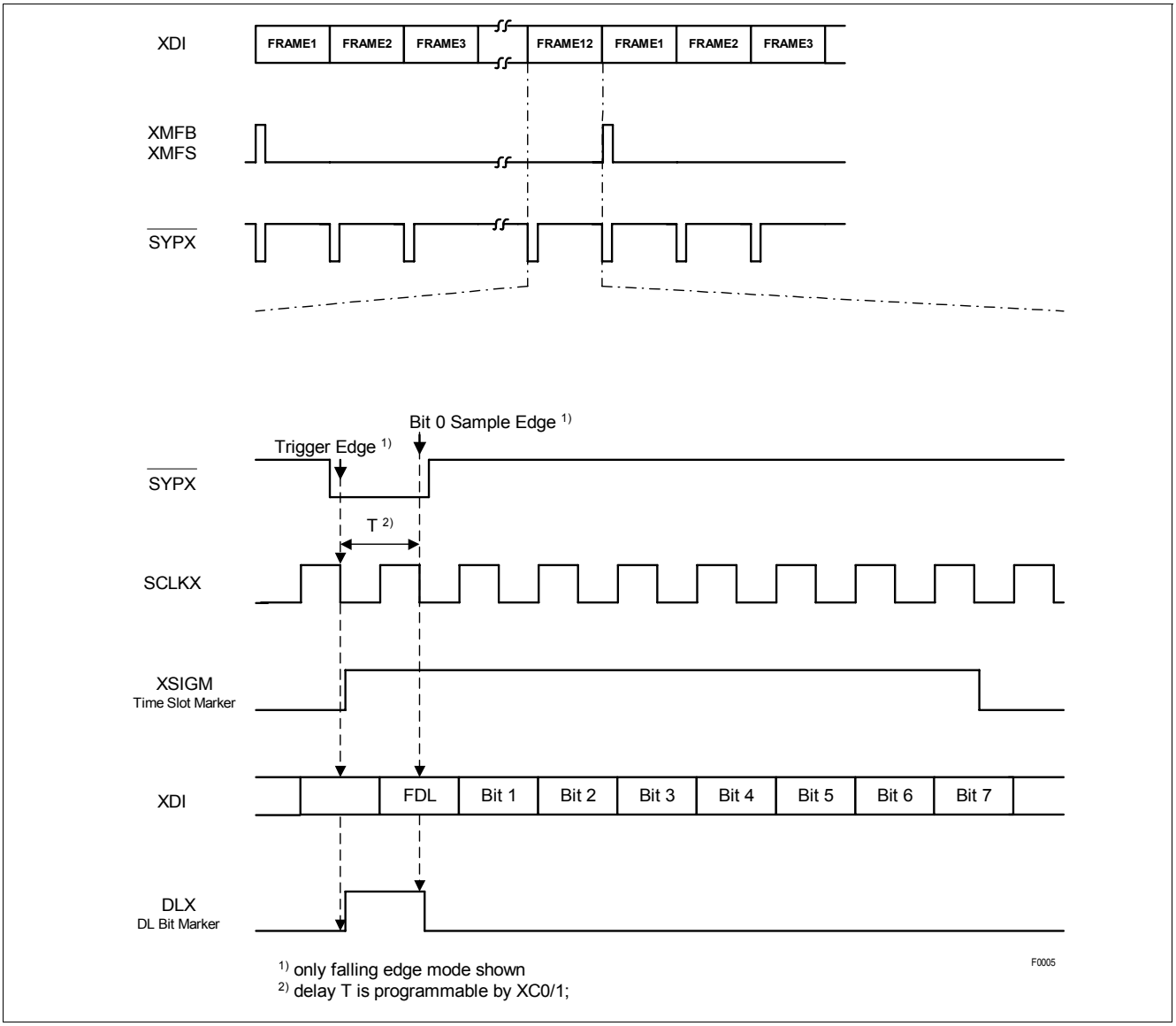


Figure 82 Transmit System Clocking: 1.544 MHz (T1/J1)

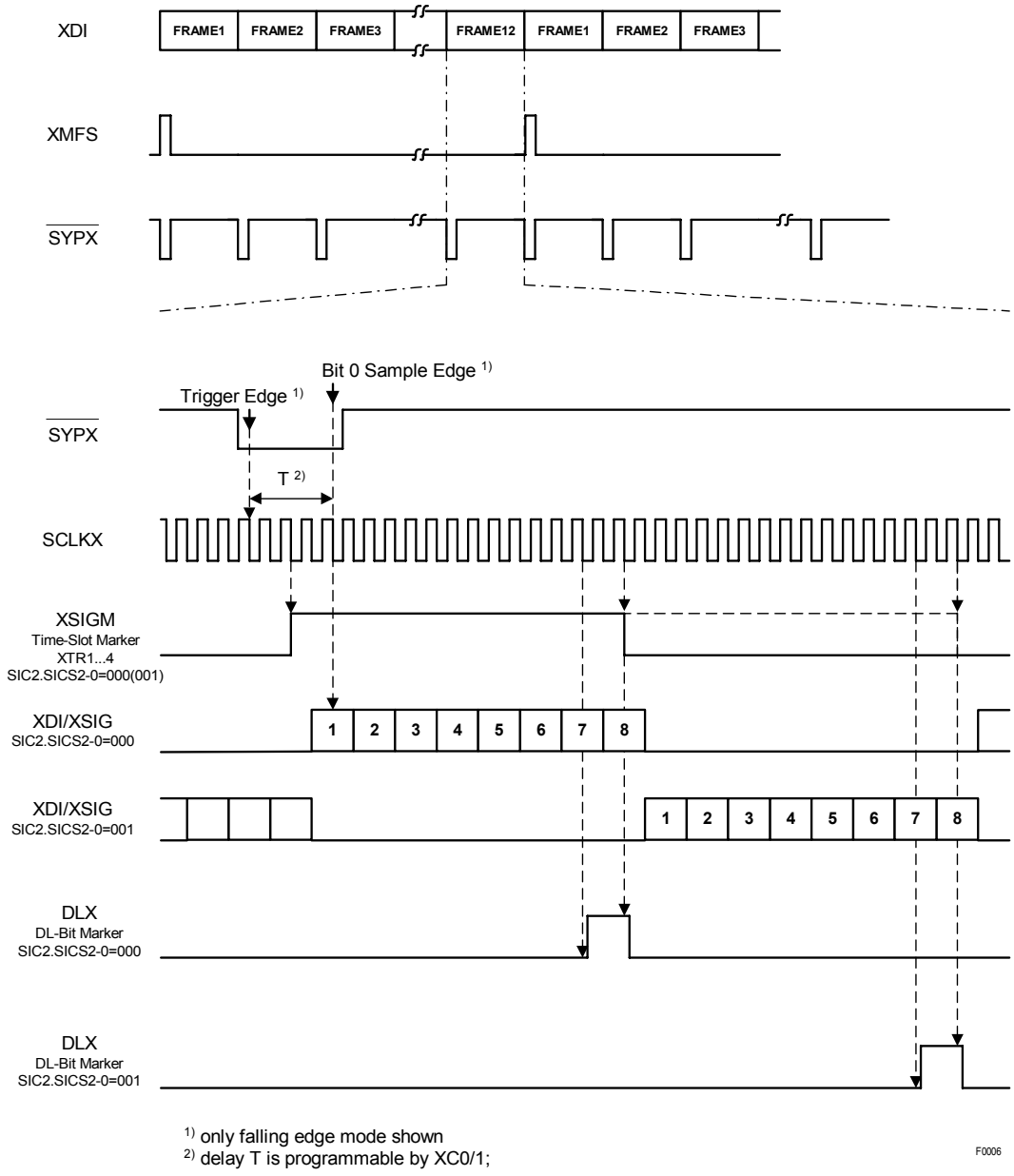


Figure 83 Transmit System Clocking: 8.192 MHz/4.096 Mbit/s (T1/J1)

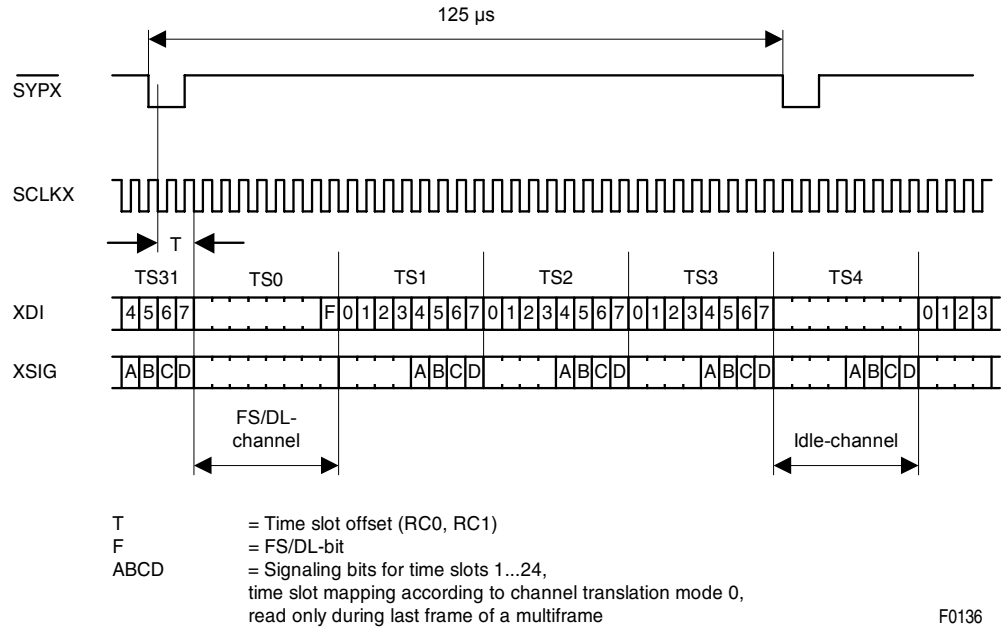


Figure 84 2.048 MHz Transmit Signaling Clocking (T1/J1)

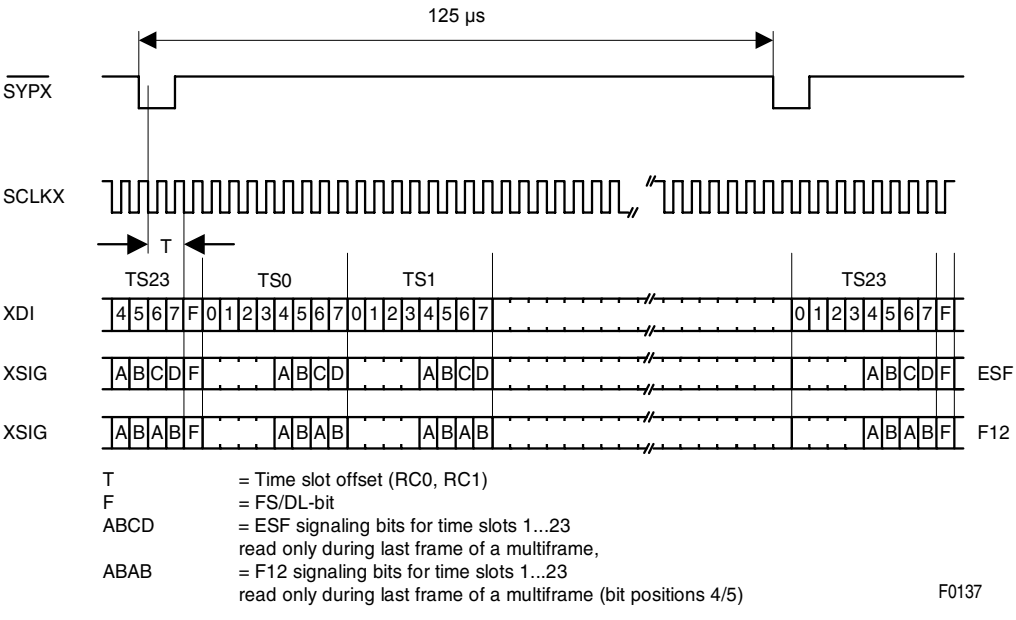
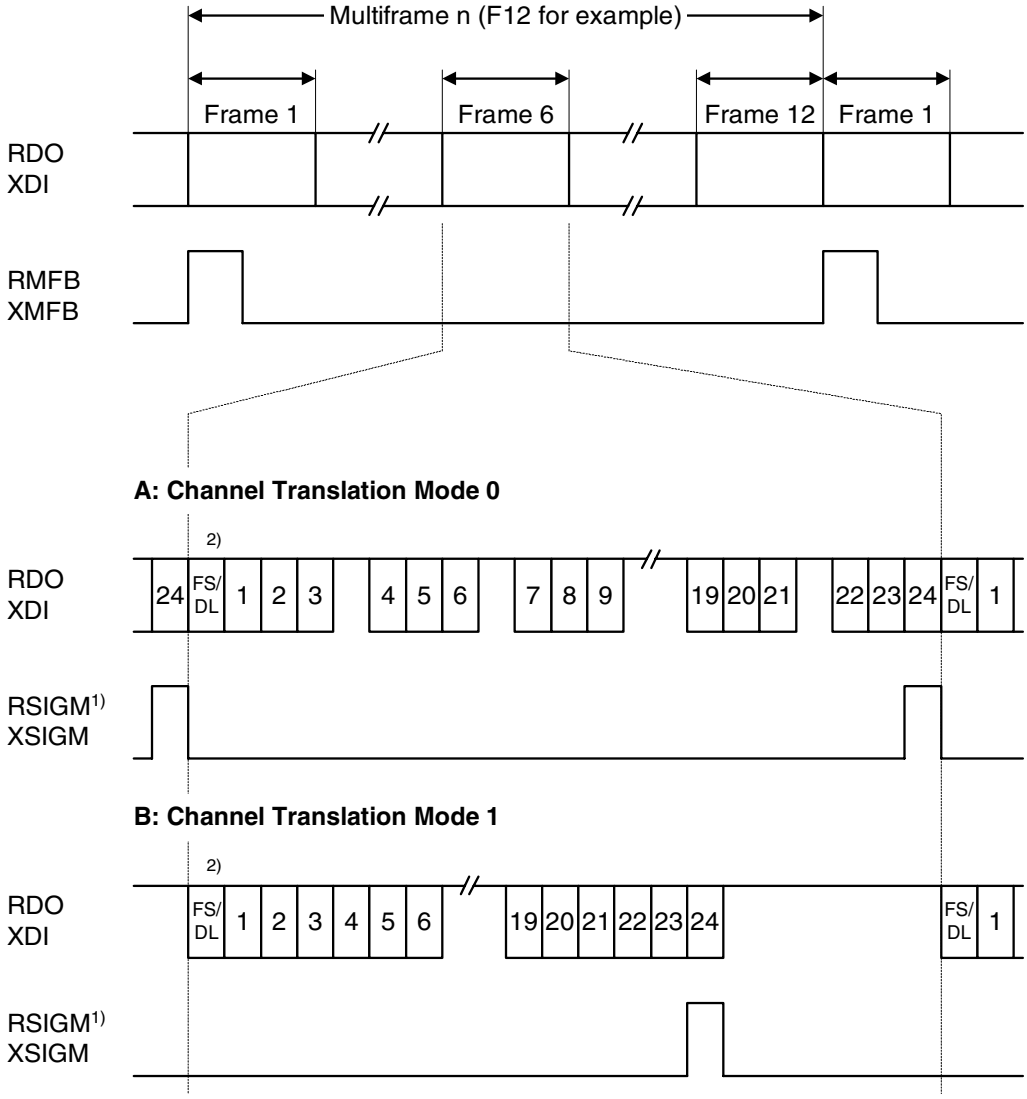


Figure 85 1.544 MHz Transmit Signaling Highway (T1/J1)



Notes:

1) RSIGM and XSIGM are programmed to mark only channel 24 in this example (via RTR(4:1) and TTR(4:1)).

2) FS/DL is don't care on XDI

F0267_1

Figure 86 Signaling Marker for CAS/CAS-CC Applications (T1/J1)

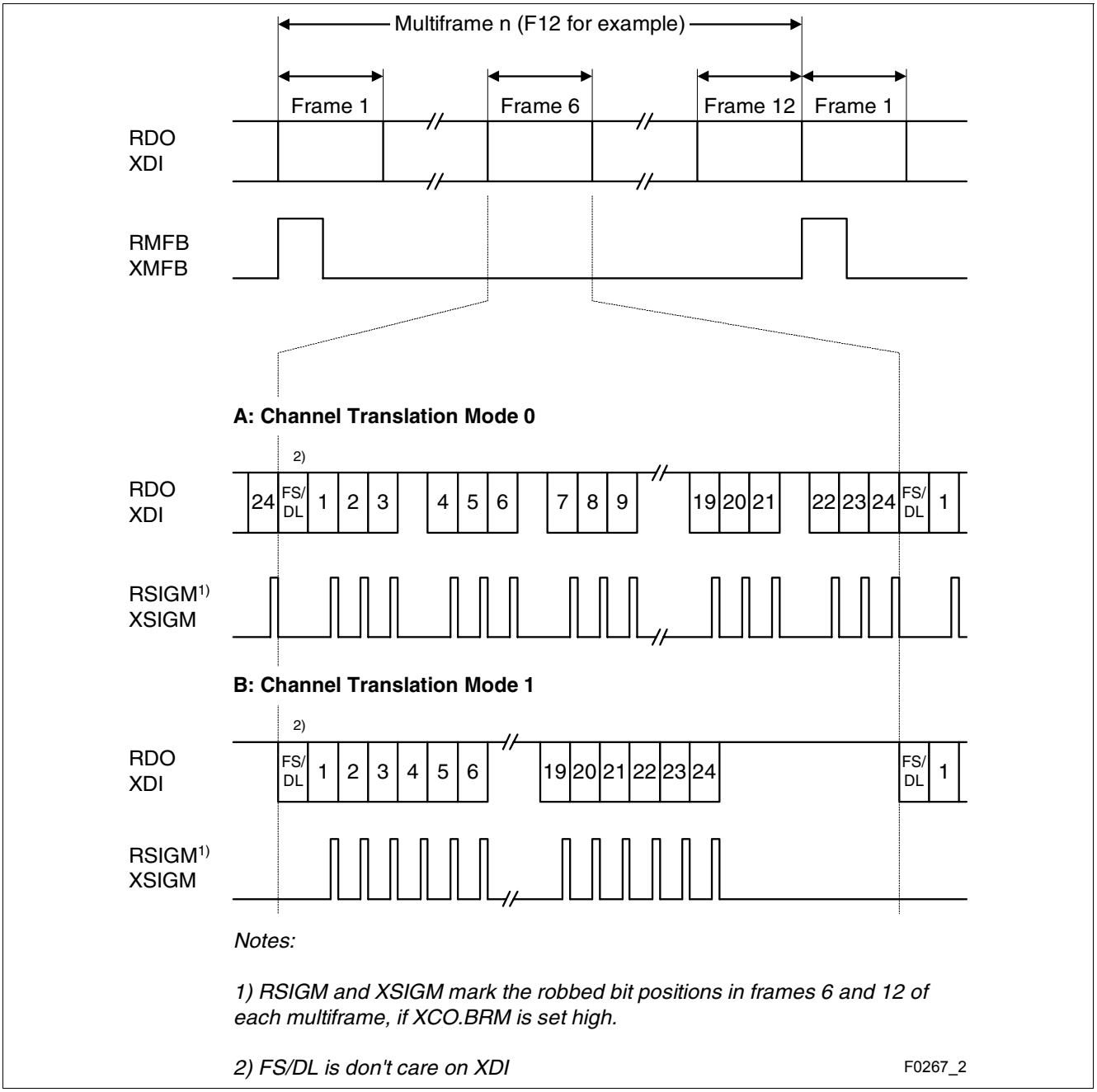


Figure 87 Signaling Marker for CAS-BR Applications (T1/J1)

FS/DL data on system transmit highway (XDI), time slot 0:

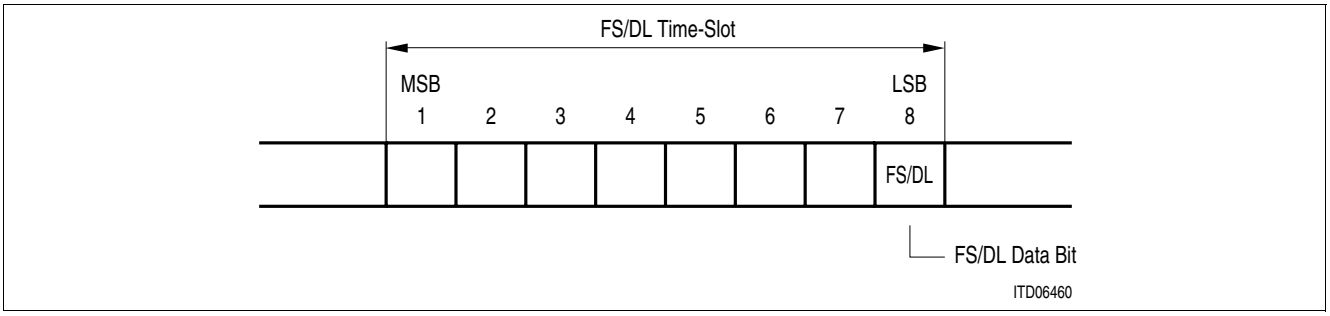


Figure 88 Transmit FS/DL Bits on XDI (T1/J1)

5.6.3.1 Transmit Offset Programming (T1/J1)

This chapter describes the system highway operation in 1.544 MHz mode only. If the system highway is operated in 2.048 MHz mode, the description given in **Chapter 4.6.3.1** applies.

$\overline{\text{SYPX}}$ Offset Calculation

T: Time between the active edge of SCLKX after $\overline{\text{SYPX}}$ pulse begin and beginning of the next frame (F-bit, channel phase 0), measured in number of SCLKX clock intervals; maximum delay: T_{max} = (200 x SC/BF) - (7 ¥ SC/BF) - 1

BF: Basic frequency; 1.544 Mbit/s

SC: System clock rate; 1.544, 3.088, 6.176, or 12.352 MHz

X: Programming value to be written to registers RC0 and RC1 (see Page 356).

$0 \leq T \leq 4$: 3 - T + (7 ° SC/BF)

$5 \leq T \leq T_{max}$: X = (200 ° SC/BF) - T + 3

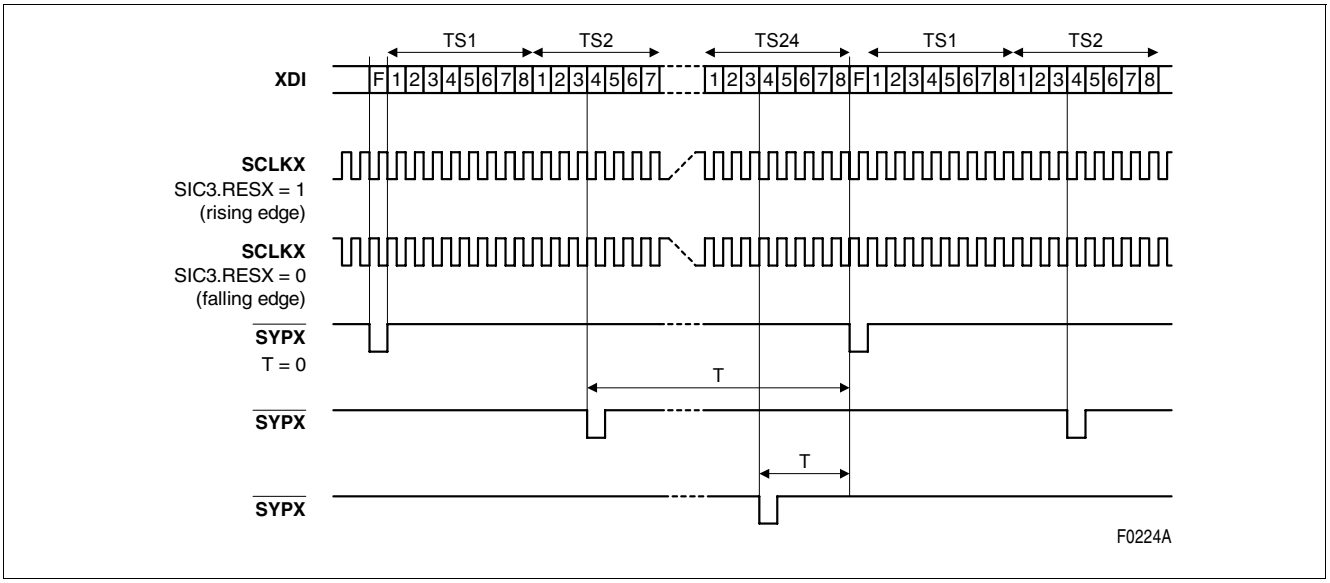


Figure 89 $\overline{\text{SYPX}}$ Offset Programming (1.544 Mbit/s, 1.544 MHz)

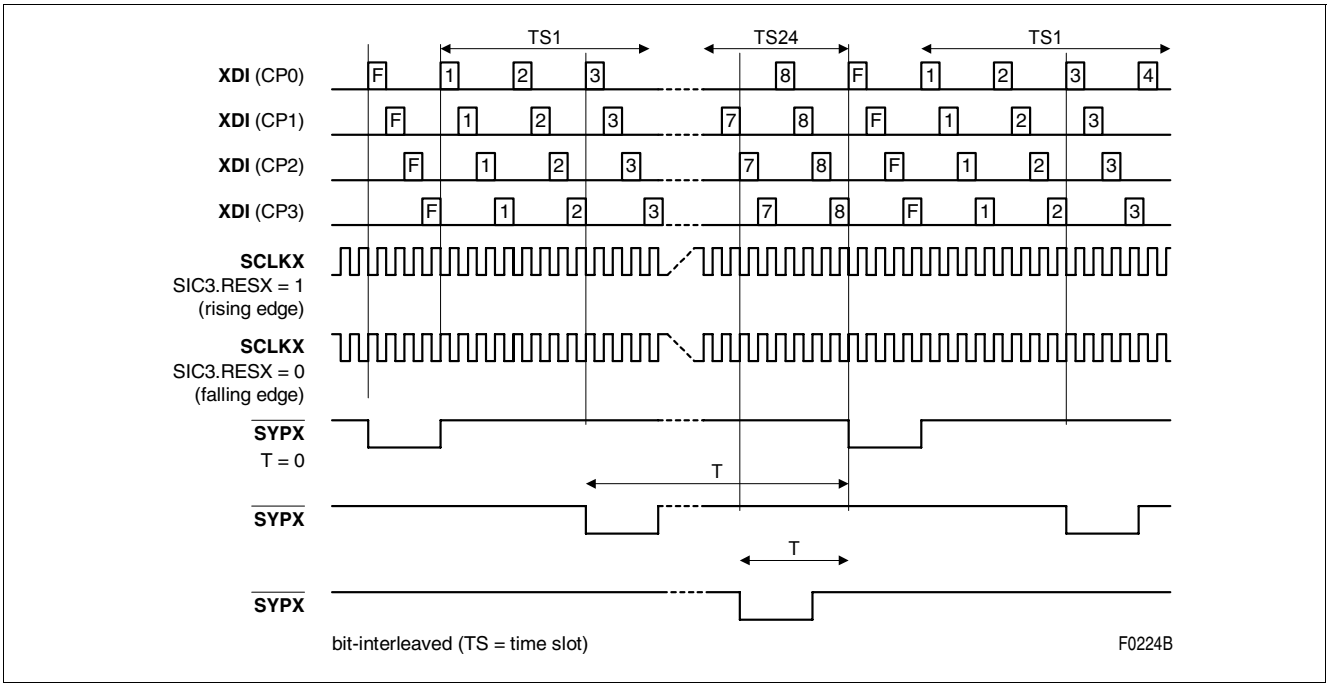


Figure 90 $\overline{\text{SYPX}}$ Offset Programming (6.176 Mbit/s, 6.176 MHz)

5.6.4 Time Slot Assigner (T1/J1)

HDLC channel 1 offers the flexibility to connect data during certain time slots, as defined by registers RTR(4:1) and TTR(4:1) (**RTR1_T**, **TTR1_T**), to the RFIFO and XFIFO, respectively. Any combinations of time slots can be programmed for the receive and transmit directions. If CCR1.EITS = 1 the selected time slots (RTR(4:1)) are stored in the RFIFO of the signaling controller and the XFIFO contents is inserted into the transmit path as controlled by registers TTR(4:1).

For HDLC channels 2 and 3, one out of 24 time slots can be selected for each channel, but in common for transmit and receive direction.

Within selected time slots single bit positions can be masked to be used/not used for HDLC transmission for all HDLC channels. Additionally, the use of even, odd or both frames can be selected for each HDLC channel individually.

Table 59 Time Slot Assigner HDLC Channel 1 (T1/J1)

Receive Time Slot Register	Transmit Time Slot Register	Time Slots	Receive Time Slot Register	Transmit Time Slot Register	Time Slots
RTR 1.7	TTR 1.7	0	RTR 3.7	TTR 3.7	16
RTR 1.6	TTR 1.6	1	RTR 3.6	TTR 3.6	17
RTR 1.5	TTR 1.5	2	RTR 3.5	TTR 3.5	18
RTR 1.4	TTR 1.4	3	RTR 3.4	TTR 3.4	19
RTR 1.3	TTR 1.3	4	RTR 3.3	TTR 3.3	20
RTR 1.2	TTR 1.2	5	RTR 3.2	TTR 3.2	21
RTR 1.1	TTR 1.1	6	RTR 3.1	TTR 3.1	22
RTR 1.0	TTR 1.0	7	RTR 3.0	TTR 3.0	23
RTR 2.7	TTR 2.7	8	RTR 4.7	TTR 4.7	24
RTR 2.6	TTR 2.6	9	RTR 4.6	TTR 4.6	25
RTR 2.5	TTR 2.5	10	RTR 4.5	TTR 4.5	26

Table 59 Time Slot Assigner HDLC Channel 1 (T1/J1) (cont'd)

Receive Time Slot Register	Transmit Time Slot Register	Time Slots	Receive Time Slot Register	Transmit Time Slot Register	Time Slots
RTR 2.4	TTR 2.4	11	RTR 4.4	TTR 4.4	27
RTR 2.3	TTR 2.3	12	RTR 4.3	TTR 4.3	28
RTR 2.2	TTR 2.2	13	RTR 4.2	TTR 4.2	29
RTR 2.1	TTR 2.1	14	RTR 4.1	TTR 4.1	30
RTR 2.0	TTR 2.0	15	RTR 4.0	TTR 4.0	31

The format for receive FS/DL data transmission in time slot 0 of the system interface is as shown in **Figure 82** below. In order to get an undisturbed reception even in the asynchronous state bit FMR2.DAIS has to be set.

5.7 Test Functions (T1/J1)

The following chapters describe the test functions which are supported by the OctalFALC™.

5.7.1 Pseudo-Random Binary Sequence Generation and Monitor (T1/J1)

The OctalFALC™ has the ability to generate and monitor pseudo-random binary sequences (PRBS). The generated PRBS pattern is transmitted to the remote end on pins XL1/2 or XDOP/N and can be inverted optionally. Generation and monitoring of PRBS pattern is done according to ITU-T O.150 and ITU-T O.151.

The PRBS monitor monitores the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non-inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter (CEC2). Synchronization is reached within 400 ms with a probability of 99.9% at a bit error rate of up to 10^{-1}.

Different PRBS modes which are using different bits and time slots in a T1/J1 frame can be selected, see **Table 61**.

In the "unframed" mode all bits of all slots in a T1/J1 frame are used for PRBS.

In the "framed" mode the frame bit (time slot 0) in a T1/J1 frame is not used for PRBS respectively.

Selection of the PRBS modes "unframed" and "framed" is done by TPC0.PRM = ´00_b´ and TPC0.FRA (**TPC0_T**).

For TPC0.PRM not ´00_b´, each time slot of an T1/J1 frame can be selected individually to send and receive a PRBS signal. Selection is done by the registers PRBSTS1 to PRBSTS4. Here the used time slot numbers are the same as used normally for numbering of the time slots: In T1/J1 frames time slot number 0 (TS0) indicates the frame bit and the time slot numbers 1 to 24 indicates the payload TS1 to TS24.

If a time slot is used or not for PRBS transmission and reception is controlled by the registers PRBSTS(1:4) (**PRBSTS1_T**). The number of used time slots for PRBS is refered to as "N" and is related to the line side. The range of N is 1, ..., 25 for T1/J1 because of the frame bit (N == 1). The time slot selection 0 up to 24 for T1/J1 by PBBSTS(1:4) is common for all eight ports respectively.

The PRBS time slot selection is independent of the configuration of the system interface, especially independent of the kind of selected channel translation mode (0 or 1): The time slot numbering for selection of PRBS is the same as used for the payload data (0, ..., 24), see numbers in the columns "Channels (received time slots)" in **Table 43**. TS0 for PRBS selection corresponds to the FS/DL channel. For example PRBS selection of TS16 (PRBSTS3.TS16) is related to time slot 21 at system interface in channel translation mode 0.

The N multiple time slots are selected arbitrarily for PRBS. The PRBS data stream has to be written into or read from the time slots consecutive respectively.

Note that PRBS deselection of time slot 0 (frame bit) by PRBSTS1.TS0 = ´0´ performes a "framed" mode.

For TPC0.PRM unequal ´00b´, normally all eight bits of the time slots are used for PRBS ("N × 64 kbit/s") with exception of the time slot 0, which includes only the frame bit. To allow CAS-BR in T1/J1 mode, only 7 MSBs of the all time slots which are selected for PRBS can be optionally used for PRBS to avoid CAS disturbance ("N × 56 kbit/s"), the eight´s bit of all time slots (which is the CAS bit in T1) is not used for PRBS. Setting of this mode is performed by setting the register bits TPC0.PRM(1:0) to´11b´.

Note that in the “N × 56 kbit/s” mode the frame bit (defined here as the time slot 0) will not be used for PRBS, even if it is selected by setting PRBSTS1.TS0. (In “N × 56 kbit/s” mode PRBSTS1.TS0 is not valid.)

Note that the “N × 56 kbit/s” mode is automatically a “framed” mode in T1/J1 because the time slot 0 is identical to the frame bit.

Note that in “N × 64 kbit/s” mode and enabling of all time slots by PRBSTS(1:4) all bits in the frame are used for PRBS (that is an “unframed” mode).

The kind of PRBS patterns (polynomials) can be selected to be 2^{11}-1, 2^{15}-1, 2^{20}-1or 2^{23}-1 by the register bits TPC0.PRP(1:0) and LCR1.LLBP, see **Table 60**. For definition of this polynomials see the Standards ITU-T O.150, O.151. and TR62441. The polynomials 2^{11}-1 and 2^{23}-1 can be selected only if TPC0.PRM not ´00b´.

Transmission of PRBS pattern is enabled by register bit LCR1.XPRBS (**LCR1_T**). With the register bit LCR1.FLLB switching between not inverted and inverted transmit pattern can be done.

The receive monitoring of PRBS patterns is enabled by register bit LCR1.EPRM. In general, depending on bit LCR1.EPRM the source of the interrupt status bit ISR1.LLBSC changed, see register description. The type of detected PRBS pattern in the receiver is shown in the status register bits PRBSSTA.PRS. Every change of the bits PRS in PRBSSTA sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected if signal “alarm simulation” is active.

The detection of all_zero or all_ones is done over 12, 16, 21 or 24 consecutive bits, depending on the selected PRBS polynomial (2^{11}-1, 2^{15}-1, 2^{20}-1or 2^{23}-1 respectively). The detection of all_zero or all_ones is independent on LCR1.FLLB.

The distinction between all-ones and all-zeros pattern is possible by combination of

- The information about the first reached PRBS status after the PRBS monitor was enabled (“PRBS pattern detected” or “inverted PRBS pattern detected”) with
- The status information “all-zero pattern detected” or “all-ones pattern detected”

Because every bit error in the PRBS sequence increments the bit error counter BEC, no special status information like “PRBS detected with errors” is given here.

The time slot selection is related to the mapping used on the system interface.

Table 60 Supported PRBS Polynomials

TPC0.PRP(1:0)	TPC0.PRM	LCR1.LLBP	Kind of Polynomial	Comment
00	01 or 11	X	2^{11} -1	
01	01 or 11	X	2^{15} -1	
10	01 or 11	X	2^{20} -1	
11	01 or 11	X	2^{23} -1	
XX	00	0	2^{15} -1	SW compatible to QuadFALC®
XX	00	1	2^{20} -1	

Table 61 Bit/Time Slot Selection of PRBS Pattern

TPC0.PRM	TPC0.FRA	Kind of Selection	Comment
00	0	Unframed	Settings in PRBSTS are not valid; SW compatible to QuadFALC®
00	1	Framed	
01	X	N x 64 kbit/s	“framed” mode if TS0 is deselected; CAS in E1 is not disturbed if time slot16 is deselected
10	X	Reserved	
11	X	N x 56 kbit/s	Implies a “framed” mode

5.7.2 Remote Loop (T1/J1)

In the remote loop-back mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON through the analog or digital transmitter, see **Figure 57** and **Figure 31**. As in normal mode they are also processed by the synchronizer and then sent to the system interface. The remote loop-back mode is activated by

- The control bit LIM1.RL or
- After detection of the appropriate In-band loop code, if enabled by ALS.LILS and if LIM0.LL = ´0´ (to avoid deadlocks), see **Chapter 5.5.7** or
- After detection of the appropriate Out-band loop code, if enabled by ALS.LOLS and if LIM0.LL = ´0´ (to avoid deadlocks), see **Chapter 5.5.8**.

Received data can be looped with or without the jitter attenuator (JATT Buffer) dependent on LIM1.JATT.

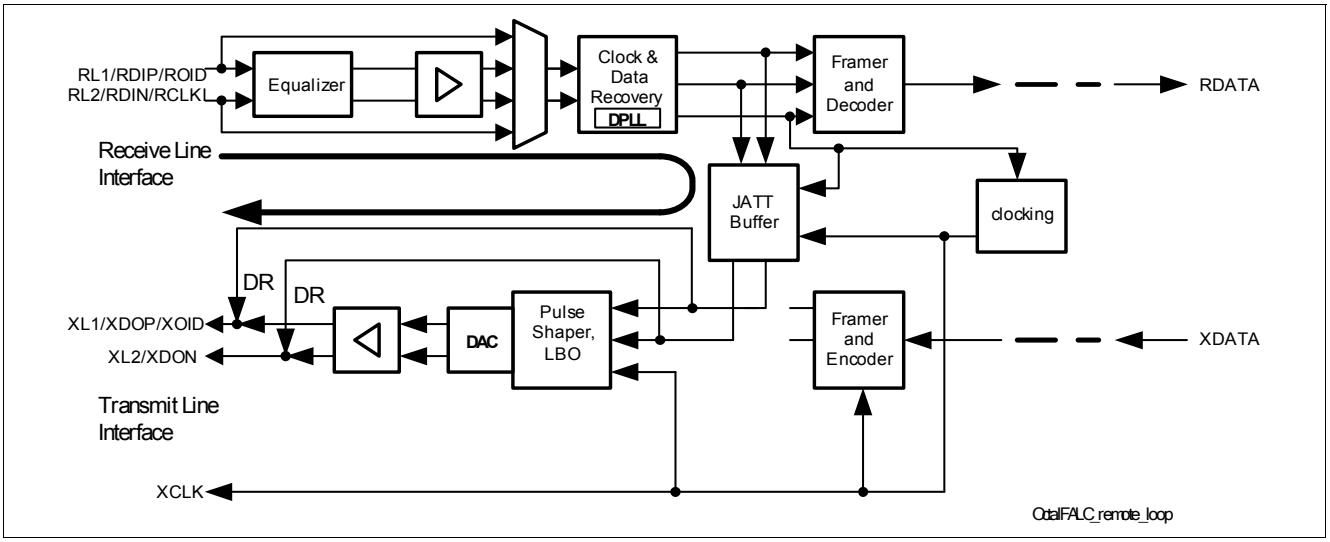


Figure 91 Remote Loop (T1/J1)

DR means digital interface with dual rail mode.

5.7.3 Payload Loop-Back (T1/J1)

To perform an effective circuit test a payload loop is implemented.

The payload loop-back is activated by

- The control bit FMR2.PLB (**FMR2_T**) or
- After detection of the appropriate Out-band loop code, if enabled by ALS.SOLS and if LIM0.LL = ´0´ (to avoid deadlocks), see **Chapter 5.5.8**.

During activation of the payload loop, the received 192 bits of payload data are looped back to the transmit direction. The framing bits, CRC6 and DL-bits are not looped, if FMR4.TM = ´0´. They are originated by the OctalFALC™ transmitter. If FMR4.TM = ´1´ the received FS/DL-bit is sent transparently back to the line interface. Following pins are ignored: XDI, XSIG, TCLK, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally. With bit FMR2.SAIS an AIS can be sent to the system interface on pin RDO.

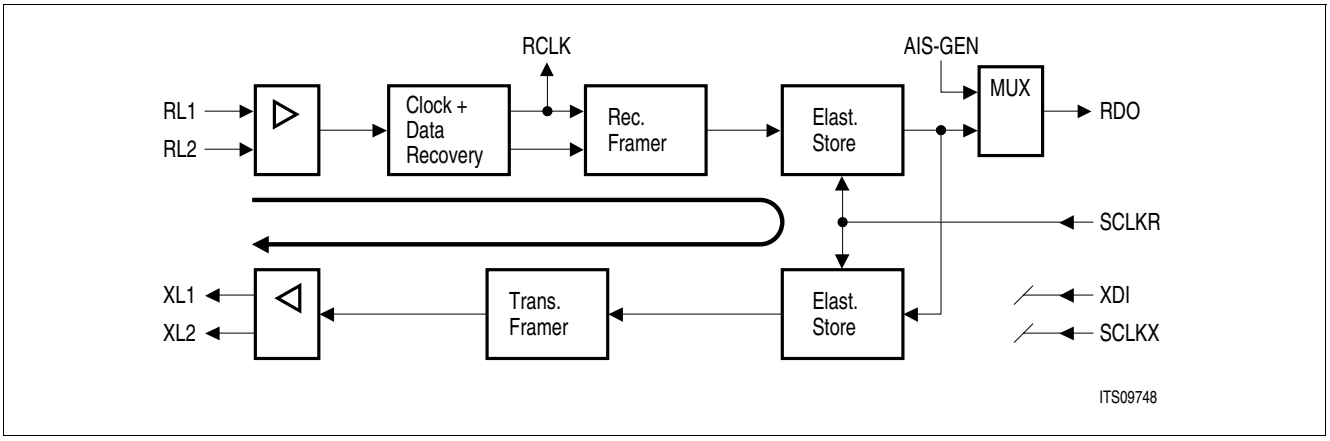


Figure 92 Payload Loop (T1/J1)

5.7.4 Local Loop (T1/J1)

The local loop-back is activated by

- The control bit LIM0.LL (**LIM0_T**) or
- After detection of the appropriate In-band loop code, if enabled by ALS.SILS, see **Chapter 5.5.7**.

The local loop-back mode disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. However, the bit stream is transmitted undisturbed on the line. An AIS to the distant end can be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop usually invokes an out of frame error until the receiver resynchronizes to the new framing. The serial codes for transmitter and receiver have to be identical.

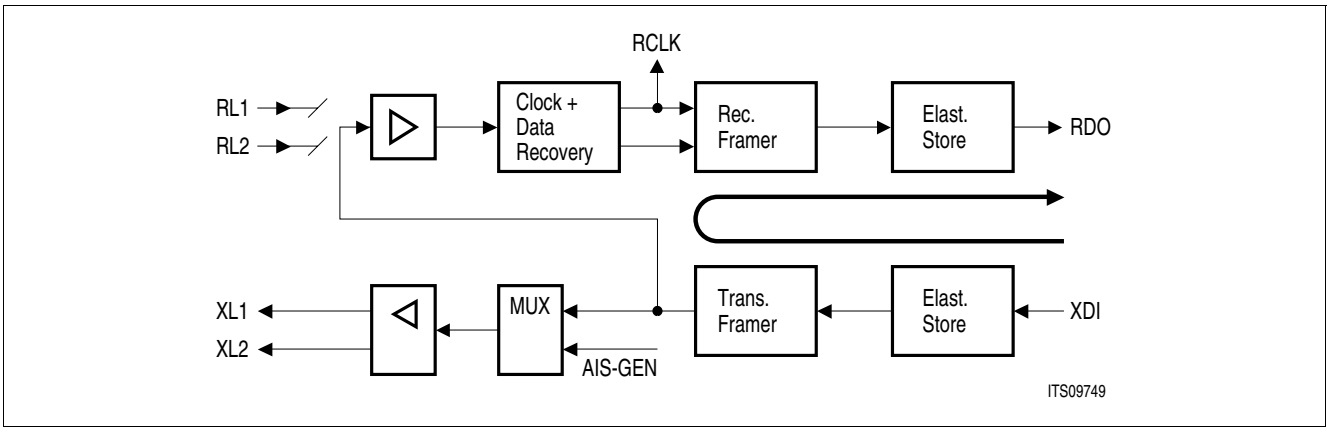


Figure 93 Local Loop (T1/J1)

5.7.5 Single Channel Loop-Back (loop-back of time slots) (T1/J1)

The channel loop-back is selected by LOOP.ECLB = ´1´ (**LOOP_T**).

Each of the 24 time slots can be selected for loop-back from the system PCM input (XDI) to the system PCM output (RDO). This loop-back is programmed for one time slot at a time selected by register LOOP. During loop-back, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time slot.

For the time slot test, sending sequences of test patterns like a 1 kHz check signal should be avoided. Otherwise an increased occurrence of slips in the tested time slot disturbs testing. These slips do not influence the other time slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

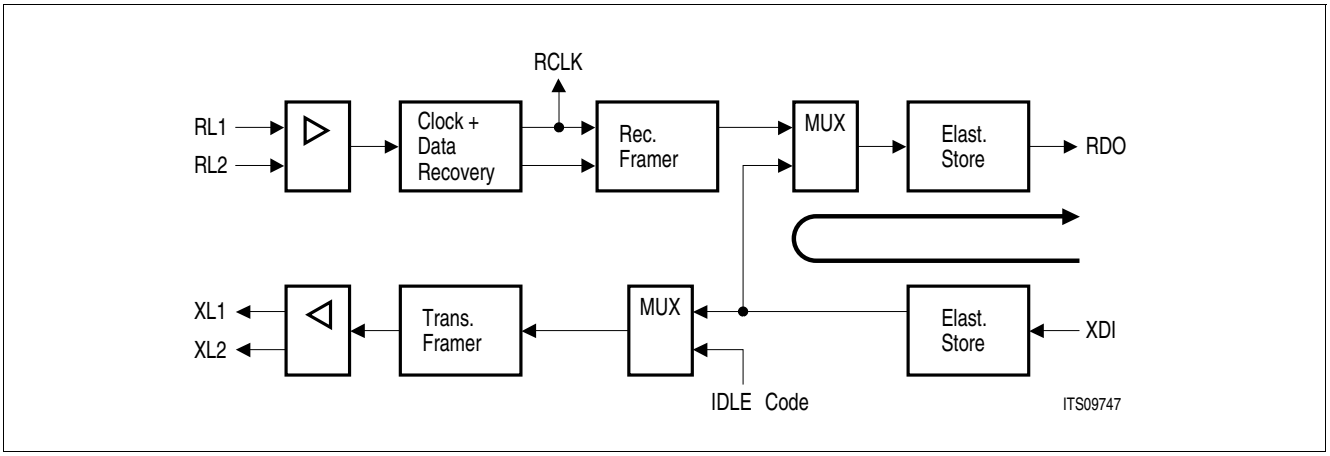


Figure 94 Channel Loop-Back (T1/J1)

5.7.6 Alarm Simulation (T1/J1)

Alarm simulation does not affect the normal operation of the device, i.e. all time slots remain available for transmission. However, possible *real* alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss-Of-Signal (LOS, red alarm)
- Alarm indication signal (AIS, blue alarm)
- Loss of pulse frame
- Remote alarm (yellow alarm) indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter
- CRC6 error counter

Some of the above indications are only simulated if the OctalFALC™ is configured in a mode where the alarm is applicable.

The alarm simulation is controlled by the value of the alarm simulation counter: FRS2.ESC which is incremented by setting bit FMR0.SIM.

Clearing of alarm indications:

- Automatically for LOS, remote (yellow) alarm, AIS, and loss of synchronization and
- User controlled for slips by reading the corresponding interrupt status register ISR3.
- Error counter have to be cleared by reading the corresponding counter registers.

Is only possible at defined counter steps of FRS2.ESC. For complete simulation (FRS2.ESC = ´0´), eight simulation steps are necessary.

5.7.7 Single Bit Defect Insertion (T1/J1)

Single bit defects can be inserted into the transmit data stream for the following functions:

FAS defect, multiframe defect, CRC defect, CAS defect, PRBS defect and bipolar violation.

Defect insertion is controlled by register IERR.

5.8 J1-Feature Overview

The Japanese J1 standard is very similar to the T1 standard, but differs in some details. To support these differences easily, the following features are provided within the OctalFALC™:

- CRC6 generation and checking according to ITU-JT G.706 (CRC checksum calculation includes FS/DL-bits, see **Chapter 5.4.6.3**)

- Remote alarm handling according to ITU-JT G.704 (remote alarm pattern in DL-channel is "1111111111111111", see **Chapter 5.4.6.2**
- NTT synchronization requirements in ESF framing mode
- Pulse shaping according to JT G.704
- Receive input thresholds according to ITU-JT G.703

J1 mode is globally selected by setting RC0.SJR = ´1´. For specific J1 framer initialization see Table 55 on page 200.

No special pulse mask setting is required, the described T1-settings also fulfill the J1 requirements.

6 Register Description

Due to the different device function is E1 and T1/J1 mode, several registers and register bits have dedicated functions according to the selected operation mode.

To maintain easy readability this chapter is divided into separate E1 and T1/J1 sections. Please choose the correct description according to your application (E1 or T1/J1).

Further this chapters are divided into separate control register and status register sections. The transmit parts of the FIFOs of the three HDLC channels are included in the control register part (XFIFO(1:3)), whereas the receive part are included in the status register part (RFIFO(1:3)), see for example **XFIFO1L_T** and **RFIFO1L_T** for the lower bytes and for T1/J1 mode.

After reset any new functions against the QuadFALC® V2.1 are not valid. Any new function to be used must be enabled explicitly.

If COMP = ´1´, the behavior is the same as for QuadFALC® V2.1. and full software compatibility is realized. The higher address part of all global registers is ´00_H´, that of the port (channel) specific ones include the channel number 0 to 7 and is marked in the following tables with ´xx_H´. So ´xx_H´ has the values ´00_H´ up to ´07_H´.

In compatibility mode (COMP = ´1´) every global register exists one times in both of the pseudo QuadFALC®s with exception of the status register DSTR and the register GLC1, which exist only one time in the whole device. But the content of the bit QFN.DSTR for COMP = ´1´ reflects the number of the pseudo QuadFALC® (0 or 1).

Global registers require specific handling, dependent on the compatibility mode selection. An overview of the global registers is given in **Table 63**. Especially for registers CIS and GIS see **Figure 95**, for registers VSTR and DSTR see **Figure 96**.

In compatibility mode (COMP = ´1´) the registers regarding the central clock PLL, GCM(1:8), exists one time in both of the pseudo QuadFALC®s, but the registers of the pseudo QuadFALC®2 are “dummys”: Writing and reading is possible but their values are not taken into account for any configuration of the PLL and writing on register GCM5 or GCM6 causes NO reset of the PLL. Only the registers GCM(1:8) of the pseudo QuadFALC®1 are taken into account for configuration of the PLL and write operations to register GCM5 or GCM6 causes a reset of the PLL as in QuadFALC® or FALC56®v2.1.

In compatibility mode (COMP = ´1´) the status registers regarding the central clock PLL, GIS2 and GIMR, exists one time in both of the pseudo QuadFALC®s: The status of the one PLL is mirrored and can be masked individually in every of the both pseudo QuadFALC®s

In generic mode (COMP = ´0´) the registers GIMR, GIS2 and GCM(1:8) exist only one times in the whole device.

If compatibility mode is selected, the version status register VSTR shows the same value as in QuadFALC® V2.1 while the JTAG boundary scan ID is always the OctalFALC number and not affected by the compatibility mode selection.

The usage of register bits for configuration of the clock system (see **Chapter 3.6** and **Chapter 3.7**) which depends on COMP is shown in **Table 62**.

Table 62 Register Usage Depending on COMP

Functionality	Used register bits for COMP = ´1´ (in both of the pseudo QuadFALC®s)	Used register bits for COMP = ´0´
RCLK source selection	GPC1.R1S	---
	---	GPC(2:6).R(1:8)S
SEC/FSC source selection	GPC1.FSS	---
	---	GPC2.FSS
Transmit clock selection	CMR1.STF	---
	---	CMR5.STF

Table 62 Register Usage Depending on COMP (cont'd)

Functionality	Used register bits for COMP = ´1´ (in both of the pseudo QuadFALC®s)	Used register bits for COMP = ´0´
Receive reference clock selection	CMR1.DRSS	---
	---	CMR5.DRSS
Receive clock frequency selection	CMR1.RS	---
	---	CMR4.RS

Table 63 Overview of Global Registers

Register name	Functions for COMP = ´1´		Functions for COMP = ´0´	Comments
	Pseudo QuadFALC 1	Pseudo QuadFALC 2		
CIS	PLLLS, GIS(4:1)	PLLLS, GIS(4:1)	GIS(8:1)	For COMP = ´0´ value of bit PLLLS of both pseudo QuadFALC®s is identical
GPC(2:6)	Dummy register	Dummy register	FSS(2:0), R(1:8)S(2:0)	Dummy register: W/R possible but no influence on configuring
IPC	IC(1:0) defines INT1	IC(1:0) define INT2	IN(1:0) defines INT	For COMP = ´1´the bits SSYF of both pseudo QuadFALC®s are logically ored
VSTR	´0000101´	´00000101´	´00100000´	x
GIS	ISR(7:0)	ISR(7:0)	ISR(7:0)	x
GPC1	SMM, FSS(1:0), R1S(1:0)	SMM, FSS(1:0), R1S(1:0)	SMM; FSS(1:0) and R1S(1:0) not used	SMM bits exists two times also for COMP = ´0´ and define together the system multiplex mode
GCM(1:8)	Configures the master clock unit	Dummy registers	Configures the master clock unit	Dummy registers: W/R possible but no influence on configuring
GIMR	PLIL, PLLL	PLIL, PLLL	PLIL, PLLL	For COMP = ´1´ masking of the doubled IS bits can be done individually in both pseudo QuadFALC®s
GIS2	PLLLS, PLLLC	PLLLS, PLLLC	PLLLS, PLLLC	For COMP = ´1´ the IS bits of the one PLL are doubled for both pseudo QuadFALC®s
GLC1	RAMRW, RAMEN	Don't exist here	RAMRW, RAMEN	
INBLDTR	INBLDR(1:0), INBLDT(1:0)	Dummy register	INBLDR(1:0), INBLDT(1:0)	Dummy register: W/R possible but no influence on configuring

Table 63 Overview of Global Registers (cont'd)

Register name	Functions for COMP = ´1´		Functions for COMP = ´0´	Comments
DSTR	QFN=´0´, COMP = ´1´	QFN=´1´, COMP = ´1´	QFN=´0´, COMP = ´0´	
PRBSTS(1:4)	TS(32:1)	Dummy registers	TS(32:1)	Dummy registers: W/R possible but no influence on configuring

Note: "RES" in the register descriptions means reserved, not reset. If these bits are written the value must be ´0´ for proper operation.

Note: In all bit fields used in the register schematics and also in the table desrciptions the most significant bit is the left one and the least significant bit is the right one. Sometimes in the text a bit field with the name "bitfieldname" is denoted as <bitfieldname>(MSB:LSB). For example: In register MODE_E the bit fiield MDS constists on MDS(1:0).

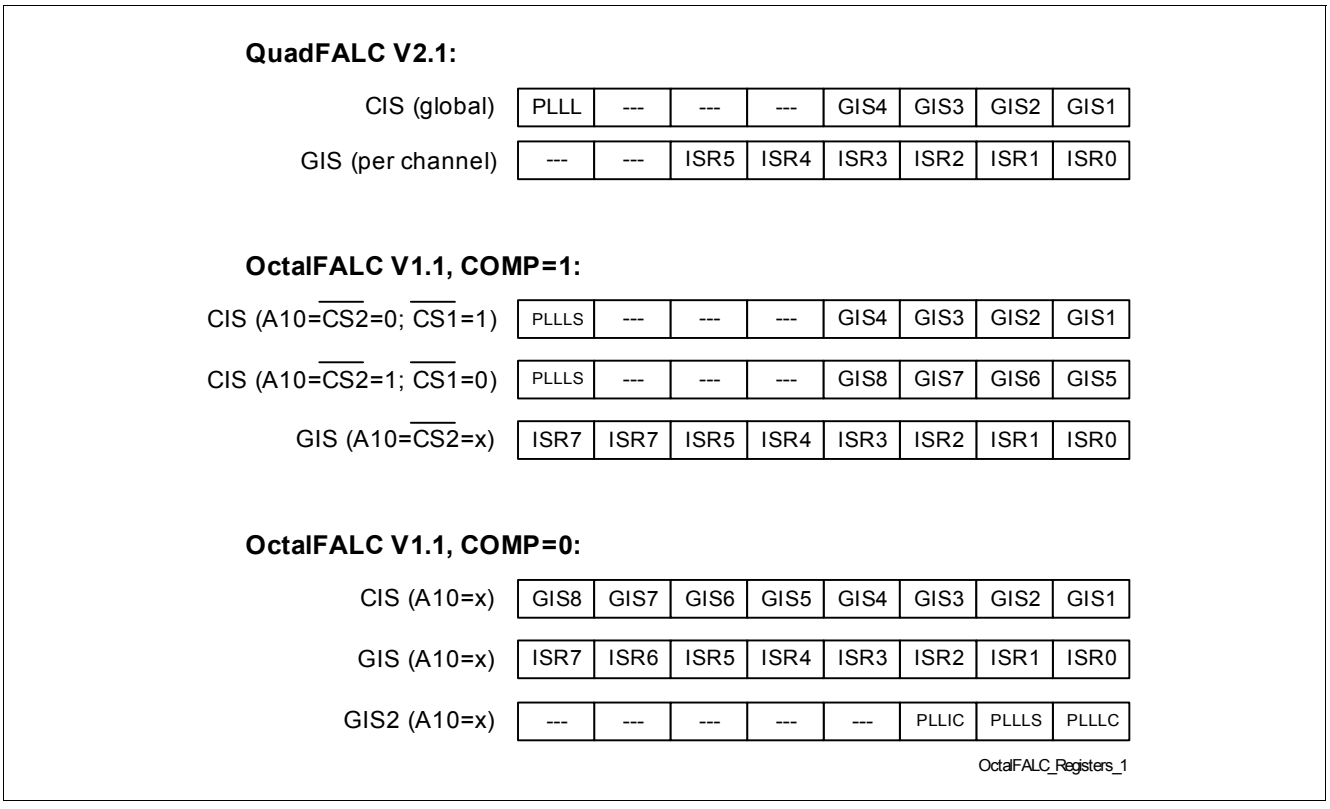


Figure 95 Register Compatibility for CIS and GIS

QuadFALC V2.1:

VSTR	0	0	0	0	0	1	0	1

OctalFALC V1.1, COMP=1:

VSTR (A10=$\overline{CS2}$=0; $\overline{CS1}$=1)	0	0	0	0	0	1	0	1
DSTR (A10=$\overline{CS2}$=0; $\overline{CS1}$=1)	0	0	0	0	0	0	0	1
VSTR (A10=$\overline{CS2}$=1; $\overline{CS1}$=0)	0	0	0	0	0	1	0	1
DSTR (A10=$\overline{CS2}$=1; $\overline{CS1}$=0)	0	0	0	0	0	0	1	1

OctalFALC V1.1, COMP=0:

VSTR (A10=x)	0	0	1	0	0	0	0	0
DSTR (A10=x)	0	0	0	0	0	0	0	0

OctalFALC_Registers_2

Figure 96 Register Compatibility for VSTR

7 E1 Registers

After reset all control registers except the XFIFO and XS(16:1) are initialized to defined values. Unused bits have to be cleared (logical "0").

Table 64 Registers Address Space

Module	Base Address	End Address	Note
E1 Registers	$xx00_H$	$_H$	xx = is the channel no. (0 to 7)

Table 65 Registers Overview E1

Register Short Name	Register Long Name	Offset Address	Page Number
XFIFO1L_E	Transmit FIFO - HDLC Channel 1 - Lower Byte	$xx00_H$	218
XFIFO1H_E	Transmit FIFO - HDLC Channel 1 - Higher Byte	$xx01_H$	219
CMDR_E	Command Register	$xx02_H$	220
MODE_E	Mode Register	$xx03_H$	222
RAH1_E	Receive Address Byte High Register 1	$xx04_H$	223
RAH2_E	Receive Address Byte High Register 2	$xx05_H$	224
RAL1_E	Receive Address Byte Low Register 1	$xx06_H$	225
RAL2_E	Receive Address Byte Low Register 2	$xx07_H$	226
CCR1_E	Common Configuration Register 1	$xx09_H$	228
CCR2_E	Common Configuration Register 2	$xx0A_H$	231
RDICR_E	RDI Clear Condition Register	$xx0B_H$	232
RTR1_E	Receive Time Slot Register 1	$xx0C_H$	233
TTR1_E	Transmit Time Slot Register 1	$xx10_H$	234
IMR0_E	Interrupt Mask Register 0	$xx14_H$	236
IERR_E	Single Bit Defect Insertion Register	$xx1B_H$	238
FMR0_E	Framer Mode Register 0	$xx1C_H$	239
FMR1_E	Framer Mode Register 1	$xx1D_H$	241
FMR2_E	Framer Mode Register 2	$xx1E_H$	243
LOOP_E	Channel Loop-Back	$xx1F_H$	245
XSW_E	Transmit Service Word Pulseframe	$xx20_H$	246
XSP_E	Transmit Spare Bits	$xx21_H$	247
XC0_E	Transmit Control 0	$xx22_H$	249
XC1_E	Transmit Control 1	$xx23_H$	250
RC0_E	Receive Control 0	$xx24_H$	251
RC1_E	Receive Control 1	$x25_H$	253
XPM0_E	Transmit Pulse Mask0	$xx26_H$	254
XPM1_E	Transmit Pulse Mask1	$xx27_H$	255
XPM2_E	Transmit Pulse Mask 2	$xx28_H$	256
TSWM_E	Transparent Service Word Mask	$xx29_H$	257
SIC4_E	System Interface Control Register 4	$xx2A_H$	258
IDLE_E	Idle Channel Code Register	$xx2B_H$	259
XSA4_E	Transmit Sa4 Register	$xx2C_H$	260
FMR3_E	Framer Mode Register 3	$xx31_H$	261

Table 65 Registers Overview E1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
ICB1_E	Idle Channel Register 1	xx32$_H$	263
LIM0_E	Line Interface Mode 0	xx36$_H$	264
LIM1_E	Line Interface Mode 1	xx37$_H$	266
PCD_E	Pulse Count Detection Register	xx38$_H$	268
PCR_E	Pulse Count Recovery	xx39$_H$	269
LIM2_E	Line Interface Mode 2	xx3A$_H$	270
LCR1_E	Loop Code Register 1	xx3B$_H$	271
LCR2_E	Loop Code Register 2	xx3C$_H$	273
SIC1_E	System Interface Control 1	xx3E$_H$	275
SIC2_E	System Interface Control 2	xx3F$_H$	277
SIC3_E	System Interface Control 3	xx40$_H$	279
CMR4_E	Clock Mode Register 4	xx41$_H$	281
CMR5_E	Clock Mode Register 5	xx42$_H$	282
CMR6_E	Clock Mode Register 6	xx43$_H$	283
CMR1_E	Clock Mode Register 1	xx44$_H$	285
CMR2_E	Clock Mode Register 2	xx45$_H$	287
ESM_E	Errored Second Mask	xx47$_H$	290
CMR3_E	Clock Mode Register 3	xx48$_H$	291
DEC_E	Disable Error Counter	xx60$_H$	292
XS1_E	Transmit CAS Register 1	xx70$_H$	293
XS2_E	Transmit CAS Register 2	xx71$_H$	294
PC1_E	Port Configuration 1	xx80$_H$	296
PC5_E	Port Configuration 5	xx84$_H$	300
PC6_E	Port Configuration 6	xx86$_H$	303
CMDR2_E	Command Register 2	xx87$_H$	304
CMDR3_E	Command Register 3	xx88$_H$	305
CMDR4_E	Command Register 4	xx89$_H$	306
CCR3_E	Common Configuration Register 3	xx8B$_H$	308
CCR4_E	Common Configuration Register 4	xx8C$_H$	310
CCR5_E	Common Configuration Register 5	xx8D$_H$	312
MODE2_E	Mode Register 2	xx8E$_H$	313
MODE3_E	Mode Register 3	xx8F$_H$	314
XFIFO2L_E	Transmit FIFO 2 Lower Byte	xx9C$_H$	325
XFIFO2H_E	Transmit FIFO 2 Higher Byte	xx9D$_H$	326
XFIFO3L_E	Transmit FIFO 3 Lower Byte	xx9E$_H$	327
XFIFO3H_E	Transmit FIFO 3 Higher Byte	xx9F$_H$	328
TSEO_E	Time Slot Even/Odd Select	xxA0$_H$	329
TSBS1_E	Time Slot Bit Select 1	xxA1$_H$	330
TSBS2_E	Time Slot Bit Select 2	xxA2$_H$	331
TSBS3_E	Time Slot Bit Select 3	xxA3$_H$	332
TSS2_E	Time Slot Select 2	xxA4$_H$	333

Table 65 Registers Overview E1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TSS3_E	Time Slot Select 3	xxA5$_H$	334
TPC0_E	Test Pattern Control Register 0	xxA8$_H$	336
TXP1_E	TX Pulse Template Register 1	xxC1$_H$	337
ALS_E	Automatic Loop Switching Register	xxD9$_H$	343
IMR7_E	Interrupt Mask Register 7	xxDF$_H$	349
RFIFO1L_E	Receive FIFO - HDLC Channel 1 - Lower Byte	xx00$_H$	350
RFIFO1H_E	Receive FIFO - HDLC Channel 1 - Higher Byte	xx01$_H$	351
RBD_E	Receive Buffer Delay	xx49$_H$	352
RES_E	Receive Equalizer Status	xx4B$_H$	354
FRS0_E	Framer Receive Status Register 0	xx4C$_H$	355
FRS1_E	Framer Receive Status Register 1	xx4D$_H$	357
RSW_E	Receive Service Word Pulseframe	xx4E$_H$	359
RSP_E	Receive Spare Bits/Additional Status	xx4F$_H$	360
FECL_E	Framing Error Counter Lower Byte	xx50$_H$	362
FECH_E	Framing Error Counter Higher Byte	xx51$_H$	363
CVCL_E	Code Violation Counter Lower Byte	xx52$_H$	364
CVCH_E	Code Violation Counter Higher Byte	xx53$_H$	365
CEC1L_E	CRC Error Counter 1 Lower Byte	xx54$_H$	366
CEC1H_E	CRC Error Counter 1 Higher Byte	xx55$_H$	367
EBCL_E	E-Bit Error Counter Lower Byte	xx56$_H$	368
EBCH_E	E-Bit Error Counter Higher Byte	xx57$_H$	369
CEC2L_E	CRC Error Counter 2 Lower Byte	xx58$_H$	370
CEC2H_E	CRC Error Counter 2 Higher Byte	xx59$_H$	371
CEC3L_E	CRC Error Counter 3 Lower Byte	xx5A$_H$	372
CEC3H_E	CRC Error Counter 3 Higher Byte	xx5B$_H$	373
RSA4_E	Receive Sa4-Bit Register	xx5C$_H$	374
RSA6S_E	Receive Sa6-Bit Status	xx61$_H$	375
RSP1_E	Receive Signaling Pointer 1	xx62$_H$	376
RSP2_E	Receive Signaling Pointer 2	xx63$_H$	377
SIS_E	Signaling Status Register	xx64$_H$	378
RSIS_E	Receive Signaling Status Register	xx65$_H$	379
RBCL_E	Receive Byte Count Low - HDLC Channel 1	xx66$_H$	381
ISR0_E	Interrupt Status Register 0	xx68$_H$	383
ISR1_E	Interrupt Status Register 1	xx69$_H$	385
ISR2_E	Interrupt Status Register 2	xx6A$_H$	387
ISR3_E	Interrupt Status Register 3	xx6B$_H$	389
ISR4_E	Interrupt Status Register 4	xx6C$_H$	391
ISR5_E	Interrupt Status Register 5	xx6D$_H$	393
GIS_E	Global Interrupt Status Register	xx6E$_H$	395
RS1_E	Receive CAS Register 1	xx70$_H$	398
RS2_E	Receive CAS Register 2	xx71$_H$	399

Table 65 Registers Overview E1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
RBC3_E	Receive Byte Count Register 3	xx91$_H$	402
SIS3_E	Signaling Status Register 3	xx9A$_H$	403
RSIS3_E	Receive Signaling Status Register 3	xx9B$_H$	404
RFIFO2L_E	Receive FIFO 2 Lower Byte	xx9C$_H$	406
RFIFO2H_E	Receive FIFO 2 Higher Byte	xx9D$_H$	407
RFIFO3L_E	Receive FIFO 3 Lower Byte	xx9E$_H$	408
RFIFO3H_E	Receive FIFO 3 Higher Byte	xx9F$_H$	409
SIS2_E	Signaling Status Register 2	xxA9$_H$	410
RSIS2_E	Receive Signaling Status Register 2	xxAA$_H$	411
MFPI_E	Multi Function Port Input Register	xxAB$_H$	413
ISR6_E	Interrupt Status Register 6	xxAC$_H$	414
ISR7_E	Interrupt Status Register 7	xxD8$_H$	416
PRBSSTA_E	PRBS Status Register	xxDA$_H$	417
CLKSTAT_E	Clock Status Register	xxFE$_H$	419
IPC_E	Interrupt Port Configuration	0008$_H$	227
RTR2	Receive Time Slot Register 2	0D$_H$	233
RTR3	Receive Time Slot Register 3	0E$_H$	233
RTR4	Receive Time Slot Register 4	0F$_H$	233
TTR2	Transmit Time Slot Register 2	11$_H$	234
TTR3	Transmit Time Slot Register 3	12$_H$	234
TTR4	Transmit Time Slot Register 4	13$_H$	234
IMR1	Interrupt Mask Register 1	15$_H$	236
IMR2	Interrupt Mask Register 2	16$_H$	236
IMR3	Interrupt Mask Register 3	17$_H$	236
IMR4	Interrupt Mask Register 4	18$_H$	236
IMR5	Interrupt Mask Register 5	19$_H$	236
IMR6	Interrupt Mask Register 6	1A$_H$	236
XSA5	Transmit Sa5 Register	2D$_H$	260
XSA6	Transmit Sa6 Register	2E$_H$	260
XSA7	Transmit Sa7 Register	2F$_H$	260
XSA8	Transmit Sa8 Register	30$_H$	260
ICB2	Idle Channel Register 2	33$_H$	263
ICB3	Idle Channel Register 3	34$_H$	263
ICB4	Idle Channel Register 4	35$_H$	263
LCR3_E	Loop Code Register 3	3D$_H$	274
GCR_E	Global Configuration Register	0046$_H$	289
VSTR_E	Version Status Register	004A$_H$	353
RSA5	Receive Sa5-Bit Register	5D$_H$	374
RSA6	Receive Sa6-Bit Register	5E$_H$	374
RSA7	Receive Sa7-Bit Register	5F$_H$	374
RSA8	Receive Sa8-Bit Register	60$_H$	374

Table 65 Registers Overview E1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
RBCH_E	Received Byte Count High - HDLC Channel 1	67_H	382
CIS_E	Channel Interrupt Status Register	$006F_H$	396
XS3	Transmit CAS Register 3	72_H	294
RS3	Receive CAS Register 3	72_H	399
XS4	Transmit CAS Register 4	73_H	294
RS4	Receive CAS Register 4	73_H	399
XS5	Transmit CAS Register 5	74_H	294
RS5	Receive CAS Register 5	74_H	399
XS6	Transmit CAS Register 6	75_H	294
RS6	Receive CAS Register 6	75_H	399
XS7	Transmit CAS Register 7	76_H	294
RS7	Receive CAS Register 7	76_H	399
XS8	Transmit CAS Register 8	77_H	294
RS8	Receive CAS Register 8	77_H	399
XS9	Transmit CAS Register 9	78_H	294
RS9	Receive CAS Register 9	78_H	399
XS10	Transmit CAS Register 10	79_H	294
RS10	Receive CAS Register 10	79_H	399
XS11	Transmit CAS Register 11	$7A_H$	294
RS11	Receive CAS Register 11	$7A_H$	399
XS12	Transmit CAS Register 12	$7B_H$	294
RS12	Receive CAS Register 12	$7B_H$	399
XS13	Transmit CAS Register 13	$7C_H$	294
RS13	Receive CAS Register 13	$7C_H$	399
XS14	Transmit CAS Register 14	$7D_H$	294
RS14	Receive CAS Register 14	$7D_H$	399
XS15	Transmit CAS Register 15	$7E_H$	294
RS15	Receive CAS Register 15	$7E_H$	399
XS16	Transmit CAS Register 16	$7F_H$	294
RS16	Receive CAS Register 16	$7F_H$	399
PC2	Port Configuration Register 2	81_H	298
PC3	Port Configuration Register 3	82_H	298
PC4	Port Configuration Register 4	83_H	298
GPC1_E	Global Port Configuration 1	0085_H	301
GPC2_E	Global Port Configuration Register 2	$008A_H$	307
RBC2_E	Receive Byte Count Register 2	90_H	401
GCM1_E	Global Clock Mode Register 1	0092_H	315
GCM2_E	Global Clock Mode Register 2	0093_H	316
GCM3_E	Global Clock Mode Register 3	0094_H	318
GCM4_E	Global Clock Mode Register 4	0095_H	319
GCM5_E	Global Clock Mode Register 5	0096_H	320

Table 65 Registers Overview E1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
GCM6_E	Global Clock Mode Register 6	0097_H	321
GCM7_E	Global Clock Mode Register 7	0098_H	323
GCM8_E	Global Clock Mode Register 7	0099_H	324
GIMR_E	Global Interrupt Mask Register	$00A7_H$	335
GIS2_E	Global Interrupt Status 2	$00AD_H$	415
TXP2	TX Pulse Template Register 2	$C2_H$	337
TXP3	TX Pulse Template Register 3	$C3_H$	337
TXP4	TX Pulse Template Register 4	$C4_H$	337
TXP5	TX Pulse Template Register 5	$C5_H$	337
TXP6	TX Pulse Template Register 6	$C6_H$	337
TXP7	TX Pulse Template Register 7	$C7_H$	337
TXP8	TX Pulse Template Register 8	$C8_H$	337
TXP9	TX Pulse Template Register 9	$C9_H$	337
TXP10	TX Pulse Template Register 10	CA_H	337
TXP11	TX Pulse Template Register 11	CB_H	337
TXP12	TX Pulse Template Register 12	CC_H	337
TXP13	TX Pulse Template Register 13	CD_H	337
TXP14	TX Pulse Template Register 14	CE_H	337
TXP15	TX Pulse Template Register 15	CF_H	337
TXP16	TX Pulse Template Register 16	$D0_H$	337
GPC3_E	Global Port Configuration Register 3	$00D3_H$	338
GPC4_E	Global Port Configuration Register 4	$00D4_H$	339
GPC5_E	Global Port Configuration Register 5	$00D5_H$	340
GPC6_E	Global Port Configuration Register 6	$00D6_H$	341
INBLDTR_E	In-Band Loop Detection Time Register	$00D7_H$	342
PRBSTS1_E	PRBS Time Slot Register 1	$00DB_H$	345
PRBSTS2_E	PRBS Time Slot Register 2	$00DC_H$	346
PRBSTS3_E	PRBS Time Slot Register 3	$00DD_H$	347
PRBSTS4_E	PRBS Time Slot Register 4	$00DE_H$	348
IMR7	Interrupt Mask Register 7	DF_H	236
DSTR_E	Device Status Register	$00E7_H$	418

The register is addressed wordwise.

Table 66 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
Basic Access Types			
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read/write virtual	rwv	Physically, there is no new register in the generated register file. The real readable and writable register resides in the attached hardware.	Register is read and writable by SW (same as rw type register)

Table 66 Registers Access Types (cont'd)

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior
read only	ro	Same as r type register	Same as r type register
read virtual	rv	Physically, there is no new register in the generated register file. The real readable register resides in the attached hardware.	Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior (same as r type register)
write	w	Register is written by software and affects hardware behavior with every write by software.	Register is writable by SW. When read, the register does not return the value that has been written previously, but some constant value instead.
write virtual	wv	Physically, there is no new register in the generated register file. The real writable register resides in the attached hardware.	Register is writable by SW (same as w type register)
read/write hardware affected	rwh	Register can be modified by hardware and software at the same time. A priority scheme decides, how the value changes with simultaneous writes by hardware and software.	Register can be modified by HW and SW, but the priority SW versus HW has to be specified. SW can read the register.

7.1 Detailed Description of E1 Control Registers

Transmit FIFO - HDLC Channel 1 - Lower Byte

Writing data to XFIFO of HDLC channel 1 can be done in 8-bit (byte) or - if the asynchronous micro controller interface is selected - in 16-bit (word) access. The LSB is transmitted first. 64 words of transmit data can be written to the XFIFO following a XPR interrupt, see Chapter 3.4.1.1.

XFIFO1L_E	Offset	Reset Value
Transmit FIFO - HDLC Channel 1 - Lower Byte	$xx00_H$	xx_H

7	6	5	4	3	2	1	0
XF7	XF6	XF5	XF4	XF3	XF2	XF1	XF0
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF7	7	w	**Transmit FIFO HDLC Channel 1, lower byte**
XF6	6	w	
XF5	5	w	
XF4	4	w	
XF3	3	w	
XF2	2	w	
XF1	1	w	
XF0	0	w	

Transmit FIFO - HDLC Channel 1 _ Higher Byte

Writing data to XFIFO of HDLC channel 1 can be done in 8-bit (byte) or - if the asynchronous micro controller interface is selected - in 16-bit (word) access. The LSB is transmitted first. Up to 64bytes/32 words of transmit data can be written to the XFIFO following a XPR interrupt, see Chapter 3.4.1.1.

XFIFO1H_E	Offset	Reset Value
Transmit FIFO - HDLC Channel 1 - Higher Byte	$xx01_H$	xx_H

7	6	5	4	3	2	1	0
XF15	XF14	XF13	XF12	XF11	XF10	XF9	XF8
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF15	7	w	**Transmit FIFO HDLC Channel 1, higher byte**
XF14	6	w	
XF13	5	w	
XF12	4	w	
XF11	3	w	
XF10	2	w	
XF9	1	w	
XF8	0	w	

Command Register

CMDR_E	Offset	Reset Value
Command Register	$xx02_H$	00_H

7	6	5	4	3	2	1	0
RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RMC	7	w	**Receive Message Complete - HDLC Channel 1** Confirmation from external micro controller to OctalFALCTM that the current frame or data block has been fetched following a RPF or RME interrupt, thus the occupied space in the RFIFO can be released. If RMC is given while RFIFO is already cleared, the next incoming data block is cleared instantly, although interrupts are generated.
RRES	6	w	**Receiver Reset** The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one-second timer and the receive signaling controller are reset. However the contents of the control registers is not deleted. A receiver reset should be made after switching from power down to power up (GCR.PD ´1´ -> ´0´).
XREP	5	w	**Transmission Repeat - HDLC Channel 1** If XREP is set together with XTF (write ´24_H´ to CMDR), the OctalFALCTM repeatedly transmits the contents of the XFIFO (1 up to 64 bytes) without HDLC framing fully transparently, i.e. without flag, CRC. If XREP is set together with XME (write ´22_H´ to CMDR), the OctalFALCTM repeatedly transmits the contents of the XFIFO (1 up to 64 bytes) including HDLC framing and calculated CRC. The cyclic transmission is stopped with a SRES command or by resetting XREP. *Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.*
XRES	4	w	**Transmitter Reset** The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper are reset. However the contents of the control registers is not deleted.
XHF	3	w	**Transmit HDLC Frame - HDLC Channel 1** After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.
XTF	2	w	**Transmit Transparent Frame - HDLC Channel 1** Initiates the transmission of a transparent frame without HDLC framing.

Field	Bits	Type	Description
XME	1	w	**Transmit Message End - HDLC Channel 1** Indicates that the data block written last to the transmit FIFO completes the current frame. The OctalFALC™ can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.
SRES	0	w	**Signaling Transmitter Reset - HDLC Channel 1** The transmitter of the signaling controller is reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to SRES a XPR interrupt is generated. This command can be used by the external micro controller to abort a frame currently in transmission. **Notes** *1. The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the external micro controller operates with a very high clock rate in comparison with the OctalFALC™'s clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.* *2. If SCLKX is used to clock the transmission path, commands to the HDLC transmitter should only be sent while this clock is available. If SCLKX is missing, the command register is blocked after an HDLC command is given.*

Mode Register

With this register the mode of the HDLC controller 1 is defined.

MODE_E	Offset	Reset Value
Mode Register	$xx03_H$	00_H

7	6	5	4	3	2	1	0
MDS			Res	HRAC	DIV	HDLCI	RFT2
rw				rw	rw	rw	rw

Field	Bits	Type	Description
MDS	7:5	rw	**Mode Select - HDLC Channel 1** The operating mode of the HDLC controller is selected. 000_B , Reserved 001_B , Signaling System 7 (SS7) support[1], see **Chapter 4.3.2** 010_B , One-byte address comparison mode (RAL1,2) 011_B , Two-byte address comparison mode (RAH1,2 and RAL1,2) 100_B , No address comparison 101_B , One-byte address comparison mode (RAH1,2) 110_B , Reserved 111_B , No HDLC framing mode
HRAC	3	rw	**Receiver Active - HDLC Channel 1** Switches the HDLC receiver to operational or inoperational state. 0_B , HDLC Receiver inactive 1_B , HDLC Receiver active
DIV	2	rw	**Data Inversion - HDLC Channel 1** Setting this bit inverts the internal generated HDLC channel 1 data stream. 0_B , Normal operation, HDLC data stream not inverted 1_B , HDLC data stream inverted
HDLCI	1	rw	**Inverse HDLC Operation Selection** Setting this bit switches the HDLC channel to the system side (”inverse” HDLC configuration). 0_B , HDLC protocol is sent and received on line side. 1_B , HDLC protocol is sent and received on system side.
RFT2	0	rw	**HDLC Receive FIFO Size Selection - HDLC channel 1** This bit selects the receive FIFO size of the HDLC channel 1, see **Table 10**. 0_B , HDLC receive FIFO is 32, 16, 4 or 2 byte deep, dependent on CCR1.RFT(1:0) *Note: Use this mode for software compatibility with QuadFALC®.* 1_B , HDLC receive FIFO is 64 byte deep to improve the HDLC performance) *Note: Use this mode to improve the HDLC performance. No dependency from CCR1.RFT(1:0).*

1) CCR2.RADD must be set, if SS7 mode is selected

Receive Address Byte High Register 1

In operating modes that provide high byte address recognition, the high byte of the received address is compared to the individually programmable values in RAH1 and RAH2. The address registers are used by all HDLC channels in common. Bit 1 (C/R-bit) is excluded from address comparison

RAH1_E	Offset	Reset Value
Receive Address Byte High Register 1	$xx04_H$	FD_H

7	6	5	4	3	2	1	0
RAH17	**RAH16**	**RAH15**	**RAH14**	**RAH13**	**RAH12**	**0**	**RAH10**
rw	rw	rw	rw	rw	rw	r	rw

Field	Bits	Type	Description
RAH17	7	rw	**Value of Second Individual High Address Bit** RAH17.
RAH16	6	rw	**Value of Second Individual High Address Bit** RAH16.
RAH15	5	rw	**Value of Second Individual High Address Bit** RAH15.
RAH14	4	rw	**Value of Second Individual High Address Bit** RAH14.
RAH13	3	rw	**Value of Second Individual High Address Bit** RAH13.
RAH12	2	rw	**Value of Second Individual High Address Bit** RAH12.
0	1	r	**Not valid** This bit (C/R bit) is excluded from address comparison.
RAH10	0	rw	**Value of Second Individual High Address Bit** RAH10.

Receive Address Byte High Register 2

RAH2_E	Offset	Reset Value
Receive Address Byte High Register 2	$xx05_H$	FF_H

7	6	5	4	3	2	1	0
RAH25	**RAH24**	**RAH23**	**RAH22**	**RAH21**	**RAH20**	**RAH19**	**RAH18**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RAH25	7	rw	**Value of Second Individual High Address Bit** RAH17.
RAH24	6	rw	**Value of Second Individual High Address Bit** RAH16.
RAH23	5	rw	**Value of Second Individual High Address Bit** RAH15.
RAH22	4	rw	**Value of Second Individual High Address Bit** RAH14.
RAH21	3	rw	**Value of Second Individual High Address Bit** RAH13.
RAH20	2	rw	**Value of Second Individual High Address Bit** RAH12.
RAH19	1	rw	**Value of Second Individual High Address Bit** RAH11.
RAH18	0	rw	**Value of Second Individual High Address Bit** RAH10.

Receive Address Byte Low Register 1

RAL1_E	Offset	Reset Value
Receive Address Byte Low Register 1	$xx06_H$	FF_H

7	6	5	4	3	2	1	0
RAL17	**RAL16**	**RAL15**	**RAL14**	**RAL13**	**RAL12**	**RAL11**	**RAL10**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RAL17	7	rw	**Value of First Individual Low Address Byte** RAL17
RAL16	6	rw	**Value of First Individual Low Address Bit** RAL16.
RAL15	5	rw	**ValLe of First Individual Low Address Bit** RAH15.
RAL14	4	rw	**Value of First Individual Low Address Bit** RAL14.
RAL13	3	rw	**Value of First Individual Low Address Bit** RAL13.
RAL12	2	rw	**Value of First Individual Low Address Bit** RAL12.
RAL11	1	rw	**Value of First Individual Low Address Bit** RAL11.
RAL10	0	rw	**Value of First Individual Low Address Bit** RAL10.

Receive Address Byte Low Register 2

RAL2_E	Offset	Reset Value
Receive Address Byte Low Register 2	$xx07_H$	FF_H

7	6	5	4	3	2	1	0
RAL25	**RAL24**	**RAL23**	**RAL22**	**RAL21**	**RAL20**	**RAL19**	**RAL18**
rw	rw	rw	rw	rw	rw	rw	rw

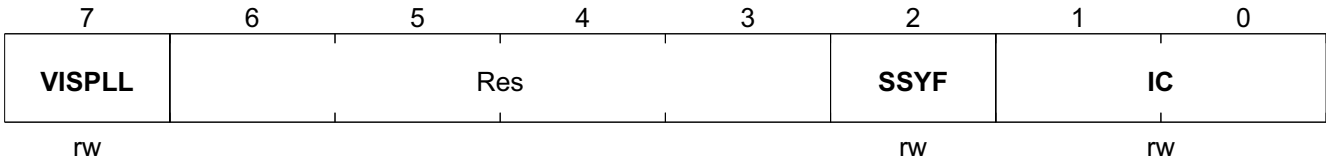
Field	Bits	Type	Description
RAL25	7	rw	**Value of Second Individual Low Address Bit** RAL25.
RAL24	6	rw	**Value of Second Individual Low Address Bit** RAL24.
RAL23	5	rw	**Value of Second Individual Low Address Bit** RAL23.
RAL22	4	rw	**Value of Second Individual Low Address Bit** RAL22.
RAL21	3	rw	**Value of Second Individual Low Address Bit** RAL21.
RAL20	2	rw	**Value of Second Individual Low Address Bit** RAL20.
RAL19	1	rw	**Value of Second Individual Low Address Bit** RAL19.
RAL18	0	rw	**Value of Second Individual Low Address Bit** RAL18.

Interrupt Port Configuration

See **Chapter 3.4.4** and **Table 16**.

Note: Unused bits have to be cleared.

IPC_E	Offset	Reset Value
Interrupt Port Configuration	**0008_H**	**00_H**



Field	Bits	Type	Description
VISPLL	7	rw	**Masked PLL Interrupts Visible** See also **Chapter 3.4.4** 0_B , Masked interrupt status bit PLLLC is not visible in register GIS2. 1_B , Masked interrupt status bit PLLLC is visible in GIS2.
SSYF	2	rw	**Select SYNC Frequency** Only applicable in master mode (LIM0.MAS = ´1´) and bit CMR2.DCF is cleared, see also **Table 16**. *Note: If COMP = ´1´ the bits SSYF of both pseudo QuadFALCs are logically ored.* 0_B , Reference clock on port SYNC is 2.048 MHz 1_B , Reference clock on port SYNC is 8 kHz
IC	1:0	rw	**Interrupt Port Configuration** These bits define the function of the interrupt output pins: If COMP = ´1´, pins INT1 and INT2 of the pseudoQuadFALC1 and pseudoQuadFALC2 respectively; if COMP = ´0´, pin INT is defined, see also **Chapter 3.4.4**. $X0_B$, Open drain output 01_B , Push/pull output, active low 11_B , Push/pull output, active high

Common Configuration Register 1

CCR1_E	Offset	Reset Value
Common Configuration Register 1	$xx09_H$	00_H

7	6	5	4	3	2	1	0
Res	XTS16RA	CASM	EITS	ITF	XMFA	RFT1	
	rw	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
XTS16RA	6	rw	**Send Remote Alarm in Time Slot 16** Sending of remote alarm in time slot 16 towards remote end by setting bit "Y" in the CAS multiframe alignment word. If XS registers are used for CAS (instead of XSIG), bit XS1.2 ("Y") is logically ored with XTS16RA. If XSIG is used for CAS, Y-data received on XSIG is logically ored with XTS16RA. 0_B , No remote alarm insertion 1_B , Remote alarm insertion
CASM	5	rw	**CAS Synchronization Mode** Determines the synchronization mode of the channel associated signaling multiframe alignment. 0_B , Synchronization is done in accordance to ITU-T G.732 1_B , Synchronization is established when two consecutively correct multiframe alignment pattern are found.
EITS	4	rw	**Enable Internal Time Slot 0 to 31 Signaling** 0_B , Internal signaling in time slots 0 to 31 defined by registers RTR(4:1) or TTR(4:1) is disabled. 1_B , Internal signaling in time slots 0 to 31 defined by registers RTR(4:1) or TTR(4:1) is enabled.
ITF	3	rw	**Interframe Time Fill** Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller. 0_B , Continuous logical "1" is output 1_B , Continuous flag sequences are output ("01111110" bit patterns)

Field	Bits	Type	Description
XMFA	2	rw	**Transmit Multiframe Aligned** Determines the synchronization between the framer and the corresponding signaling controller. *Note: During the transmission of the XFIFO content, the $\overline{SYPX}$ or XMFS interval time should not be changed, otherwise the XFIFO data has to be retransmitted.* 0_B , The contents of the XFIFO is transmitted without multiframe alignment. 1_B , The contents of the XFIFO is transmitted multiframe aligned. The first byte in XFIFO is transmitted in the first time slot selected by TTR(4:1) and so on. After reception of a complete multiframe in the time slot mode (RTR(4:1)) an ISR0.RME interrupt is generated, if no HDLC mode is enabled. In Sa-bit access mode XMFA is not valid.
RFT1	1:0	rw	**RFIFO Threshold Level - HDLC Channel 1** The size of the accessible part of RFIFO can be determined by programming these bits and the bit MODE.RFT2. If MODE.RFT2 = ´1´ these bits are not valid and the accessable receive FIFO size is 64 byte. The value of RFT(2:0) can be changed dynamically. See **Table 10** • If reception is not running or • After the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer). *Note: Changing of the value of RFT(2:0) is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after a RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by a RMC command (see table **RFT Constant Values**).* 000_B , 32 bytes (default value) 001_B , 16 bytes 010_B , 4 bytes 011_B , 2 bytes $1xx_B$, 64 bytes

Similar Registers

Table 67 RFT Constant Values

Name and Description	Value
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(5:0)	$1xx_B$
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(4:0)	000_B
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(3:0)	001_B

Table 67 RFT Constant Values (cont'd)

Name and Description	Value
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(1:0)	010_B
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC0	011_B

Common Configuration Register 2

Note: Unused bits have to be cleared.

CCR2_E	Offset	Reset Value
Common Configuration Register 2	$xx0A_H$	00_H

7	6	5	4	3	2	1	0
Res		TSFL	RADD	Res	RCRC	XCRC	Res
		rw	rw		rw	rw	

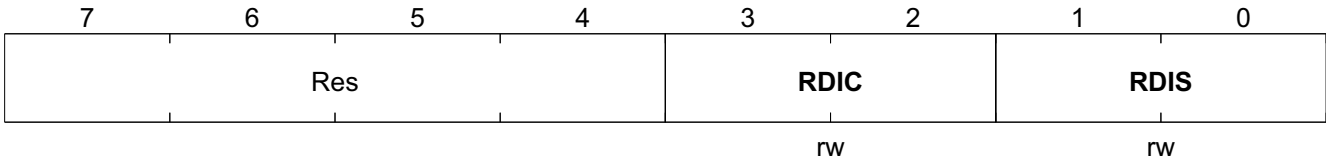
Field	Bits	Type	Description
TSFL	5	rw	**Enable Shared Flags in Transmit Direction** In receive direction shared flag is detected automatically 0_B , Both, an opening and a closing flag (´7Eh´) are transmitted for each HDLC frame (normal operation). 1_B , The closing flag (´7Eh´) of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one to be transmitted.
RADD	4	rw	**Receive Address Pushed to RFIFO - HDLC Channel 1** If this bit is set, the received HDLC address information (1 or 2 bytes, depending on the address mode selected by MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode and transparent mode 1.RADD must be set, if SS7 mode is selected, see **Chapter 4.3.2**.
RCRC	2	rw	**Receive CRC on/off - HDLC Channel 1** Only applicable in non-auto mode. If this bit is set, the received CRC checksum is written to RFIFO(CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed by the status information byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If non-auto mode is selected, the limits for “valid frame” check are modified (refer toRSIS.VFR), see **Chapter 4.3.2**.
XCRC	1	rw	**Transmit CRC on/off - HDLC Channel 1** If this bit is set, the CRC checksum is not generated internally.It has to be written to the transmit FIFO as the last two bytes. The transmitted frame is closed automatically with a closing flag. *Note: The OctalFALCTM does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.*

Framer Mode Register 4

Configures the condition when to clear and when to set the bit FRS1.RDI.

Note: Unused bits have to be cleared.

RDICR_E	Offset	Reset Value
RDI Clear Condition Register	**xx0B$_H$**	**00$_H$**



Field	Bits	Type	Description
RDIC	3:2	rw	**RDI Clear Condition** 00_B , RA condition must be gone for at least 1 multiframe/double frame. 01_B , RA condition must be gone for at least 2 multiframe/double frame. 10_B , RA condition must be gone for at least 3 multiframe/double frame. 11_B , RA condition must be gone for at least 4 multiframe/double frame.
RDIS	1:0	rw	**RDI Set Condition** 00_B , RDI condition must be detected for at least 1 multiframe/double frame. 01_B , RDI condition must be detected for at least 2 multiframe/double frame. 10_B , RDI condition must be detected for at least 3 multiframe/double frame. 11_B , RDI condition must be detected for at least 4 multiframe/double frame.

Receive Time Slot Register 1

See **Chapter 4.6.4**.

RTR1_E	Offset	Reset Value
Receive Time Slot Register 1	**xx0C$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
TS0	**TS1**	**TS2**	**TS3**	**TS4**	**TS5**	**TS6**	**TS7**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS0	7	rw	**Time Slot** These bits define the received time slots on the system highway port RDO to be extracted to RFIFO and marked. Additionally these registers control the RSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.A one in the RTR(4:1) bits samples the corresponding time slots and send their data to the RFIFO of the signaling controller if bit CCR1.EITS is set.Assignments: TS0 is assigned to Time slot 0...TS31 is assigned to Time slot 31 0_B , The corresponding time slot is not extracted and stored into the RFIFO. 1_B , The contents of the selected time slot is stored in the RFIFO. Although the idle time slots can be selected. This function is activated, if bit CCR1.EITS is set. The corresponding time slot is forced high on marker pin RSIGM.
TS1	6		
TS2	5		
TS3	4		
TS4	3		
TS5	2		
TS6	1		
TS7	0		

Similar Registers

Registers RTR2 to RTR4 have the same description. Their reset values are ´00$_H$´.

The Offset Addresses are listed in **RTRn Overview**, for bit names and layout refer to **Receive Time Slot Registers**.

Table 68 RTRn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
RTR2	Receive Time Slot Register 2	0D$_H$	
RTR3	Receive Time Slot Register 3	0E$_H$	
RTR4	Receive Time Slot Register 4	0F$_H$	

Table 69 Receive Time Slot Registers

	7	6	5	4	3	2	1	0
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

Transmit Time Slot Register 1

See **Chapter 4.6.4**.

TTR1_E	Offset	Reset Value
Transmit Time Slot Register 1	$xx10_H$	00_H

7	6	5	4	3	2	1	0
TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS0	7	rw	**Time Slot** These bits define the transmit time slots on the system highway to be inserted. Additionally these registers control the XSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.A one in the TTR(4:1) bits inserts the corresponding time slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EITS is cleared insertion of data received on port XSIG is controlled by this registers. Assignments: TS0 is assigned to Time slot 0 ...TS31 is assigned to Time slot 31 0_B , The selected time slot is not inserted into the outgoing data stream. 1_B , The contents of the selected time slot is inserted into the outgoing data stream from XFIFO. This function is active only if bit CCR1.EITS is set. The corresponding time slot is forced high on marker pin XSIGM.
TS1	6		
TS2	5		
TS3	4		
TS4	3		
TS5	2		
TS6	1		
TS7	0		

Similar Registers

Registers TTR2 to TTR4 have the same description. Their reset values are ´00_H´.

The Offset Addresses are listed in **TTRn Overview**, for bit names and layout refer to **Transmit Time Slot Registers**.

Table 70 TTRn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
TTR2	Transmit Time Slot Register 2	11_H	
TTR3	Transmit Time Slot Register 3	12_H	
TTR4	Transmit Time Slot Register 4	13_H	

Table 71 Transmit Time Slot Registers

	7	6	5	4	3	2	1	0
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15

Table 71 Transmit Time Slot Registers (cont'd)

TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

Interrupt Mask Register 0

Each interrupt source can generate an interrupt signal on port INT (or INT1 and INT2 respectively). Characteristics of the output stage are defined by register IPC. A “1” in a bit position of IMR(7:0) sets the mask active for the interrupt status in ISR(7:0). Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are- not displayed in the interrupt status register if bit GCR.VIS is cleared- displayed in the interrupt status register if bit GCR.VIS is set, see **Chapter 3.4.4**.

Note: After reset, all interrupts are disabled.

IMR0_E	Offset	Reset Value
Interrupt Mask Register 0	**$xx14_H$**	**FF_H**

7	6	5	4	3	2	1	0
RME	**RFS**	**T8MS**	**RMB**	**CASC**	**CRC4**	**SA6SC**	**RPF**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RME	7	rw	**Interrupt Mask Register** Each interrupt source can generate an interrupt signal on port INT (or INT1 and INT2 respectively). Characteristics of the output stage are defined by register IPC. A ´1´ in a bit position of IMR(7:0) sets the mask active for the interrupt status in ISR(7:0). Mask interrupt statuses neither generate a signal on INT (INT1, INT2), not are they visible in register GIS. Moreover they are not displayed in the interrupt status register if bit GCR.VIS is cleared; they are displayed in the interrupt status register if bit GCR.VIS is set.
RFS	6		
T8MS	5		
RMB	4		
CASC	3		
CRC4	2		
SA6SC	1		
RPF	0		

Similar Registers

Registers IMR1 to IMR5 have the same description. Their reset values are ´FF_H´.

The Offset Addresses are listed in **IMRn Overview**, for bit names and layout refer to **Interrupt Mask Registers**.

Table 72 IMRn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
IMR1	Interrupt Mask Register 1	15_H	
IMR2	Interrupt Mask Register 2	16_H	
IMR3	Interrupt Mask Register 3	17_H	
IMR4	Interrupt Mask Register 4	18_H	
IMR5	Interrupt Mask Register 5	19_H	
IMR6	Interrupt Mask Register 6	$1A_H$	
IMR7	Interrupt Mask Register 7	DF_H	

Table 73 Interrupt Mask Registers

Bit number	7	6	5	4	3	2	1	0
IMR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF

Table 73 Interrupt Mask Registers (cont'd)

IMR1	LLBSC	RDO	ALLS	XDU	XMB	SUEX	XLSC	XPR
IMR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA
IMR3	ES	SEC	LMFA16	AIS16	RA16	LTC	RSN	RSP
IMR4	XSP	XSN	RME2	RFS2	RDO2	ALLS2	XDU2	RPF2
IMR5	XPR2	XPR3	RME3	RFS3	RDO3	ALLS3	XDU3	RPF3
IMR6	SOLSU	SOLSD	LOLSU	LOLSD	SILSU	SILSD	LILSU	LILSD
IMR7				XCLKSS1	XCLKSS0			

IMR3.LTC masks the status it ISR3.LTC.

Loop code monitoring with registers ISR6 and IMR6 might not be necessary in both directions (line and system side) simultaneously.

Single Bit Defect Insertion Register

After setting the corresponding bit, the selected defect is inserted into the transmit data stream at the next possible position. After defect insertion is completed, the bit is reset automatically. See **Chapter 4.7.7**.

IERR_E	Offset	Reset Value
Single Bit Defect Insertion Register	**xx1B$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res		**IFASE**	**IMFE**	**ICRCE**	**ICASE**	**IPE**	**IBV**
		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IFASE	5	rw	**Insert single FAS defect** 0_B , no insertion. 1_B , a FAS defect is inserted into the transmit data stream.
IMFE	4	rw	**Insert single multiframe defect** 0_B , no insertion. 1_B , a multiframe defect is inserted into the transmit data stream.
ICRCE	3	rw	**Insert single CRC defect** 0_B , no insertion. 1_B , a CRC defect is inserted into the transmit data stream.
ICASE	2	rw	**Insert single CAS defect** 0_B , no insertion. 1_B , a CAS defect is inserted into the transmit data stream.
IPE	1	rw	**Insert single PRBS defect** 0_B , no insertion. 1_B , a PRBS defect is inserted into the transmit data stream.
IBV	0	rw	**Insert bipolar violation** *Note: Except for CRC defects, CRC checksum calculation is done after defect insertion.* 0_B , no insertion. 1_B , a bipolar violation defect is inserted into the transmit data stream.

Framer Mode Register 0

FMR0_E	Offset	Reset Value
Framer Mode Register 0	$xx1C_H$	00_H

7	6	5	4	3	2	1	0
XC		RC		EXZE	ALM	FRS	SIM
rw		rw		rw	rw	rw	rw

Field	Bits	Type	Description
XC	7:6	rw	**Transmit Code** Serial line code for the transmitter, independent of the receiver. After changing XC(1:0), a transmitter software reset is required (CMDR.XRES = 1). See **Chapter 3.7.1**. 00_B , NRZ (optical interface) 01_B , CMI (1T2B+HDB3), (optical interface) 10_B , AMI (ternary or digital dual-rail interface) 11_B , HDB3 Code (ternary or digital dual-rail interface)
RC	5:4	rw	**Receive Code** Serial line code for the receiver, independent of the transmitter. After changing RC(1:0), a receiver software reset is required (CMDR.RRES = ´1´). See **Chapter 3.6.1**. 00_B , NRZ (optical interface) 01_B , CMI (1T2B+HDB3), (optical interface) 10_B , AMI (ternary or digital dual-rail interface) 11_B , HDB3 Code (ternary or digital dual-rail interface)
EXZE	3	rw	**Extended HDB3 Error Detection** Selects error detection mode. 0_B , Only double violations are detected. 1_B , Extended code violation detection: 0000 strings are detected additionally. Incrementing of the code violation counter CVC is done after receiving four zeros. Errors are indicated by FRS1.EXZD = ´1´. If HDB3 code is enabled, counting of bipolar violations in substitution patterns is only done, if the violation bits of two consecutive substitution patterns have different polarities.

Field	Bits	Type	Description
ALM	2	rw	**Alarm Mode** Selects the AIS alarm detection mode. 0_B , The AIS alarm is detected according to ETS300233. Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros within a period of 512 bits and a loss of frame alignment is indicated. Recovery: The alarm is cleared if 3 or more zeros within 512 bits are detected or the FAS word is found. 1_B , The AIS alarm is detected according to ITU-T G.775 Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros in each doubleframe period of two consecutive doubleframe periods (1024 bits). Recovery: The alarm is cleared if 3 or more zeros are detected within two consecutive doubleframe periods.
FRS	1	rw	**Force Resynchronization** A transition from low to high initiates a resynchronization procedure of the pulse frame and the CRC-multiframe (if enabled by bit FMR2.RFS1) starting directly after the old framing candidate.
SIM	0	rw	**Alarm Simulation** SIM has to be held stable at high or low level for at least one receive clock period before changing it again. 0_B , Normal operation. 1_B , Initiates internal error simulation of AIS, loss-of-signal, loss of synchronization, remote alarm, slip, framing errors, CRC errors, and code violations. The error counters FEC, CVC, CEC1 are incremented.

Framer Mode Register 1

FMR1_E	Offset	Reset Value
Framer Mode Register 1	$xx1D_H$	00_H

7	6	5	4	3	2	1	0
MFCS	AFR	ENSA	PMOD	XFS	ECM	SSD0	XAIS
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MFCS	7	rw	**Multiframe Force Resynchronization** Only valid if CRC multiframe format is selected (FMR2.RFS(1:0) = 10). A transition from low to high initiates the resynchronization procedure for CRC-multiframe alignment without influencing doubleframe synchronous state. In case, “Automatic Force Resynchronization” (FMR1.AFR) is enabled and multiframe alignment cannot be regained, a new search of doubleframe (and CRC multiframe) is automatically initiated.
AFR	6	rw	**Automatic Force Resynchronization** Only valid if CRC multiframe format is selected (FMR2.RFS(1:0) = 10). If this bit is set, a search of doubleframe alignment is automatically initiated if two multiframe patterns with a distance of n x 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained or command FMR1.MFCS has been issued.
ENSA	5	rw	**Enable Sa-Bit Access through Register XSA4-8** Only applicable if FMR1.XFS is set. 0_B , Normal operation. The Sa-bit information is taken from bits XSW.XY(4:0) and written to bits RSW.RY(4:0). 1_B , Sa-bit register access. The Sa-bit information is taken from the registers XSA(8:4). In addition, the received information is written to registers RSA(8:4). Transmitting of the contents of registers XSA(8:4) is disabled if one of time slot 0 transparent modes is enabled (XSP.TT0 or TSWM.SA(8:4)).
PMOD	4	rw	**PCM Mode** This bit decides between E1 and T1/J1 mode. Switching from E1 to T1 or vice versa the device needs up to 20 µs to settle up to the internal clocking. 0_B , PCM 30 or E1 mode. 1_B , PCM 24 or T1/J1 mode (see RC0.SJR for T1/J1 selection).
XFS	3	rw	**Transmit Framing Select** Selection of the transmit framing format can be done independently of the receive framing format. 0_B , Doubleframe format enabled. 1_B , CRC4-multiframe format enabled.

Field	Bits	Type	Description
ECM	2	rw	**Error Counter Mode** The function of the error counters is determined by this bit. 0_B , Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8-bit access the low byte of the error counter should always be read before the high byte. The error counters are reset with the rising edge of the corresponding bits in the DEC register. 1_B , Every second the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided (do not access an error counter within 1 µs after the one-second interrupt occurs).
SSD0	1	rw	**Select System Data Rate 0** FMR1.SSD0 and SIC1.SSD1 define the data rate on the system highway. See **Chapter 4.6**. Programming is done with SSD1/SSD0 in the following table. 00_B , 2.048 Mbit/s 01_B , 4.096 Mbit/s 10_B , 8.192 Mbit/s 11_B , 16.384 Mbit/s
XAIS	0	rw	**Transmit AIS Towards Remote End** Sends AIS on ports XL1, XL2, XOID towards the remote end. The outgoing data stream which can be looped back through the local loop to the system interface is not affected.

Framer Mode Register 2

FMR2_E	Offset	Reset Value
Framer Mode Register 2	$xx1E_H$	00_H

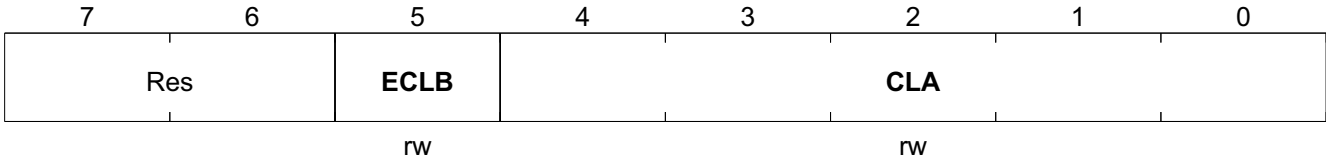
7	6	5	4	3	2	1	0
RFS		RTM	DAIS	SAIS	PLB	AXRA	ALMF
rw		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RFS	7:6	rw	**Receive Framing Select** 00_B , Doubleframe format 01_B , Doubleframe format 10_B , CRC4 Multiframe format 11_B , CRC4 Multiframe format with modified CRC4 Multiframe alignment algorithm (Interworking according to ITU-T G.706 Annex B). Setting of FMR3.EXTIW changes the reaction after the 400 ms time-out.
RTM	5	rw	**Receive Transparent Mode** 0_B , normal mode 1_B , Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of resynchronization of the receiver. This function can be used together with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.This bit should be enabled in case of unframed data reception mode
DAIS	4	rw	**Disable AIS to System Interface** 0_B , AIS is automatically inserted into the data stream to RDO if Octal FALC is in asynchronous state. 1_B , Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.
SAIS	3	rw	**Send AIS Towards System Interface** Sends AIS on output RDO towards system interface. This function is not influenced by bit FMR2.DAIS. 0_B , no sending of AIS 1_B , sending of AIS

Field	Bits	Type	Description
PLB	2	rw	**Payload Loop-Back** See **Chapter 4.7.3**. 0_B , Normal operation. Payload loop is disabled. 1_B , The payload loop-back loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, $\overline{SYPX}$ and XMFS is ignored. With XSP.TT0 = ´1´ time slot 0 is also looped back. If XSP.TT0 = 0 time slot 0 is generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. It is recommended to write the actual value of XC1 into this register once again, because a write access to register XC1 sets the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation (the write operation forces a slip).
AXRA	1	rw	**Automatic Transmit Remote Alarm** 0_B , Normal operation (remote alarm bit is not set automatically) 1_B , The remote alarm bit is set automatically in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is reset. Additionally in multiframe format FMR2.RFS1 = ´1´ and FMR3.EXTIW = ´1´ and the 400 ms time-out has elapsed, the remote alarm bit is active in the outgoing data stream. In multiframe synchronous state the outgoing remote alarm bit is cleared. The remote alarm will be send at least for one second. Superframe Format (F4, F12, F72): Bit 2 in every DS0 channel is forced to zero, even if the payload is not channelized. Extended Superframe Format (ESF): A repeating 16-bit pattern “1111111100000000” is transmitted continuously on the ESF data link. This pattern may be interrupted, while interrupt periods do not exceed 100 ms.
ALMF	0	rw	**Automatic Loss of Multiframe** 0_B , Normal operation 1_B , The receiver searches a new basic and multiframing if more than 914 CRC errors have been detected in a time interval of one second. The internal 914 CRC error counter is reset if the multiframe synchronization is found. Incrementing the counter is only enabled in the multiframe synchronous state.

Channel Loop-Back

LOOP_E	Offset	Reset Value
Channel Loop-Back	$xx1F_H$	00_H



Field	Bits	Type	Description
ECLB	5	rw	**Enable Channel Loop-Back** See **Chapter 4.7.5** 0_B , Disables the channel loop-back. 1_B , Enables the channel loop-back selected by this register.
CLA	4:0	rw	**Channel Address For Loop-Back** CLA = 0 to 31 selects the channel.During looped back the contents of the assigned outgoing channel on ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed at register IDLE. See **Chapter 4.7.5**

Transmit Service Word Pulseframe

XSW_E	Offset	Reset Value
Transmit Service Word Pulseframe	$xx20_H$	00_H

7	6	5	4	3	2	1	0
XSIS	XTM	XRA	XY0	XY1	XY2	XY3	XY4
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XSIS	7	rw	**Spare Bit For International Use** First bit of the service word. Only significant in doubleframe format.If not used, this bit should be fixed to "1". If one of the time slot 0 transparent modes is enabled (bit XSP.TT0, or TSWM.TSIS),bit XSW.XSIS is ignored.
XTM	6	rw	**Transmit Transparent Mode** 0_B , Ports $\overline{SYPX}$/XMFS define the frame/multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FAS-bits according to this framing. Any change of the transmit time slot assignment subsequently produces a change of the FAS-bit positions. 1_B , Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to actualize the multiframe position. The framing (FAS-bits) generated by the transmitter is not “disturbed” (in case of changing the transmit time slot assignment) by the transmit system highway unless register XC1 is written. Useful in loop-timed applications. For proper operation the transmit elastic buffer (2 frames, SIC1.XBS(1:0) = 10) has to be enabled.
XRA	5	rw	**Transmit Remote Alarm** 0_B , Normal operation. 1_B , Sends remote alarm towards remote end by setting bit 3 of the service word. If time slot 0 transparent mode is enabled by bit XSP.TT0 or TSWM.TRA bit is set, bit XSW.XRA is ignored.
XY0	4	rw	**Spare Bits For National Use (Y-Bits, Sn-Bits, Sa-Bits)** These bits are inserted in the service word of every other pulseframe if Sa-bit register access is disabled (FMR1.ENSA = 0). If not used, they should be fixed to “1”. If one of the time slot 0 transparent modes is enabled (bit XSP.TT0 or TSWM.TSA(8:4)), bits XSW.XY(4:0) are ignored.
XY1	3		
XY2	2		
XY3	1		
XY4	0		

Transmit Spare Bits

XSP_E	Offset	Reset Value
Transmit Spare Bits	$xx21_H$	00_H

7	6	5	4	3	2	1	0
Res	**CASEN**	**TT0**	**EBP**	**AXS**	**XSIF**	**XS13**	**XS15**
	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CASEN	6	rw	**Channel Associated Signaling Enable** 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to send the CAS information stored in the XS(16:1) registers or serial CAS data in the corresponding time slots.
TT0	5	rw	**Time slot 0 Transparent Mode** 0_B , Normal operation. 1_B , All information for time slot 0 on port XDI is inserted in the outgoing pulseframe. All internal information of the OctalFALC™ (framing, CRC, Sa/Si-bit signaling, remote alarm) is ignored. This function is mainly useful for system test applications (test loops), see **Chapter 4.7.3**. Priority sequence of transparent modes: XSP.TTO > TSWM.
EBP	4	rw	**E-Bit Polarity** 0_B , In the basic and multiframe asynchronous state the E-bit is cleared. 1_B , In the basic- and multiframe asynchronous state the E-bit is set. If automatic transmission of submultiframe status is enabled by setting bit XSP.AXS and the receiver has lost synchronization, the E-bit with the programmed polarity is inserted automatically in Si-bit position of every outgoing CRC multiframe (under the condition that time slot 0 transparent mode and transparent Si bit in service word are both disabled).
AXS	3	rw	**Automatic Transmission of Submultiframe Status** Only applicable to CRC multiframe. 0_B , Normal operation. 1_B , Information of submultiframe status bits RSP.SI1 and RSP.SI2 are inserted automatically in Si -bit positions of the outgoing CRC multiframe (RSP.SI1 → Si -bit of frame 13; RSP.SI2 → Si-bit of frame 15). Contents of XSP.XS13 and XSP.XS15 is ignored. If one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.AXS has no function.

Field	Bits	Type	Description
XSIF	2	rw	**Transmit Spare Bit For International Use (FAS Word)** First bit in the FAS word. Only significant in doubleframe format. If not used, this bit should be fixed to "1". If one of the time slot 0 transparent modes is enabled (bits XSP.TT0, or TSWM.TSIF), bit XSP.XSIF is ignored.
XS13	1	rw	**Transmit Spare Bit (Frame 13, CRC-Multiframe)** First bit in the service word of frame 13 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to "1". The information of XSP.XS13 is shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe. If automatic transmission of submultiframe status is enabled by bit XSP.AXS, or, if one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.XS13 is ignored.
XS15	0	rw	**Transmit Spare Bit (Frame 15, CRC-Multiframe)** First bit in the service word of frame 15 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to "1". The information of XSP.XS15 is shifted into the internal transmission buffer with beginning of the next following transmitted CRC multiframe. If automatic transmission of submultiframe status is enabled by bit XSP.AXS, or, if one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIF is enabled, bit XSP.XS15 is ignored.

Transmit Control 0

XC0_E	Offset	Reset Value
Transmit Control 0	$xx22_H$	00_H

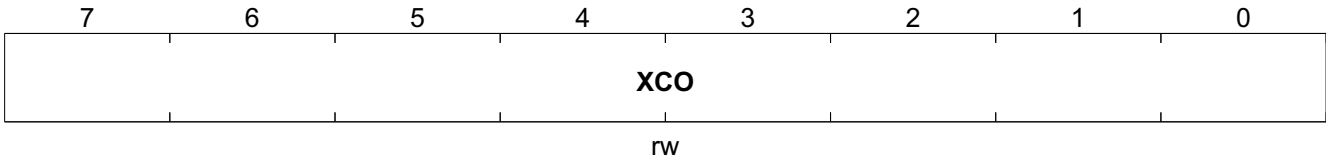
7	6	5	4	3	2	1	0
SA8E	SA7E	SA6E	SA5E	SA4E	XCO10	XCO9	XCO8
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SA8E	7	rw	**Sa-Bit Signaling Enable** 0_B , Standard operation. 1_B , Setting this bit makes it possible to send/receive a LAPD protocol in any combination of the Sa-bit positions in the outgoing/incoming data stream. The on chip signaling controller has to be configured in the HDLC/LAPD mode. In transmit direction together with these bits the TSWM.TSA(8:4) bits must be set to enable transmission to the remote end transparently through the QuadFALC®.
SA7E	6		
SA6E	5		
SA5E	4		
SA4E	3		
XCO10	2	rw	**Transmit Offset** Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse on port $\overline{\text{SYPX}}$/XMFS is active Refer to register XC1.
XCO9	1		
XCO8	0		

Transmit Control 1

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating the value should only be done when the QuadFALC® is initialized or when the buffer should be centered. As a consequence a transmit slip will occur. See **Chapter 4.6.3.1**.

XC1_E	Offset	Reset Value
Transmit Control 1	$xx23_H$	$9C_H$



Field	Bits	Type	Description
XCO	7:0	rw	**Transmit Offset** Calculation of delay time T (SCLKX cycles) depends on the value X of the “Transmit Offset” register XC(1:0): • $0 \leq T \leq 4$: X = 4 - T • $5 \leq T \leq$ maximum delay: X = 256 x SC/SD - T + 4) With maximum delay = (256 x SC/SD) -1 and with SC = system clock defined by SIC1. SSC(1:0) and with SD = 2.048 MHz Delay time T = time between beginning of time slot 0 (bit 0, channel phase 0) at XDI/XSIG and the initial edge of SCLKX after $\overline{\text{SYPX}}$/XMFS goes active. See **Chapter 4.6.3.1** for further description.

Receive Control 0

RC0_E	Offset	Reset Value
Receive Control 0	$xx24_H$	00_H

7	6	5	4	3	2	1	0
SWD	ASY4	CRCI	XCRCI	RDIS	RCO10	RCO9	RCO8
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SWD	7	rw	**Service Word Condition Disable** 0_B , Standard operation. Three or four consecutive incorrect service words (depending on bit RC0.ASY4) causes loss of synchronization. 1_B , Errors in service words have no influence when in synchronous state. However, they are used for the resynchronization procedure.
ASY4	6	rw	**Select Loss of Sync Condition** 0_B , Standard operation. Three consecutive incorrect FAS words or three consecutive incorrect service words causes loss of synchronization. 1_B , Four consecutive incorrect FAS words or four consecutive incorrect service words causes loss of synchronization. The service word condition is disabled by bit RC0.SWD.
CRCI	5	rw	**Automatic CRC4 Bit Inversion** If set, all CRC bits of one outgoing submultiframe are inverted in case a CRC error is flagged for the previous received submultiframe. This function is logically ored with RC0.XCRCI.
XCRCI	4	rw	**Transmit CRC4 Bit Inversion** If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ored with RC0.CRCI.
RDIS	3	rw	**Receive Data Input Sense** Digital interface, dual-rail: see table RDIS Constant Values (Case 1) Digital Interface, CMI: see table RDIS Constant Values (Case 2)
RCO10	2	rw	**Receive Offset/Receive Frame Marker Offset** Depending on the RP(A to D) pin function different offsets can be programmed. The $\overline{SYPR}$ and the RFM pin function cannot be selected in parallel. • **Receive Offset/** • **Receive Frame Marker Offset**
RCO9	1		
RCO8	0		

Table 74 RDIS Constant Values (Case 1)

Name and Description	Value
Digital Interface, dual rail Inputs RDIP/RDIN are active low	0_B
Digital Interface, dual rail Inputs RDIP/RDIN are active high	1_B

Table 75 RDIS Constant Values (Case 2)

Name and Description	Value
Digital Interface, DCIM Input ROID is active high	0_B
Digital Interface, DCIM Input ROID is active low	1_B

Receive Offset/Receive Frame Marker Offset

Depending on the configurations on multifunction ports RPA to RPC different offsets can be programmed.

Receive Offset/

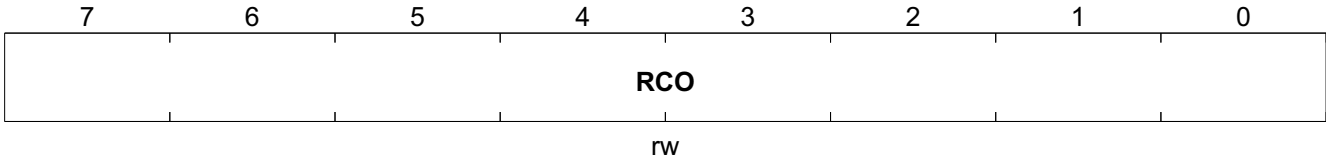
(PC(3:1).RPC(3:0) = ´0000_B´): Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse on port $\overline{\text{SYPR}}$ is active. Calculation of delay time T (SCLKR cycles) depends on the value X of the receive offset register RC(1:0). For programming refer to register RC1.

Receive Frame Marker Offset

(PC(3:1).RPC(3:0) = ´0001_b´): Offset programming of the receive frame marker which is output on port SYPR. The receive frame marker can be activated during any bit position of the current frame. Calculation of the value X of the receive offset register RC(1:0) depends on the bit position which should be marked and SCLKR. Refer to register RC1.

Receive Control 1

RC1_E	Offset	Reset Value
Receive Control 1	$x25_H$	$9C_H$



Field	Bits	Type	Description
RCO	7:0	rw	**Receive Offset/Receive Frame Marker Offset** Depending on the RP(A to D) pin function different offsets can be programmed. The SYPR and the RFM pin function cannot be selected in parallel. • **Receive Offset** • **Receive Frame Marker Offset**

Receive Offset

PC(3:1).RPC(3:0) = ´0000_b´: Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse on port SYPR is active. Calculation of delay time T (SCLKR cycles) depends on the value X of the receive offset register RC(1:0):

$0 \leq T \leq 4$: X = 4 - T

$5 \leq T \leq$ maximum delay: X = 2052 - T

- Maximum delay = (256 x SC/SD) -1
- SC = system clock defined by SIC1.SSC(1:0)
- SD = system data rate

See **Chapter 5.6.2.1** fur further description.

Receive Frame Marker Offset

PC(3:1).RPC(3:0) = ´0001_b´: Offset programming of the receive frame marker which is output on multifunction port RFM. The receive frame marker can be activated during any bit position of the entire frame and depends on the selected system clock rate. Calculation of the value X of the receive offset register RC(1:0) depends on the bit position which should be marked at marker position MP:

$0 \leq MP \leq 2045$: X = MP + 2

$2046 \leq MP \leq 2047$: X = MP - 2046

E.g: 2.048 MHz: MP = 0 to 255; up to 16.384 MHz: MP = 0 to 2047

See **Chapter 5.6.2.1** fur further description.

Transmit Pulse Mask 0

See **Chapter 3.7.5** and **Chapter 3.7.5.1**. The transmit pulse shape which is defined in ITU-T G.703 is output on pins XL1 and XL2. The level of the pulse shape can be programmed by registers XPM(2:0) if XPM2.XPDIS is set to ´0´ to create a custom waveform. If XPM2.XPDIS is set to ´1´, the custom waveform can be programed by the registers TXP(16:1) and the register bits of XPM(2:0) are unused with exception of the bits XPM2.XLT, XPM2.DAXLT and XPM2.XPDIS. In order to get an optimized pulse shape for the external transformers each pulse shape is internally divided into four sub pulse shapes if XPM2.XPDIS is set to ´0´. In each sub pulse shape a programmed 5-bit value defines the level of the analog voltage on pins XL1/2. Together four 5-bit values have to be programmed to form one complete transmit pulse shape. The four 5-bit values are sent in the following sequence:

XP04 to 00: First pulse shape level

XP14 to 10: Second pulse shape level

XP24 to 20: Third pulse shape level

XP34 to 30: Fourth pulse shape level.

Changing the LSB of each subpulse in registers XPM(2:0) changes the amplitude of the differential voltage on XL1/2 by approximately 80 mV. Recommended values for standard applications are given in **Table 23** and **Table 24**.

Note that in the special cases were the LBO pulse masks are performed in T1 mode, the programming of the pulse masks is done internally, independent on the settings in XPM(2:0).

XPM0_E	Offset	Reset Value
Transmit Pulse Mask0	$xx26_H$	$7B_H$

7	6	5	4	3	2	1	0
XP12	**XP11**	**XP10**	**XP04**	**XP03**	**XP02**	**XP01**	**XP00**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XP12	7	rw	**Bit 2 of second pulse shape level**
XP11	6	rw	**Bit 1 of second pulse shape level**
XP10	5	rw	**Bit 0 (LSB) of second pulse shape level**
XP04	4	rw	**Bit 4 (MSB) of first pulse shape level**
XP03	3	rw	**Bit 3 of first pulse shape level**
XP02	2	rw	**Bit 2 of first pulse shape level**
XP01	1	rw	**Bit 1 of first pulse shape level**
XP00	0	rw	**Bit 0 (LSB) of first pulse shape level**

Transmit Pulse Mask 1

For description see **Transmit Pulse Mask 0**

XPM1_E	Offset	Reset Value
Transmit Pulse Mask1	$xx27_H$	03_H

7	6	5	4	3	2	1	0
XP30	**XP24**	**XP23**	**XP22**	**XP21**	**XP20**	**XP14**	**XP13**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XP30	7	rw	**Bit 0 (LSB) of fourth pulse shape level**
XP24	6	rw	**Bit 4 (MSB) of third pulse shape level**
XP23	5	rw	**Bit 3 of third pulse shape level**
XP22	4	rw	**Bit 2 of third pulse shape level**
XP21	3	rw	**Bit 1of third pulse shape level**
XP20	2	rw	**Bit 0 (LSB) of third pulse shape level**
XP14	1	rw	**Bit 4 (MSB) of second pulse shape level**
XP13	0	rw	**Bit 3 of second pulse shape level**

Transmit Pulse Mask 2

For description see **Transmit Pulse Mask 0**

XPM2_E	Offset	Reset Value
Transmit Pulse Mask 2	$xx28_H$	40_H

7	6	5	4	3	2	1	0
0	**XLT**	**DAXLT**	**XPDIS**	**XP34**	**XP33**	**XP32**	**XP31**
r	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
0	7	r	**Always ´0´**
XLT	6	rw	**Transmit Line Tristate** See also **Chapter 3.6.7** and **Table 20**. 0_B , Normal operation 1_B , Transmit line XL1/XL2 or XDOP/XDON are switched into high-impedance state. If this bit is set the transmit line monitor status information is frozen (default value after hardware reset).
DAXLT	5	rw	**Disable Automatic Tristating of XL1/2** See **Chapter 3.7.6**. 0_B , Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high-impedance state. 1_B , If a short is detected on XL1/2 pins automatic setting these pins into a high-impedance (by the XL-monitor) state is disabled.
XPDIS	4	rw	**Disable XPM Values** See **Chapter 3.7.5**. 0_B , XP values from registers XPM(2:0) are used for pulse shaping. 1_B , TXP values from registers TXP(16:1) are used for pulse shaping.
XP34	3	rw	**Bit 4 (MSB) of second pulse shape level** See **Chapter 3.7.5.1**.
XP33	2	rw	**Bit 3 of fourth pulse shape level**
XP32	1	rw	**Bit 2 of fourth pulse shape level**
XP31	0	rw	**Bit 1 of fourth pulse shape level**

Transparent Service Word Mask

TSWM_E	Offset	Reset Value
Transparent Service Word Mask	$xx29_H$	00_H

7	6	5	4	3	2	1	0
TSIS	TSIF	TRA	TSA4	TSA5	TSA6	TSA7	TSA8
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TSIS	7	rw	**Transparent Si-Bit in Service Word** 0_B , The Si-Bit is generated internally. 1_B , The Si-Bit in the service word is taken from port XDI and transparently passed through the OctalFALC™ without any changes. The internal information of the OctalFALC™ (register XSW) is ignored.
TSIF	6	rw	**Transparent Si-Bit in FAS Word** 0_B , The Si-Bit is generated internally. 1_B , The Si-Bit in the FAS word is taken from port XDI and routed transparently through the OctalFALC™ without any changes. The internal information of the OctalFALC™ (register XSW) is ignored.
TRA	5	rw	**Transparent Remote Alarm** 0_B , The remote alarm bit is generated internally. 1_B , The A-Bit is taken from port XDI and routed transparently through the OctalFALC™ without any changes. The internal information of the OctalFALC™ (register XSW) is ignored.
TSA4	4	rw	**Transparent Sa(8:4)-Bit** 0_B , The Sa(8:4)bits are generated internally. 1_B , The Sa(8:4)-bits are taken from port XDI or from the internal signaling controller if enabled and transparently passed through the OctalFALC™ without any changes. The internal information of the OctalFALC™ (registers XSW and XSA(8:4)) is ignored.
TSA5	3		
TSA6	2		
TSA7	1		
TSA8	0		

System Interface Control Register 4

This register configures the clock edge selection of the system interface signals $\overline{\text{SYPR}}$ and $\overline{\text{SYPX}}$ in relation to the clock edge used for the data.

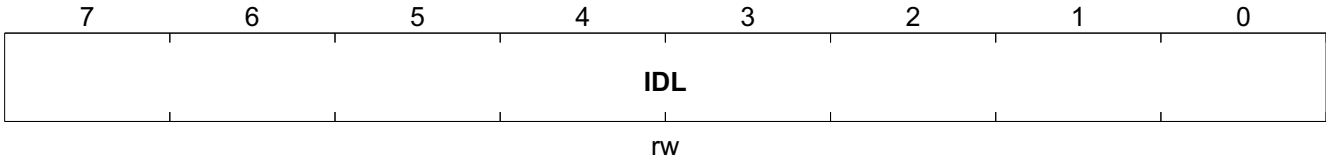
SIC4_E	Offset	Reset Value
System Interface Control Register 4	$xx2A_H$	00_H

7	6	5	4	3	2	1	0
Res					CES	SYPRCE	SYPXCE
					rw	rw	rw

Field	Bits	Type	Description
CES	2	rw	**Clock Edge Selection Enable** This bit enables the function of SYPRCE and $\overline{\text{SYPX}}$CE. 0_B , SYPRCE and SYPXCE are disabled. ($\overline{\text{SYPR}}$ and $\overline{\text{SYPX}}$ are clocked by the same edge as receive interface data and marker.) 1_B , SYPRCE and SYPXCE are enabled.
SYPRCE	1	rw	**SYPR Clock Edge Selection** See **Chapter 4.6** and **SIC1_E**. 0_B , $\overline{\text{SYPR}}$ is clocked by the same edge as receive interface data and marker. 1_B , $\overline{\text{SYPR}}$ is clocked by the opposite edge as receive interface data and marker.
SYPXCE	0	rw	**SYPX Clock Edge Selection** See **Chapter 4.6** and **SIC1_E**. 0_B , $\overline{\text{SYPX}}$ is clocked by the same edge as transmit interface data and marker. 1_B , $\overline{\text{SYPX}}$ is clocked by the same edge as transmit interface data and marker.

Idle Channel Code Register

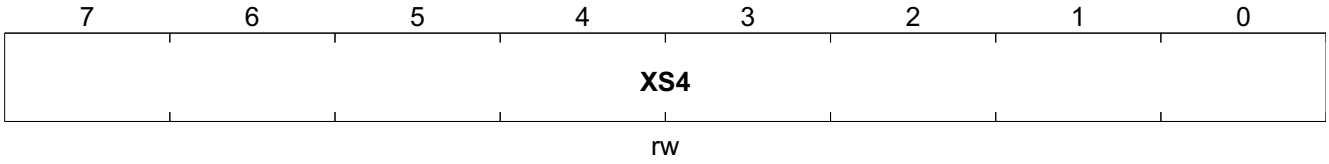
IDLE_E	Offset	Reset Value
Idle Channel Code Register	$xx2B_H$	00_H



Field	Bits	Type	Description
IDL	7:0	rw	**Idle Channel Code** If channel loop-back is enabled by programming LOOP.ECLB = 1, the contents of the assigned outgoing channel on ports XL1/XL2 or XDOP/XDON is set equal to the idle channel code selected by this register.Additionally, the specified pattern overwrites the contents of all channels selected by the idle channel registers ICB(4:1). IDL7 is transmitted first.

Transmit Sa4 Register

XSA4_E	Offset	Reset Value
Transmit Sa4 Register	$xx2C_H$	00_H



Field	Bits	Type	Description
XS4	7:0	rw	**Transmit Sa-Bit Data** The Sa-bit register access is enabled by setting bit FMR1.ENSA = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XSA(8:4) is copied into a shadow register. The contents is subsequently sent out in the service words of the next outgoing CRC multiframe (or doubleframes) if none of the time slot 0 transparent modes is enabled. XS40 is sent out in bit position 4 in frame 1, XS47 in frame 15. The transmit multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information are ignored, current contents is repeated.

Similar Registers

Registers XSA5 to XSA8 have the same description.

The Offset Addresses are listed in **XSAn Overview**, for bit names and layout refer to **Transmit San Registers**.

Table 76 XSAn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
XSA5	Transmit Sa5 Register	$2D_H$	
XSA6	Transmit Sa6 Register	$2E_H$	
XSA7	Transmit Sa7 Register	$2F_H$	
XSA8	Transmit Sa8 Register	30_H	

Table 77 Transmit San Registers

	7	6	5	4	3	2	1	0
XSA4	XS47	XS46	XS45	XS44	XS43	XS42	XS41	XS40
XSA5	XS57	XS56	XS55	XS54	XS53	XS52	XS51	XS50
XSA6	XS67	XS66	XS65	XS64	XS63	XS62	XS61	XS60
XSA7	XS77	XS76	XS75	XS74	XS73	XS72	XS71	XS70
XSA8	XS87	XS86	XS85	XS84	XS83	XS82	XS81	XS80

Framer Mode Register 3

FMR3_E	Offset	Reset Value
Framer Mode Register 3	$xx31_H$	00_H

7	6	5	4	3	2	1	0
Res		**XLD**	**XLU**	**CMI**	**SA6SY**	Res	**EXTIW**
		rw	rw	rw	rw		rw

Field	Bits	Type	Description
XLD	5	rw	**Transmit LLB Down Code** 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down Code is optionally overwritten by the time slot 0 depending on bit LCR1.FLLB.
XLU	4	rw	**Transmit LLB UP Code** 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB UP Code continuously until this bit is reset. The LLB UP Code is overwritten by the time slot 0 depending on bit LCR1.FLLB. For proper operation bit FMR3.XLD must be cleared.
CMI	3	rw	**Select CMI Precoding** Only valid if CMI code (FMR0.XC(1:0) = ´01_b´) is selected. This bit defines the CMI precoding and influences transmit and receive data. *Note: Before local loop is selected, HDB3 precoding has to be disabled.* 0_B , CMI with HDB3 precoding 1_B , CMI without HDB3 precoding
SA6SY	2	rw	**Receive Sa6-Access Synchronous Mode** Only valid if multiframe format (FMR2.RFS(1:0) = ´$1x_b$´) is selected. 0_B , The detection of the predefined Sa6-bit pattern (refer to chapter Sa6-bit detection according to ETS 300233) is done independently of the multiframe synchronous state. 1_B , The detection of the Sa6-bit pattern is done synchronously to the multiframe.

Field	Bits	Type	Description
EXTIW	0	rw	**Extended CRC4 to Non-CRC4 Interworking** Only valid in multiframe format. This bit selects the reaction of the synchronizer after the 400 ms time-out has been elapsed and starts transmitting a remote alarm if FMR2.AXRA is set. 0_B , The CRC4 to Non CRC4 interworking is done as described in ITU-T G. 706 Annex B. 1_B , The interworking is done according to ITU-T G. 706 with the exception that the synchronizer still searches the multiframing even if the 400 ms timer is expired. Switching into doubleframe format is disabled. If FMR2.AXRA is set the remote alarm bit is active in the outgoing data stream until the multiframe is found.

Idle Channel Register 1

ICB1_E	Offset	Reset Value
Idle Channel Register 1	$xx32_H$	00_H

7	6	5	4	3	2	1	0
IC0	IC1	IC2	IC3	IC4	IC5	IC6	IC7
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IC0	7	rw	**Idle Channel Selection Bits** These bits define the channels (time slots) of the outgoing PCM frame to be altered.Assignments:IC0 → Time slot 0; IC1 → Time slot 1;...; .IC31 → Time slot 31 *Note: Although time slot 0 can be selected by bit IC0, its contents is only altered if the transparent mode is selected (XSP.TT0).* 0_B , Normal operation. 1_B , Idle channel mode. The contents of the selected time slot is overwritten by the idle channel code defined by register IDLE.
IC1	6		
IC2	5		
IC3	4		
IC4	3		
IC5	2		
IC6	1		
IC7	0		

Similar Registers

Registers ICB2 to ICB4 have the same description and layout.

The Offset Addresses are listed in **ICBn Overview**, for bit names refer to **Idle Channel Registers**.

Table 78 ICBn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
ICB2	Idle Channel Register 2	33_H	
ICB3	Idle Channel Register 3	34_H	
ICB4	Idle Channel Register 4	35_H	

Table 79 Idle Channel Registers

	7	6	5	4	3	2	1	0
ICB1	IC0	IC1	IC2	IC3	IC4	IC5	IC6	IC7
ICB2	IC8	IC9	IC10	IC11	IC12	IC13	IC14	IC15
ICB3	IC16	IC17	IC18	IC19	IC20	IC21	IC22	IC23
ICB4	IC24	IC25	IC26	IC27	IC28	IC29	IC30	IC31

Line Interface Mode 0

LIM0_E	Offset	Reset Value
Line Interface Mode 0	$xx36_H$	00_H

7	6	5	4	3	2	1	0
XFB	XDOS	RTRS	DCIM	EQON	RLM	LL	MAS
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XFB	7	rw	**Transmit Full Bauded Mode** Only applicable for dual-rail mode (bit LIM1.DRS = ´1´). *Note: If CMI coding is selected (FMR0.XC(1:0) = ´01_b´) this bit has to be cleared.* 0_B , Output signals XDOP/XDON are half bauded. 1_B , Output signals XDOP/XDON are full bauded.
XDOS	6	rw	**Transmit Data Out Sense** *Note: If CMI coding is selected (FMR0.XC(1:0) = ´01_b´) this bit has to be cleared. The transmit frame marker XFM is independent of this bit.* 0_B , Output signals XDOP/XDON are active low. Output XOID is active high (normal operation). 1_B , Output signals XDOP/XDON are active high. Output XOID is active low.
RTRS	5	rw	**Receive Termination Resistance Selection** This bit controls the analog switch of the receive line interface, see Chapter 3.6.6. *Note: If the RLT functionality is selected at one of the multi function ports, a logical equivalence is build out of RTRS and RLT for controlling the analog switch. If RLT functionality is not configured at one of the multi function ports, the analog switch is controlled only by RTRS.* 0_B , analog is switched off. 1_B , analog switch is switched on.
DCIM	4	rw	**Digital Clock Interface Mode** *Note: DCO-X must be used in DCIM mode (CMR1.DXJA = ´0´).* 0_B , normal operation. 1_B , enables the digital Clock Interface Mode (synchronization interface mode) according to ITU-T G.703, Section 13. A 2048/1544 kHz clock is expected on RL1/2. On XL1/2 a 2048/1544 kHz output clock is driven. The transmit clock signal on XL1/2 is derived from the clock supplied on SCLKX (CMR1.DXSS = ´0´).

Field	Bits	Type	Description
EQON	3	rw	**Receive Equalizer On** *Note: This function is no longer used. The receive equalizer automatically adapts to the incoming signal level. This bit is ignored to assure software compatibility with QuadFALC®.*
RLM	2	rw	**Receive Line Monitoring** See **Chapter 3.6.7**. 0_B , Normal receiver mode 1_B , Receiver mode for receive line monitoring; the receiver sensitivity is increased to detect resistively attenuated signals of -20 dB (short-haul mode only)
LL	1	rw	**Local Loop** See **Chapter 4.7.4**. 0_B , Normal operation 1_B , Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream is transmitted undisturbedly on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transferred through the complete analog receiver.
MAS	0	rw	**Master Mode** See also **Table 16**. 0_B , Slave mode 1_B , Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (2.048 MHz or 8 kHz, see IPC.SSYF) supplied by SYNC. If this pin is connected to VSS or VDD (or left open and pulled up to VDD internally) the DCO-R circuitry is centered and no receive jitter attenuation is performed (only if 2.048 MHz clock is selected by resetting bit IPC.SSYF). The generated clocks are stable.

Line Interface Mode 1

LIM1_E	Offset	Reset Value
Line Interface Mode 1	$xx37_H$	80_H

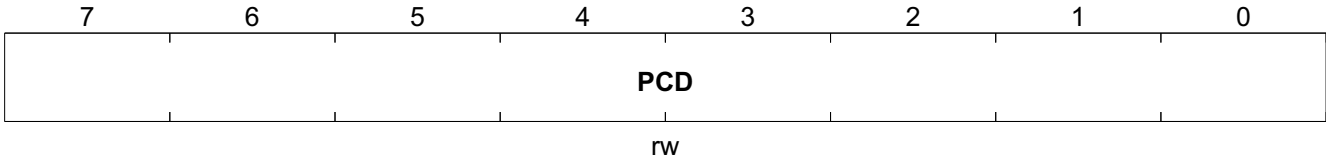
7	6	5	4	3	2	1	0
CLOS	**RIL2**	**RIL1**	**RIL0**	Res	**JATT**	**RL**	**DRS**
rw	rw	rw	rw		rw	rw	rw

Field	Bits	Type	Description
CLOS	7	rw	**Clear data in case of LOS** 0_B , Normal receiver mode, receive data stream is transferred normally in long-haul mode 1_B , received data is cleared (driven to low level), as soon as LOS is detected
RIL2	6	rw	**Receive Input Threshold** Only valid if analog line interface is selected (LIM1.DRS = ´0´).“No signal” is declared if the voltage between pins RL1 and RL2 drops below the limits programmed by bits RIL(2:0) and the received data stream has no transition for a period defined in the PCD register. See **Chapter 5.1.2** and the DC characteristics (**Table 139**) for detail.
RIL1	5	rw	
RIL0	4	rw	
JATT	2	rw	**Transmit Jitter Attenuator** *Note: JATT is only used to define the jitter attenuation during remote loop operation. Remote loop operation can be set by LIM1.RL or by automatic loop switching by BOM messages. Jitter attenuation during normal operation is not affected by JATT.* 0_B , Transmit jitter attenuator is disabled for remote Loop. Transmit data bypasses the remote loop jitter attenuator buffer. 1_B , Jitter attenuator is active for remote loop. Received data from pins RL1/2 or RDIP/N or ROID is sent "jitter-free" on ports XL1/2 or XDOP/N or XOID. The de-jittered clock is generated by the DCO-X circuitry.
RL	1	rw	**Remote Loop** *Note: RL is logically ored with automatic loop switching by BOM messages.* 0_B , Normal operation. 1_B , Remote Loop active.

Field	Bits	Type	Description
DRS	0	rw	**Dual-Rail Select** 0_B , The ternary interface is selected. Ports RL1/2 and XL1/2 become analog in/outputs. 1_B , The digital dual-rail interface is selected. Received data is latched on ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register

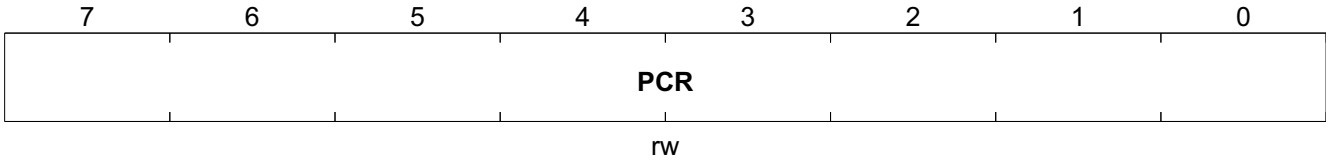
PCD_E	Offset	Reset Value
Pulse Count Detection Register	$xx38_H$	00_H



Field	Bits	Type	Description
PCD	7:0	rw	**Pulse Count Detection** A LOS alarm is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable by the PCD register and can be calculated as follows: T = 16 x (N+1); with 0 ≤ N ≤ 255. The maximum time is: 256 x 16 x 488 ns = 2 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery

PCR_E	Offset	Reset Value
Pulse Count Recovery	$xx39_H$	00_H



Field	Bits	Type	Description
PCR	7:0	rw	**Pulse Count Recovery** A LOS alarm is cleared if a pulse-density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable by the PCR register and can be calculated as follows: M = N+1; with $0 \leq N \leq 255$.The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared to the contents of PCR register. If the pulse number is higher or equal to the PCR value the LOS alarm is reset otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval.

Line Interface Mode 2

LIM2_E	Offset	Reset Value
Line Interface Mode 2	$xx3A_H$	20_H

7	6	5	4	3	2	1	0
Res		**SLT1**	**SLT0**	**SCF**	**ELT**	Res	
		rw	rw	rw	rw		

Field	Bits	Type	Description
SLT1	5	rw	**Receive Slicer Threshold**
SLT0	4	rw	00_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 55% of the peak amplitude. 01_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 67% of the peak amplitude (recommended in some T1/J1 applications). 10_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 50% of the peak amplitude (default, recommended in E1 mode). 11_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 45% of the peak amplitude.
SCF	3	rw	**Select Corner Frequency of DCO-R** Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.2 Hz. See **Chapter 3.6.5**. *Note: Reducing the corner frequency of the DCO-R circuitry increases the synchronization time of the DCO-R.*
ELT	2	rw	**Enable Loop-Timed** 0_B , Normal operation 1_B , Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register XSW.XTM. For correct operation of loop timed the remote loop (bit LIM1.RL = ´0´) must be inactive and bit CMR1.DXSS must be cleared.

Loop Code Register 1

LCR1_E	Offset	Reset Value
Loop Code Register 1	$xx3B_H$	00_H

7	6	5	4	3	2	1	0
EPRM	XPRBS	LDC		LAC		FLLB	LLBP
rw	rw	rw		rw		rw	rw

Field	Bits	Type	Description
EPRM	7	rw	**Enable Pseudo-Random Binary Sequence Monitor** See **Chapter 4.7.1**. 0_B , Pseudo-Random Binary Sequence (PRBS) monitor is disabled. 1_B , PRBS is enabled. Setting this bit enables incrementing the CEC2 error counter with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR1.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit RSP.LLBAD.
XPRBS	6	rw	**Transmit Pseudo-Random Binary Sequence** A one in this bit position enables transmission of a pseudo-random binary sequence to the remote end. Depending on bit LLBP the PRBS is generated according to 2^{11} -1, 2^{15} -1, 2^{20} -1 or 2^{23} -1 with a maximum-14-zero restriction (ITU-T O. 151). See **Chapter 4.7.1**.
LDC	5:4	rw	**Length Deactivate (Down) Code** These bits defines the length of the LLB deactivate code which is programmable in register LCR2. 00_B , Length: 5 bit 01_B , Length: 6 bit, 2 bit, 3 bit 10_B , Length: 7 bit 11_B , Length: 8 bit, 2 bit, 4bit
LAC	3:2	rw	**Length Activate (Up) Code** These bits defines the length of the LLB activate code which is programmable in register LCR3. 00_B , Length: 5 bit 01_B , Length: 6 bit, 2 bit, 3 bit 10_B , Length: 7 bit 11_B , Length: 8 bit, 2 bit, 4 bit
FLLB	1	rw	**Framed Line Loop-Back/Invert PRBS** Depending on bit LCR1.XPRBS this bit enables different functions: LCR1.XPRBS = ´0´: see **Table 80**. *Note: Invert PRBS LCR1.XPRBS = ´1´: see **Table 81***
LLBP	0	rw	**Line Loop-Back Pattern** See **Chapter 4.5.6** LCR1.XPRBS = ´0´: see **Table 82** LCR1.XPRBS = ´1´ or LCR1.EPRM = ´1´: see **Table 83** and **Table 39**

Table 80 FLLB Constant Values (Case 1)

Name and Description	Value
Framed Line Loop-Back/Invert PRBS The line loop-back code is transmitted including framing bits. LLB code overwrites the FS/DL-bits.	0_B
Framed Line Loop-Back/Invert PRBS The line loop-back code is transmitted unframed. LLB code does not overwrite the FS/DL-bits.	1_B

Table 81 FLLB Constant Values (Case 2)

Name and Description	Value
Framed Line Loop-Back/Invert PRBS The generated PRBS is transmitted not inverted.	0_B
Framed Line Loop-Back/Invert PRBS The PRBS is transmitted inverted.	1_B

Table 82 LLBP Constant Values (Case 1)

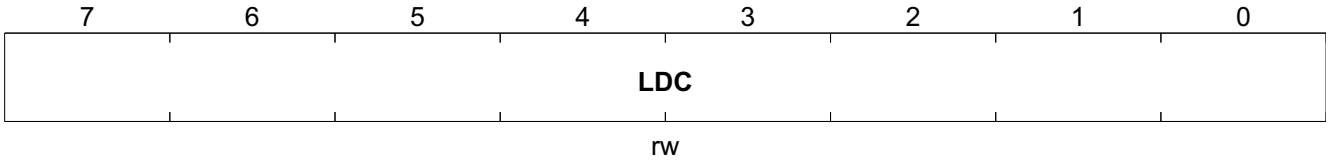
Name and Description	Value
Line Loop-Back Pattern Fixed line loop-back code according to ANSI T1. 403.	0_B
Line Loop-Back Pattern Enable user-programmable line loop-back code by register LCR2/3.	1_B

Table 83 LLBP Constant Values (Case 2)

Name and Description	Value
Line Loop-Back Pattern 2^{15} -1	0_B
Line Loop-Back Pattern 2^{20} -1	1_B

Loop Code Register 2

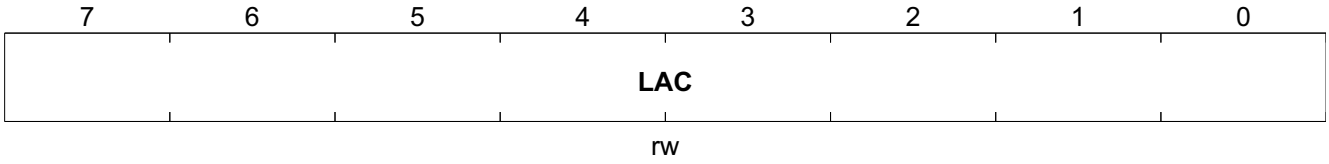
LCR2_E	Offset	Reset Value
Loop Code Register 2	$xx3C_H$	00_H



Field	Bits	Type	Description
LDC	7:0	rw	**Line Loop-Back Deactivate Code** If enabled by bit FMR3.XLD = ´1´ the LLB deactivate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared. If LCR2 is changed while the previous deactivate code has been detected and is still received, bit RSP.LLBDD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´).

Loop Code Register 3

LCR3_E	Offset	Reset Value
Loop Code Register 3	$3D_H$	00_H



Field	Bits	Type	Description
LAC	7:0	rw	**Line Loop-Back Activate Code** If enabled by bit FMR3.XLU = ´1´ the LLB activate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.If LCR3 is changed while the previous activate code has been detected and is still received, bit RSP.LLBAD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´).

System Interface Control 1

See **Chapter 4.6**.

SIC1_E	Offset	Reset Value
System Interface Control 1	$xx3E_H$	00_H

7	6	5	4	3	2	1	0
SSC1	SSD1	RBS		SSC0	BIM	XBS	
rw	rw	rw		rw	rw	rw	

Field	Bits	Type	Description
SSC1	7	rw	**Select System Clock** SIC1.SSC1 and SIC1.SSC0 define the clocking rate on the system interface, see **Chapter 4.6**., **Table 36** 00_B , 2.048 MHz 01_B , 4.096 MHz 10_B , 8.192 MHz 11_B , 16.384 MHz
SSD1	6	rw	**Select System Data Rate 1** SIC1.SSD1 and FMR1.SSD0 define the data rate on the system interface. 00_B , 2.048 Mbit/s 01_B , 4.096 Mbit/s 10_B , 8.192 Mbit/s 11_B , 16.384 Mbit/s
RBS	5:4	rw	**Receive Buffer Size** See **Chapter 4.1.7**. 00_B , Buffer size: 2 frames 01_B , Buffer size: 1 frame 10_B , Buffer size: 96 bits 11_B , bypass of receive elastic store
SSC0	3	rw	**Select System Clock** SIC1.SSC1 and SIC1.SSC0 define the clocking rate on the system highway. See **Chapter 4.6**, **Table 36** 00_B , 2.048 MHz 01_B , 4.096 MHz 10_B , 8.192 MHz 11_B , 16.384 MHz
BIM	2	rw	**Bit Interleaved Mode** 0_B , Byte interleaved mode 1_B , Bit interleaved mode

Field	Bits	Type	Description
XBS	1:0	rw	**Transmit Buffer Size** See **Chapter 4.2.1**. 00_B , Bypass of transmit elastic store 01_B , Buffer size: 1 frame 10_B , Buffer size: 2 frames 11_B , Buffer size: 96 bits

System Interface Control 2

SIC2_E	Offset	Reset Value
System Interface Control 2	$xx3F_H$	00_H

7	6	5	4	3	2	1	0
FFS	**SSF**	**CRB**	Res	**SICS**			Res
rw	rw	rw		rw			

Field	Bits	Type	Description
FFS	7	rw	**Force Freeze Signaling** Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is started again. The freeze signaling status can also be automatically generated by detecting the loss-of-signal alarm or a loss of CAS frame alignment or a receive slip (only if external register access on pin RSIG is enabled). This automatic freeze signaling function is logically ored with this bit.The current internal freeze signaling status is output on pin RPA to RPC using pin function FREEZE which is selected by PC(3:1).RPC(3:0) = ´0110_b´. Additionally, this status is also available in register SIS.SFS.
SSF	6	rw	**Serial Signaling Format** Only applicable if pin function RSIG/XSIG and SIC3.TTRF = ´0´ is selected. 0_B , Bits 1 to 4 in all time slots except time slots 0 and16 are cleared. 1_B , Bits 1 to 4 in all time slots except time slots 0 and16 are set high.
CRB	5	rw	**Center Receive Elastic Buffer** Only applicable if the time slot assigner is disabled (PC(3:1).RPC(3:0) = ´0001_b´), no external or internal synchronous pulse receive is generated. A transition from low to high forces a receive slip and the read- pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 2.048 MHz periods before it is cleared.

Field	Bits	Type	Description
SICS	3:1	rw	**System Interface Channel Select** Only applicable if the system clock rate is greater than 2.048 MHz.Received data is transmitted on pin RDO/RSIG or received on XDI/XSIG with the selected system data rate. If the data rate is greater than 2.048 Mbit/s the data is output or sampled in half, a quarter or one eighth of the time slot. Data is not repeated. The time while data is active during a 8 x 488 ns time slot is called a channel phase. RDO/RSIG are cleared (driven to low level) while XDI/XSIG are ignored for the remaining time of the 8 x 488 ns or for the remaining channel phases. The channel phases are selectable with these bits. See **Chapter 4.6**. 000_B , Data active in channel phase 1, valid if system data rate is 16⁄8⁄4 Mbit/s 001_B , Data active in channel phase 2, valid if system data rate is 16⁄8⁄4 Mbit/s 010_B , Data active in channel phase 3, valid if data rate is 16/8 Mbit/s 011_B , Data active in channel phase 4, valid if data rate is 16/8 Mbit/s 100_B , Data active in channel phase 5, valid if data rate is 16 Mbit/s 101_B , Data active in channel phase 6, valid if data rate is 16 Mbit/s 110_B , Data active in channel phase 7, valid if data rate is 16 Mbit/s 111_B , Data active in channel phase 8, valid if data rate is 16 Mbit/s

System Interface Control 3

SIC3_E	Offset	Reset Value
System Interface Control 3	$xx40_H$	00_H

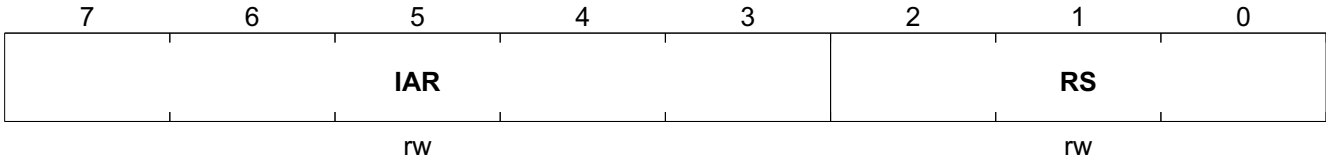
7	6	5	4	3	2	1	0
CASMF	RRTRI	RTRI	FSCT	RESX	RESR	TTRF	DAF
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CASMF	7	rw	**CAS Multiframe Begin Marker** 0_B , The time slot 0 multiframe begin is asserted on pin RP(A to C)/pin function RMFB. 1_B , The time slot 16 CAS multiframe begin is asserted on pin RP(A to C)/pin function RMFB.
RRTRI	6	rw	**RSIG/RDO Tri-state Mode** See **Chapter 3.6.7** *Note: RRTRI is logically exored with RTDMT multi function port, if this function is selected. RTDMT exor RRTRI sets additionally RFM and SCLKR into tristate, see**Table 19**.* 00_B , normal operation (RSIG and RDO are switched to low level during inactive channel/bit phases). 01_B , RSIG and RDO are switched into tristate mode during inactive channel/bit phases. 10_B , RSIG and RDO are tristate constantly (and also RFM and SCLKR). 11_B , RSIG and RDO are tristate constantly (and also RFM and SCLKR).
RTRI	5		
FSCT	4	rw	**FSC Tristate Mode** *Note: If SEC/FSC is selected as SEC input, this bit is ignored.* 0_B , normal operation of SEC/FSC pin. 1_B , SEC/FSC is switched into tristate mode.

Field	Bits	Type	Description
RESX	3	rw	**Rising Edge Synchronous Pulse Transmit** Depending on this bit all transmit system interface data and marker are clocked (outputs) or sampled (inputs) with the selected active edge. See **Chapter 4.6** and also **SIC4_E**. Only valid if CMR2.IXSC = ´0´: *Note: CMR2.IXSC = ´1´: value of RESX bit has no impact on the selected edge of the system interface clock but value of RESR bit is used as RESX. Example: If RESR = ´0´, the rising edge of system interface clock is the selected one for sampling data on XDI and vice versa.* 0_B , Clocked or sampled with the first falling edge of the selected system interface clock. 1_B , Clocked or sampled the first rising edge of the selected system interface clock.
RESR	2	rw	**Rising Edge Synchronous Pulse Receive** Depending on this bit all receive system interface data and marker are clocked (outputs) or sampled (inputs) with the selected active edge. See **Chapter 4.6** and also **SIC4_E**. *Note: If bit CMR2.IRSP is set, the behavior of signal RFM (if used) is inverse (´1´ = falling edge, ´0´ = rising edge)* 0_B , Clocked or sampled with the first falling edge of the selected system interface clock. 1_B , Clocked or sampled with the first rising edge of the selected system interface clock.
TTRF	1	rw	**TTR Register Function (Fractional E1 Access)** Setting this bit the function of the TTR(4:1) registers is changed. A one in each TTR register forces the XSIGM marker high for the corresponding time slot and controls sampling of the time slots provided on pin XSIG. XSIG is selected by PC(2:1).XPC(3:0).
DAF	0	rw	**Disable Automatic Freeze** 0_B , Signaling is automatically frozen if one of the following alarms occurred: Loss-Of-Signal (FRS0.LOS), Loss of CAS Frame Alignment (FRS1.TS16LFA), or receive slips (ISR3.RSP/N). 1_B , Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set. Significant only if the serial signaling access is enabled.

Clock Mode Register 4

CMR4_E	Offset	Reset Value
Clock Mode Register 4	$xx41_H$	00_H

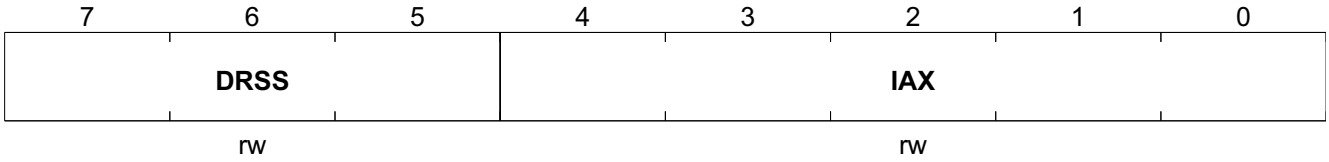


Field	Bits	Type	Description
IAR	7:3	rw	**Integral parameter selection (Corner frequency and attenuation selection) for the DCO-R** Only valid if CMR6.DCOCOMPN = ´1´and CMR2.ECFAR = ´1´, see Chapter 3.6.5 and Table 15.
RS	2:0	rw	**Receive Clock (RCLK) Frequency Selection** See also Chapter 3.6 *Note: Only valid for COMP = ´0´. In QuadFALC® compatibility mode (COMP = ´1´) these bits are ignored (see CMR1.RS). RS_2 to RS_5 are dejittered clocks sourced by DCO-R.* 000_B , clock recovered from the line through the DPLL drives RCLK. 001_B , clock recovered from the line through the DPLL drives RCLK. Ored with the incoming LOS signal. 010_B , 2.048 MHz, dejitered, sourced by DCO-R. 011_B , 4.096 MHz, dejitered, sourced by DCO-R. 100_B , 8.192 MHz, dejitered, sourced by DCO-R. 101_B , 16.384 MHz, dejitered, sourced by DCO-R. 110_B , 2.048 MHz ored with LOS. 111_B , 16.384 MHz ored with LOS.

Clock Mode Register 5

Note: The reset value depends on the channel, so that for the DCO-R the current channel is selected by the bits DRSS (for example for channel 3 the reset value is ´40´$_H$).

CMR5_E	Offset	Reset Value
Clock Mode Register 5	$xx42_H$	00_H



Field	Bits	Type	Description
DRSS	7:5	rw	**DCO-R Channel Selection** See **Chapter 3.6** *Note: Only valid for COMP = ´0´. In QuadFALC® compatibility mode (COMP = ´1´) these bits are ignored and CMR1.DRSS are used.* 000_B , receive reference clock generated by the DPLL of channel 1. 001_B , receive reference clock generated by the DPLL of channel 2. 010_B , receive reference clock generated by the DPLL of channel 3. 011_B , receive reference clock generated by the DPLL of channel 4. 100_B , receive reference clock generated by the DPLL of channel 5. 101_B , receive reference clock generated by the DPLL of channel 6. 110_B , receive reference clock generated by the DPLL of channel 7. 111_B , receive reference clock generated by the DPLL of channel 8.
IAX	4:0	rw	**Integral parameter selection (Corner frequency and attenuation selection) for the DCO-X** Only valid if CMR6.DCOCOMPN = ´1´and CMR2.ECFAX = ´1´, see **Chapter 3.7.4** and **Table 15**.

Clock Mode Register 6

CMR6_E	Offset	Reset Value
Clock Mode Register 6	$xx43_H$	00_H

7	6	5	4	3	2	1	0
DCOCOMPN	SRESR	SRESX	STF			SCFX	ATCS
rw	rw	rw	rw			rw	rw

Field	Bits	Type	Description
DCOCOMPN	7	rw	**Compatibility programming of DCO-R/DCO-X disable** Only applicable if CMR2.ECFAR/ECFAX is set. See Chapter 3.6.5, Table 15. 0_B , programming of corner frequencies of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0) /CFAX(3:0), compatible to the FALC56® v2.x. Register bits CMR5.IAX(4:0)/CMR4.IAR(4:0) are not valid. 1_B , programming of corner frequencies and attenuation factors of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0)/CFAX(3:0) and CMR4.IAR(4:0)/CMR5.IAX(4:0) in the range 0.2 ... 20 Hz.
SRESR	6	rw	**Soft Reset of DCO-R** By setting this bit a soft reset of the DCO-R will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-R lock functionality, this bit must be cleared subsequently. See Chapter 3.6.5. 0_B , DCO-R enabled (normal lock functionality). 1_B , soft reset of DCO-R, no lock functionality.
SRESX	5	rw	**Soft Reset of DCO-X** By setting this bit a soft reset of the DCO-X will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-X lock functionality, this bit must be cleared subsequently. See Chapter 3.7.4. 0_B , DCO-X enabled (normal lock functionality). 1_B , soft reset of DCO-X, no lock functionality.

Field	Bits	Type	Description
STF	4:2	rw	**Transmit Clock (TCLK) Frequency Selection** See **Chapter 3.7.2** *Note: Only valid for COMP = ´0´. In QuadFALC® compatibility mode (COMP = ´1´) these bits are ignored and CMR1.STF is used. Note that frequencies are not in ascent ordering .* 000_B , 2.048 MHz. 001_B , 8.192 MHz. 010_B , 4.096 MHz. 011_B , 16.384 MHz. 100_B , 32.768 MHz. 101_B , reserved. 110_B , reserved. 111_B , reserved.
SCFX	1	rw	**Select Corner Frequency of DCO-X** Only applicable if CMR2.EXFAX = ´0´. See **Chapter 3.6.5** and **Chapter 3.7.4**. 0_B , corner frequency of DCO-X is 2 Hz. 1_B , corner frequency of DCO-X is 0.2 Hz.
ATCS	0	rw	**Automatic Transmit Clock Switching** See **Chapter 3.7.3**. If TCLK is lost, automatically switching to SCLKX can be performed. *Note: Status bits ISR7.XCLKSS(1:0) (**ISR7_E**) show if automatic clock switching was performed. Status bits CLKSTAT.TCLKLOS and CLKSTAT.SCLKXLOS (**CLKSTAT_E**) show the current status of the input clocks TCLK and SCLKX respectively.* 0_B , automatic clock switching is disabled. 1_B , automatic clock switching is enabled.

Clock Mode Register 1

CMR1_E	Offset	Reset Value
Clock Mode Register 1	$xx44_H$	00_H

7	6	5	4	3	2	1	0
DRSS		RS		DCS	STF	DXJA	DXSS
rw		rw		rw	rw	rw	rw

Field	Bits	Type	Description
DRSS	7:6	rw	**Select RCLK Source Channel** These bits select the source channel of RCLK, see also **Chapter 3.6**. *Note: Only valid for COMP = ´1´. For COMP = ´0´) these bits are ignored and CMR5.DRSS are used.* 00_B , Receive reference clock generated by channel 1 01_B , Receive reference clock generated by channel 2. 10_B , Receive reference clock generated by channel 3. 11_B , Receive reference clock generated by channel 4.
RS	5:4	rw	**Select RCLK Source** These bits select the source of RCLK, see also **Chapter 3.6**. *Note: Only valid for COMP = ´1´. For COMP = ´0´) these bits are ignored and CMR4.RS are used.* 00_B , Clock recovered from the line through the DPLL drives RCLK 01_B , Clock recovered from the line through the DPLL drives RCLK and in case of an active LOS alarm RCLK pin is set high (ored with LOS). 10_B , Clock recovered from the line is de-jittered by DCO-R to drive a 2.048 MHz clock on RCLK. 11_B , Clock recovered from the line is de-jittered by DCO-R to drive a 8.192 MHz clock on RCLK.
DCS	3	rw	**Disable Clock-Switching** In Slave mode (LIM0.MAS = ´0´) the DCO-R is synchronized on the recovered route clock. In case of loss-of-signal LOS the DCO-R switches automatically to the clock sourced by port SYNC, see also **Table 16**. 0_B , automatic switching from RCLK to SYNC is enabled 1_B , automatic switching from RCLK to SYNC is disabled

Field	Bits	Type	Description
STF	2	rw	**Select TCLK Frequency** See **Chapter 3.7.2**. Only applicable if the pin function TCLK on multi function port XP(A,B) is selected by PC(3:1).XPC(3:0) = ´0011_b´. Data on XL1/2 (XDOP/N / XOID) are clocked with TCLK. *Note: Only valid for COMP = ´1´. For COMP = ´0´) these bit is ignored and CMR6.STF are used.* 0_B , 2.048 MHz 1_B , 8.192 MHz
DXJA	1	rw	**Disable Internal Transmit Jitter Attenuation** Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N/XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from SCLKX, independent of this bit.
DXSS	0	rw	**DCO-X Synchronization Clock Source** 0_B , The DCO-X circuitry synchronizes to the internal reference clock which is sourced by SCLKX/R or RCLK. Since there are many reference clock opportunities the following internal prioritizing in descending order from left to right is realized: LIM1.RL > CMR1.DXSS > LIM2.ELT > current working clock of transmit system interface. If one of these bits is set the corresponding reference clock is taken. 1_B , DCO-X synchronizes to an external reference clock provided on multi function port XPA or XPB pin function TCLK, if no remote loop is active. TCLK is selected by PC(2:1).XPC(3:0) = ´0011B´.

Clock Mode Register 2

CMR2_E	Offset	Reset Value
Clock Mode Register 2	$xx45_H$	00_H

7	6	5	4	3	2	1	0
ECFAX	ECFAR	DCOXC	DCF	IRSP	IRSC	IXSP	IXSC
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ECFAX	7	rw	**Enable Corner Frequency Adjustment for DCO-X** See **Chapter 3.7.4** and **Table 15**. *Note: DCO-X must be activated.* 0_B , adjustment is disabled (only 2Hz and 0.2Hz are possible). 1_B , adjustment is enabled as programmed in CMR3.CFAX(3:0) and CMR4.IAX(4:0).
ECFAR	6	rw	**Enable Corner Frequency Adjustment for DCO-R** See **Chapter 3.7.4** and **Table 15**. *Note: DCO-R must be activated.* 0_B , adjustment is disabled (only 2Hz and 0.2Hz are possible). 1_B , adjustment is enabled as programmed in CMR3.CFAR(3:0) and CMR5.IAR(4:0).
DCOXC	5	rw	**DCO-X Center-Frequency Enable** See **Chapter 3.6.5** 0_B , The center function of the DCO-X circuitry is disabled. 1_B , The center function of the DCO-X circuitry is enabled. DCO-X centers to 2.048 MHz related to the master clock reference (MCLK), if reference clock (e.g. SCLKX) is missing.
DCF	4	rw	**DCO-R Center- Frequency Disabled** See also **Table 16**. 0_B , The DCO-R circuitry is frequency centered in master mode if no 2.048 MHz reference clock on pin SYNC is provided or in slave mode if a loss-of-signal occurs in combination with no 2.048 MHz clock on pin SYNC or a gapped clock is provided on pin RCLKI and this clock is inactive or stopped. 1_B , The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available on pin SYNC or pin RCLKI. The DCO-R circuitry starts synchronization as soon as a clock appears on pins SYNC or RCLKI.

Field	Bits	Type	Description
IRSP	3	rw	**Internal Receive System Frame Sync Pulse** 0_B , The frame sync pulse for the receive system interface is sourced by $\overline{SYPR}$ (if $\overline{SYPR}$ is applied). If $\overline{SYPR}$ is not applied, the frame sync pulse is derived from RDO output signal internally free running). *Note: The use of IRSP = ´0´ is recommended.* 1_B , The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry. This internally generated frame sync signal can be output (active low) on multifunction ports RP(A to C) (RPC(3:0) = ´0001H´). *Note: This is the only exception where the use of RFM and $\overline{SYPR}$ is allowed at the same time. Because only one set of offset registers (RC1/0) is available, programming is done by using the $\overline{SYPR}$ calculation formula in the same way as for the external $\overline{SYPR}$ pulse. Bit IRSC must be set for correct operation.*
IRSC	2	rw	**Internal Receive System Clock** See also **Figure 45**. 0_B , The working clock for the receive system interface is sourced by SCLKR or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK. 1_B , The working clock for the receive system interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock. SCLKR is ignored.
IXSP	1	rw	**Internal Transmit System Frame Sync Pulse** 0_B , The frame sync pulse for the transmit system interface is sourced by $\overline{SYPX}$. 1_B , The frame sync pulse for the transmit system interface is internally sourced by the DCO-R circuitry. Additionally, the external XMFS signal defines the transmit multiframe begin. XMFS is enabled or disabled by the multifunction port configuration. For correct operation bits CMR2.IXSC/IRSC must be set. $\overline{SYPX}$ is ignored.
IXSC	0	rw	**Internal Transmit System Clock** See also **Figure 45**. 0_B , The working clock for the transmit system interface is sourced by SCLKX. 1_B , The working clock for the transmit system interface is sourced internally by the working clock of the receive system interface. SCLKX is ignored.

Global Configuration Register

GCR_E	Offset	Reset Value
Global Configuration Register	0046_H	00_H

7	6	5	4	3	2	1	0
VIS	SCI	SES	ECMC	Res			PD
rw	rw	rw	rw				rw

Field	Bits	Type	Description
VIS	7	rw	**Masked Interrupts Visible** See also **Chapter 3.4.4** 0_B , Masked interrupt status bits are not visible in registers ISR(7:0). 1_B , Masked interrupt status bits are visible in ISR(7:0), but they are not visible in register GIS.
SCI	6	rw	**Status Change Interrupt** 0_B , Interrupts are generated either on activation or deactivation of the internal interrupt source. 1_B , The following interrupts are activated both on activation and deactivation of the internal interrupt source: ISR2.LOS, ISR2.AIS, ISR3.LMFA16.
SES	5	rw	**Select External Second Timer** 0_B , Internal second timer selected 1_B , External second timer selected
ECMC	4	rw	**Error Counter Mode COFA** 0_B , The Sa6-bit error indications are accumulated in the error counter CEC3L/H. 1_B , A Change of Frame or Multiframe Alignment COFA is detected since the last resynchronization. The events are accumulated in the error counter CEC3L.(1:0). Multiframe periods received in the asynchronous state are accumulated in the error counter CEC3L.7-2. An overflow of each counter is disabled.
PD	0	rw	**Power Down** Switches between power-up and power-down mode. After switching from power down to power up a receiver reset should be made by setting of CMDR.RRES. 0_B , Power up 1_B , Power down: All outputs are driven inactive; multifunction ports are driven high by the weak internal pullup device.

Errored Second Mask

This register functions as an additional mask register for the interrupt status bit Errored Second (ISR3.ES). A "1" in a bit position of ESM deactivates the related second interrupt.

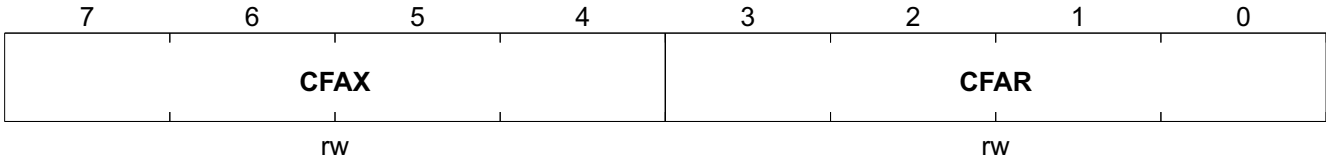
ESM_E	Offset	Reset Value
Errored Second Mask	$xx47_H$	FF_H

7	6	5	4	3	2	1	0
LFA	**FER**	**CER**	**AIS**	**LOS**	**CVE**	**SLIP**	**EBE**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
LFA	7	rw	**Errored Second Mask LFA**
FER	6	rw	**Errored Second Mask FER**
CER	5	rw	**Errored Second Mask CER**
AIS	4	rw	**Errored Second Mask AIS**
LOS	3	rw	**Errored Second Mask LOS**
CVE	2	rw	**Errored Second Mask CVE**
SLIP	1	rw	**Errored Second Mask SLIP**
EBE	0	rw	**Errored Second Mask EBE**

Clock Mode Register 3

CMR3_E	Offset	Reset Value
Clock Mode Register 3	$xx48_H$	00_H



Field	Bits	Type	Description
CFAX	7:4	rw	**Corner Frequency Adjustment for DCO-X** See **Chapter 3.7.4** and **Table 15**. *Note: DCO-X must be activated and CMR2.ECFAX must be set (adjustment must be enabled).*
CFAR	3:0	rw	**Corner Frequency Adjustment for DCO-R** See **Chapter 3.6.5** and **Table 15**. *Note: DCO-R must be activated and CMR2.ECFAR must be set (adjustment must be enabled).*

Disable Error Counter

Note: Error counters and receive buffer delay can be read 1 µs after setting the according bit in bit DEC.

DEC_E	Offset	Reset Value
Disable Error Counter	**xx60$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
DRBD	Res	**DCEC3**	**DCEC2**	**DCEC1**	**DEBC**	**DCVC**	**DFEC**
w		w	w	w	w	w	w

Field	Bits	Type	Description
DRBD	7	w	**Disable Receive Buffer Delay** This bit has to be set before reading the register RBD. It is reset automatically if RBD has been read.
DCEC3	5	w	**Disable CRC Error Counter 3**
DCEC2	4	w	**Disable CRC Error Counter 2**
DCEC1	3	w	**Disable CRC Error Counter 1**
DEBC	2	w	**Disable Errored Block Counter**
DCVC	1	w	**Disable Code Violation Counter**
DFEC	0	w	**Disable Framing Error Counter** These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They are reset automatically if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Transmit CAS Register 1

The transmit CAS register access is enabled by setting bit XSP.CASEN = ´1´. Each register except XS1 contains the CAS bits for two time slots, see **Chapter 4.3.5.4**. With the transmit multiframe begin ISR1.XMB the contents of these registers is copied into a shadow register. The contents is sent out subsequently in the time slots 16 of the outgoing data stream. XS1.7 is sent out first and XS16.0 is sent last. The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, current contents is repeated. XS1 has to be programmed with the multiframe pattern. This pattern should always stay low otherwise the remote end loses its synchronization. With setting the Y-bit a remote alarm is transmitted to the far end. The X bits (spare bits) should be set if they are not used. If access to these registers is done without control of the interrupt ISR1.XMB the registers should be written twice to avoid an internal data transfer error.

Note: If ISR1.XMB is not used and the write access to these registers is done exact in the moment when this interrupt is generated, data is lost.

3. A software reset (CMDR.XRES) resets these registers.

XS1_E	**Offset**	**Reset Value**
Transmit CAS Register 1	**xx70$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
0				**X1**	**Y1**	**X2**	**Y2**
w				w	w	w	w

Field	Bits	Type	Description
0	7:4	w	**Fixed ´0´**
X1	3	w	**X1**
Y1	2	w	**Y1**
X2	1	w	**X2**
Y2	0	w	**Y2**

Transmit CAS Register 2

For description see **Transmit CAS Register 1**

XS2_E	Offset	Reset Value
Transmit CAS Register 2	**xx71$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
A1	**B1**	**C1**	**D1**	**A16**	**B16**	**C16**	**D16**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
A1	7	w	**A1**
B1	6	w	**B1**
C1	5	w	**C1**
D1	4	w	**D1**
A16	3	w	**A16**
B16	2	w	**B16**
C16	1	w	**C16**
D16	0	w	**D16**

Similar Registers

Registers XS3 to XS16 have the same layout and description as XS2.

The Offset Addresses are listed in **XSn Overview**, for bit names refer to **Transmit CAS Registers**

Table 84 XSn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
XS3	Transmit CAS Register 3	72$_H$	
XS4	Transmit CAS Register 4	73$_H$	
XS5	Transmit CAS Register 5	74$_H$	
XS6	Transmit CAS Register 6	75$_H$	
XS7	Transmit CAS Register 7	76$_H$	
XS8	Transmit CAS Register 8	77$_H$	
XS9	Transmit CAS Register 9	78$_H$	
XS10	Transmit CAS Register 10	79$_H$	
XS11	Transmit CAS Register 11	7A$_H$	
XS12	Transmit CAS Register 12	7B$_H$	
XS13	Transmit CAS Register 13	7C$_H$	
XS14	Transmit CAS Register 14	7D$_H$	
XS15	Transmit CAS Register 15	7E$_H$	
XS16	Transmit CAS Register 16	7F$_H$	

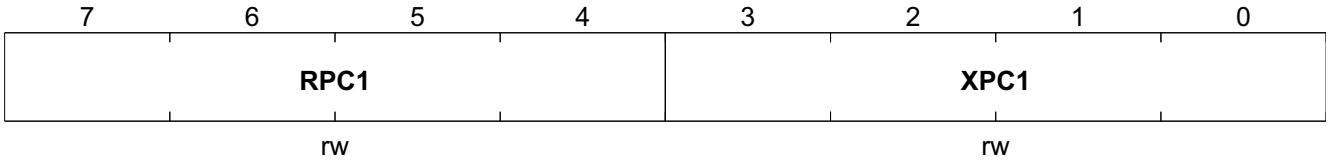
Table 85 Transmit CAS Registers

	7	6	5	4	3	2	1	0
XS1	0	0	0	0	X1	Y1	X2	Y2
XS2	A1	B1	C1	D1	A16	B16	C16	D16
XS3	A2	B2	C2	D2	A17	B17	C17	D17
XS4	A3	B3	C3	D3	A18	B18	C18	D18
XS5	A4	B4	C4	D4	A19	B19	C19	D19
XS6	A5	B5	C5	D5	A20	B20	C20	D20
XS7	A6	B6	C6	D6	A21	B21	C21	D21
XS8	A7	B7	C7	D7	A22	B22	C22	D22
XS9	A8	B8	C8	D8	A23	B23	C23	D23
XS10	A9	B9	C9	D9	A24	B24	C24	D24
XS11	A10	B10	C10	D10	A25	B25	C25	D25
XS12	A11	B11	C11	D11	A26	B26	C26	D26
XS13	A12	B12	C12	D12	A27	B27	C27	D27
XS14	A13	B13	C13	D13	A28	B28	C28	D28
XS15	A14	B14	C14	D14	A29	B29	C29	D29
XS16	A15	B15	C15	D15	A30	B30	C30	D30

Port Configuration 1

See **Chapter 3.8**. The unavailable multi function ports must be configured to an allowed value. It is suggested to configure them to an uncritical output signal, for example PC3 = ´x5$_H$´, PC4 = ´35$_H$´.

PC1_E	Offset	Reset Value
Port Configuration 1	xx80$_H$	00$_H$



Field	Bits	Type	Description
RPC1	7:4	rw	**Receive multifunction Port Configuration** See **Chapter 3.8**. The multifunction ports RP(A to C) are bidirectional. After Reset the ports RPA and RPB are configured as SYPR., the port RPC is configured as RCLK output. With the selection of the pin function the In/Output configuration is also achieved. The input function $\overline{\text{SYPR}}$ may only be selected once, it must not be selected twice or more. Register PC1 configures port RPA, while PC2 → port RPB and PC3 → port RPC. See **RPC1 Constant Values**
XPC1	3:0	rw	**Transmit multifunction Port Configuration** The multifunction ports XP(A to B) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the four different input functions ($\overline{\text{SYPX}}$, XMFS, XSIG, TCLK, XLT and $\overline{\text{XLT}}$) may only be selected once. No input function must be selected twice or more. $\overline{\text{SYPX}}$ and XMFS should not be selected in parallel. Register PC1 configures port XPA and PC2 the port XPB. See **XPC1 Constant Values**

Table 86 RPC1 Constant Values

Name and Description	Value
SYPR Synchronous Pulse Receive (Input, low active) Together with register RC(1:0) $\overline{\text{SYPR}}$ defines the frame begin on the receive system interface. Because of the offset programming the $\overline{\text{SYPR}}$ and the RFM pin function cannot be selected in parallel.	0000$_B$
RFM: Receive Frame Marker (Output) CMR2.IRSP = ´0´: The receive frame marker is active high for one 2.048 MHz period during any bit position of the current frame. Programming of the bit position is done by using registers RC(1:0). The internal time slot assigner is disabled. The RFM offset calculation formula has to be used. CMR2.IRSP = ´1´: Internally generated frame synchronization pulse sourced by the DCO-R circuitry. The pulse is active low for one 2.048 MHz period.	0001$_B$

Table 86 RPC1 Constant Values (cont'd)

Name and Description	Value
RMFB: Receive Multiframe Begin (Output) Marks the beginning of every received multiframe or optionally the begin of every CAS multiframe begin (active high).	0010_B
RSIGM: Receive Signaling Marker (Output) Marks the time slots which are defined by register RTR(4:1) of every frame on port RDO.	0011_B
RSIG: Receive Signaling Data (Output) The received CAS multiframe is transmitted on this pin. Time slot on RSIG correlates directly to the time slot assignment on RDO.	0100_B
DLR: Data Link Bit Receive (Output) Marks the Sa-bits within the data stream on RDO.	0101_B
FREEZE: Freeze Signaling (Output) The freeze signaling status is active high by detecting a loss-of-signal alarm, or a loss of CAS frame alignment or a receive slip (positive or negative). It stays high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.	0110_B
RFSP: Receive Frame Synchronous Pulse (Output, low active) RFSP marks the frame begin in the receivers synchronous state. This marker is active low for 488 ns with a frequency of 8 kHz.	0111_B
RLT: Receive line termination (input) "Hardware" switching of receive line termination, see **Chapter 3.6.7**	1000_B
GPI: general purpose input Value of this input is stored in register MFPI.	1001_B
GPOH: General purpose output, high level Pin is set fixed to high level	1010_B
GPOL: General purpose output, low level Pin is set fixed to low level	1011_B
LOS: Loss of signal Loss of signal indication output	1100_B
RTDMT: Receive TDM tristate (input) receive TDM i/f tristate (RDO, RSIG, SCLKR, RFM).	1101_B
reserved	1110_B
RCLK: RCLK output	1111_B

Table 87 XPC1 Constant Values

Name and Description	Value
SYPX: Synchronous Pulse Transmit (Input, low active) Together with register XC(1:0) SYPX defines the frame begin on the transmit system interface ports XDI and XSIG.	0000_B
XMFS: Transmit Multiframe Synchronization (Input) Together with register XC(1:0) XMFS defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low.	0001_B
XSIG: Transmit Signaling Data (Input) Input for transmit signaling data received from the signaling highway. Optionally sampling of XSIG data is controlled by the active high XSIGM marker.	0010_B

Table 87 XPC1 Constant Values (cont'd)

Name and Description	Value
TCLK: Transmit Clock (Input) A 2.048/8.192 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) is not used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 MHz.	0011_B
XMFB: Transmit Multiframe Begin (Output) Marks the beginning of every transmit multiframe.	0100_B
XSIGM: Transmit Signaling Marker (Output) Marks the time slots which are defined by register TTR(4:1) of every frame on port XDI.	0101_B
DLX: Data Link Bit Transmit (Output) Marks the Sa-bits within the data stream on XDI.	0110_B
XCLK: Transmit Line Clock (Output) Frequency: 2.048 MHz	0111_B
XLT: Transmit Line Tristate control input, high active With a high level on this port the transmit lines XL1/2 or XDOP/N are set directly into tristate. This pin function is logically ored with register XPM2.XLT. See **Chapter 3.6.7** and **Chapter 3.7.1**	1000_B
GPI: General Purpose Input, low level Value of this input is stored in register MFPI.	1001_B
GPOH: General Purpose Output, high level Pin is set fixed to high level	1010_B
GPOL: General Purpose Output, low level Pin is set fixed to low level	1011_B
reserved	1100_B
reserved	1101_B
XLT: Transmit Line Tristate control input, low active see XLT	1110_B
reserved	1111_B

Registers PC2 to PC3 have the same layout and description, but the 4 LSBs of PC3 are not used because only 2 MFPs in transmit direction exists.

The register PC4 and the bits (3:0) of the register PC3 can be written and read, but are not valid. These bits are dummys for software compatibility to the QuadFALC.

Only one of the ports RPA, RPB or RPC must be configured as RTDMT.

Only one of the ports XPA or XPB must be configured as XLT or $\overline{\text{XLT}}$.

The registers PC1, PC2 and PC4 have the reset values ´00H´, PC3 has the reset value ´F0H´.

The Offset Addresses are listed in **PCn Overview**, for bit names refer to **Port Configuration Registers**.

Table 88 PCn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
PC2	Port Configuration Register 2	81_H	
PC3	Port Configuration Register 3	82_H	
PC4	Port Configuration Register 4	83_H	

Table 89 Port Configuration Registers

	7	6	5	4	3	2	1	0
PC1	RPC13	RPC12	RPC11	RPC10	XPC13	XPC12	XPC11	XPC10
PC2	RPC23	RPC22	RPC21	RPC20	XPC23	XPC22	XPC21	XPC20
PC3	RPC33	RPC32	RPC31	RPC30	XPC33	XPC32	XPC31	XPC30
PC4	RPC43	RPC42	RPC41	RPC40	XPC43	XPC42	XPC41	XPC40

Port Configuration 5

PC5_E	Offset	Reset Value
Port Configuration 5	$xx84_H$	00_H

7	6	5	4	3	2	1	0
PHDSX	**PHDSR**	Res		**CXMFS**	**0**	**CSRP**	**CRP**
rw	rw			rw	rw	rw	rw

Field	Bits	Type	Description
PHDSX	7	rw	**Phase Decoder Switch for DCO-X** See **Chapter 3.7.4** and formulas in **GCM6_E**. 0_B , switch phase decoder by 1/3 1_B , switch phase decoder by 1/6
PHDSR	6	rw	**Phase Decoder Switch for DCO-R** See **Chapter 3.6.5** and formulas in **GCM6_E**. 0_B , switch phase decoder by 1/3 1_B , switch phase decoder by 1/6
CXMFS	3	rw	**Configure XMFS Port** 0_B , Port XMFS is active low. 1_B , Port XMFS is active high.
0	2	rw	**Fixed 0**
CSRP	1	rw	**Configure SCLKR Port** 0_B , SCLKR: Input 1_B , SCLKR: Output
CRP	0	rw	**Configure RCLK Port** 0_B , RCLK: Input 1_B , RCLK: Output

Global Port Configuration 1

GPC1_E	Offset	Reset Value
Global Port Configuration 1	0085_H	00_H

7	6	5	4	3	2	1	0
SMM	**CSFP**		Res	**FSS1**		**R1S**	
rw	rw			rw		rw	

Field	Bits	Type	Description
SMM	7	rw	**System Interface Multiplex Mode** Setting of these bit enables 4:1 or 8:1 multiplexing of E1 frames into one or two data streams, dependent on GPC6.SSI16, see **Chapter 4.6** or **Chapter 5.6**. Refer to **Table 37**. 0_B , System multiplex mode disabled 1_B , System multiplex mode enabled
CSFP	6:5	rw	**Configure SEC/FSC Port** The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = ´1´ or CMR1.RS(1:0) = ´10_b´ or ´11_b´), see **Chapter 4.5.5** 00_B , SEC: Input, active high 01_B , SEC: Output, active high 10_B , FSC: Output, active high 11_B , FSC: Output, active low
FSS1	3:2	rw	**SEC/FSC Source** One of four internally generated dejittered 8 kHz clocks FSC or second timers SEC (switching between FSC and SEC depends on GPC1.CSFP) are output on pin SEC/FSC, see **Figure 44**. Switching between FSC and SEC is done by GPC1.CSFP. *Note: Only valid for COMP = ´1´. For COMP = ´0´) these bits are ignored and GPC2.FSS are used.* 00_B , FSC or SEC respectively, sourced by channel 1 01_B , FSC or SEC respectively, sourced by channel 2 10_B , FSC or SEC respectively, sourced by channel 3 11_B , FSC or SEC respectively, sourced by channel 4

Field	Bits	Type	Description
R1S	1:0	rw	**RCLK1 Source** One of the four internally generated receive route clocks is output on pin RCLK1. Ouputs RCLK(4:2) are valid independent of these bits. See **Chapter 3.6**. *Note: Only valid for COMP = ´1´. For COMP = ´0)´ these bits are ignored and GPC2.R1S are used.* 00_B , RCLK1 sourced by channel 1 01_B , RCLK1 sourced by channel 2 10_B , RCLK1 sourced by channel 3 11_B , RCLK1 sourced by channel 4

Port Configuration 6

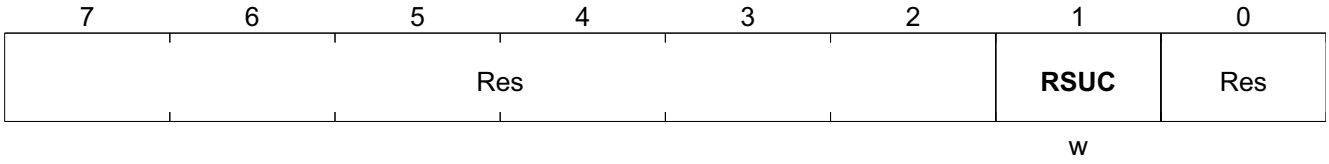
PC6_E	Offset	Reset Value
Port Configuration 6	$xx86_H$	00_H

7	6	5	4	3	2	1	0
Res	**TSRE**	Res					
	rw						

Field	Bits	Type	Description
TSRE	6	rw	**Transmit serial resistor enable** *Note: See **Table 22** for more details* 0_B , Internal serial resistors are disabled. 1_B , Internal serial resistors are enabled.

Command Register 2

CMDR2_E	Offset	Reset Value
Command Register 2	$xx87_H$	00_H



Field	Bits	Type	Description
RSUC	1	w	**Reset Signaling Unit Counter - HDLC Channel 1** *Note: The maximum time between writing to the CMDR2 register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the external micro controller operates with a very high clock rate in comparison with the OctalFALCTM's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.* 0_B , no reset of the SS7 signaling unit counter and error counter is done (no action is done) 1_B , After setting this bit the SS7 signaling unit counter and error counter are reset.The bit is cleared automatically after execution

Command Register 3

CMDR3_E	Offset	Reset Value
Command Register 3	$xx88_H$	00_H

7	6	5	4	3	2	1	0
RMC2	Res	**XREP2**	Res	**XHF2**	**XTF2**	**XME2**	**SRES2**
w		w		w	w	w	w

Field	Bits	Type	Description
RMC2	7	w	**Receive Message Complete - HDLC Channel 2** Confirmation from external micro controller to OctalFALCTM that the current frame or data block has been fetched following an RPF2 or RME2 interrupt, thus the occupied space in the RFIFO2 can be released.
XREP2	5	w	**Transmission Repeat - HDLC Channel 2** If XREP2 is set together with XTF2 (write 24H to CMDR3), the OctalFALCTM repeatedly transmits the contents of the XFIFO2 (1 up to 64bytes) without HDLC framing fully transparently, i.e. without flag, CRC.The cyclic transmission is stopped with an SRES2 command or by resetting XREP2.
XHF2	3	w	**Transmit HDLC Frame - HDLC Channel 2** After having written up to 64bytes to the XFIFO2, this command initiates the transmission of a HDLC frame.
XTF2	2	w	**Transmit Transparent Frame - HDLC Channel 2** Initiates the transmission of a transparent frame without HDLC framing.
XME2	1	w	**Transmit Message End - HDLC Channel 2** Indicates that the data block written last to the XFIFO2 completes the current frame. The OctalFALCTM can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.
SRES2	0	w	**Signaling Transmitter Reset - HDLC Channel 2** The transmitter of the signaling controller is reset. XFIFO2 is cleared of any data and an abort sequence (seven ´1´s) followed by interframe time fill is transmitted. In response to SRES2 an XPR2 interrupt is generated. This command can be used by the external micro controller to abort a frame currently in transmission.

Command Register 4

CMDR4_E	Offset	Reset Value
Command Register 4	$xx89_H$	00_H

7	6	5	4	3	2	1	0
RMC3	Res	**XREP3**	Res	**XHF3**	**XTF3**	**XME3**	**SRES3**
w		w		w	w	w	w

Field	Bits	Type	Description
RMC3	7	w	**Receive Message Complete - HDLC Channel 3** Confirmation from external micro controller to OctalFALCTM that the current frame or data block has been fetched following an RPF3 or RME3 interrupt, thus the occupied space in the RFIFO3 can be released.
XREP3	5	w	**Transmission Repeat - HDLC Channel 3** If XREP3 is set together with XTF3 (write ´24_H´ to CMDR4), the OctalFALCTM repeatedly transmits the contents of the XFIFO3 (1 up to 64 bytes) without HDLC framing fully transparently, i.e. without flag, CRC.The cyclic transmission is stopped with an SRES3 command or by resetting XREP3.
XHF3	3	w	**Transmit HDLC Frame - HDLC Channel 3** After having written up to 64 bytes to the XFIFO3, this command initiates the transmission of a HDLC frame.
XTF3	2	w	**Transmit Transparent Frame - HDLC Channel 3** Initiates the transmission of a transparent frame without HDLC framing.
XME3	1	w	**Transmit Message End - HDLC Channel 3** Indicates that the data block written last to the XFIFO3 completes the current frame. The OctalFALCTM can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.
SRES3	0	w	**Signaling Transmitter Reset - HDLC Channel 3** The transmitter of the signaling controller is reset. XFIFO3 is cleared of any data and an abort sequence (seven ´1´s) followed by interframe time fill is transmitted. In response to SRES3 an XPR3 interrupt is generated. This command can be used by the external micro controller to abort a frame currently in transmission.

Global Port Configuration Register 2

GPC2_E	Offset	Reset Value
Global Port Configuration Register 2	$008A_H$	00_H

7	6	5	4	3	2	1	0
Res	FSS			Res	R1S		
	rw				rw		

Field	Bits	Type	Description
FSS	6:4	rw	**SEC/FSC Source Selection** See **Chapter 3.6**. *Note: Only valid for COMP = ´0´. For COMP = ´1´ these bits are ignored and GPC1.FSS are used.* 000_B , SEC/FSC sourced by channel 1. 001_B , SEC/FSC sourced by channel 2. 010_B , SEC/FSC sourced by channel 3. 011_B , SEC/FSC sourced by channel 4. 100_B , SEC/FSC sourced by channel 5. 101_B , SEC/FSC sourced by channel 6. 110_B , SEC/FSC sourced by channel 7. 111_B , SEC/FSC sourced by channel 8.
R1S	2:0	rw	**RCLK1 Source Selection** See **Chapter 3.6**. *Note: Only valid for COMP = ´0´. For COMP = ´1´ these bits are ignored and GPC1.R1S are used.* 000_B , RCLK1 sourced by channel 1. 001_B , RCLK1 sourced by channel 2. 010_B , RCLK1 sourced by channel 3. 011_B , RCLK1 sourced by channel 4. 100_B , RCLK1 sourced by channel 5. 101_B , RCLK1 sourced by channel 6. 110_B , RCLK1 sourced by channel 7. 111_B , RCLK1 sourced by channel 8.

Common Configuration Register 3

CCR3_E	Offset	Reset Value
Common Configuration Register 3	$xx8B_H$	00_H

7	6	5	4	3	2	1	0
RFT22	RADD2	RCRC2	XCRC2	ITF2	XMFA2	RFT12	RFT02
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RFT22	7	rw	**RFIFO2 Threshold Level - HDLC Channel 2** Highest bit to set the RFIFO2 size. See RFT12, RFT02.
RADD2	6	rw	**Receive Address Pushed to RFIFO2** If this bit is set, the received HDLC channel 2 address information (1 or 2 bytes, depending on the address mode selected via MODE2.MDS02) is pushed to RFIFO2. This function is applicable in non-auto mode and transparent mode 1.
RCRC2	5	rw	**Receive CRC ON/OFF - HDLC Channel 2** Only applicable in non-auto mode. If this bit is set, the received CRC checksum is written to RFIFO2 (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO2 by the status information byte (contents of register RSIS2). The received CRC checksum will additionally be checked for correctness. If non-auto mode is selected, the limits for “Valid Frame” check are modified.
XCRC2	4	rw	**Transmit CRC ON/OFF - HDLC Channel 2** If this bit is set, the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO2). The transmitted frame is closed automatically with a closing flag.
ITF2	3	rw	**Interframe Time Fill - HDLC Channel 2** Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller. 0_B , Continuous logical "1" is output 1_B , Continuous flag sequences are output ("01111110" bit patterns)
XMFA2	2	rw	**Transmit Multiframe Aligned - HDLC Channel 2** Determines the synchronization between the framer and the corresponding signaling controller. 0_B , The contents of the XFIFO2 is transmitted without multiframe alignment. 1_B , The contents of the XFIFO2 is transmitted multiframe aligned.

Field	Bits	Type	Description
RFT12	1	rw	**RFIFO2 Threshold Level - HDLC Channel 2** The size of the accessible part of RFIFO2 can be determined by programming these bits together with the bit RFT22. The number of valid bytes after an RPF interrupt is given in the following overview. The value of RFT(2:0)2 can be changed dynamically if reception is not running or after the current data block has been read, but before the command CMDR3.RMC2 is issued (interrupt controlled data transfer). 000_B , 32 bytes (default value) 001_B , 16 bytes 010_B , 4 bytes 011_B , 2 bytes $1xx_B$, 64 bytes
RFT02	0		

Common Configuration Register 4

CCR4_E	Offset	Reset Value
Common Configuration Register 4	$xx8C_H$	00_H

7	6	5	4	3	2	1	0
RFT23	RADD3	RCRC3	XCRC3	ITF3	XMFA3	RFT13	RFT03
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RFT23	7	rw	**RFIFO3 Threshold Level - HDLC Channel 3** Highest bit to set the RFIFO3 size. See RFT13, RFT03.
RADD3	6	rw	**Receive Address Pushed to RFIFO3** If this bit is set, the received HDLC channel 3 address information (1 or 2 bytes, depending on the address mode selected via MODE3.MDS03) is pushed to RFIFO3. This function is applicable in non-auto mode and transparent mode 1.
RCRC3	5	rw	**Receive CRC ON/OFF - HDLC Channel 3** Only applicable in non-auto mode. If this bit is set, the received CRC checksum is written to RFIFO3 (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO3 by the status information byte (contents of register RSIS3). The received CRC checksum will additionally be checked for correctness. If non-auto mode is selected, the limits for “Valid Frame” check are modified.
XCRC3	4	rw	**Transmit CRC ON/OFF - HDLC Channel 3** If this bit is set, the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO3). The transmitted frame is closed automatically with a closing flag.
ITF3	3	rw	**Interframe Time Fill - HDLC Channel 3** Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller. 0_B , Continuous logical "1" is output 1_B , Continuous flag sequences are output ("01111110" bit patterns)
XMFA3	2	rw	**Transmit Multiframe Aligned - HDLC Channel 3** Determines the synchronization between the framer and the corresponding signaling controller. 0_B , The contents of the XFIFO3 is transmitted without multiframe alignment. 1_B , The contents of the XFIFO3 is transmitted multiframe aligned.

Field	Bits	Type	Description
RFT13	1	rw	**RFIFO3 Threshold Level - HDLC Channel 3** The size of the accessible part of RFIFO3 can be determined by programming these bits together with the bit RFT23. The number of valid bytes after an RPF interrupt is given in the following overview. The value of RFT(2:0)3 can be changed dynamically if reception is not running or after the current data block has been read, but before the command CMDR4.RMC3 is issued (interrupt controlled data transfer). 00_B , 32 bytes (default value) 01_B , 16 bytes 10_B , 4 bytes 11_B , 2 bytes $1xx_B$, 64 bytes
RFT03	0		

Common Configuration Register 5

Note: These bits are only valid, if SS7 mode of HDLC channel 1 is selected by the register bits MODE.MDS(3:0).

CCR5_E	Offset	Reset Value
Common Configuration Register 5	$xx8D_H$	00_H

7	6	5	4	3	2	1	0
Res	**CSF2**	**SUET**	**CSF**	**AFX**	Res	**CR**	Res
	rw	rw	rw	rw		rw	

Field	Bits	Type	Description
CSF2	6	rw	**Compare Status Field-Mode 2** 0_B , Compare disabled 1_B , Compare enabled
SUET	5	rw	**Signaling Unit Error Threshold** Defines the number of signaling units received in error that will cause an error rate high indication (ISR1.SUEX), see **Chapter 4.3.2**. 0_B , Threshold 64 errored signaling units 1_B , Threshold 32 errored signaling units
CSF	4	rw	**Compare Status Field** If the status fields of consecutive LSSUs are equal, only the first is stored and every following is ignored, see **Chapter 4.3.2**. 0_B , Compare disabled. 1_B , Compare enabled.
AFX	3	rw	**Automatic FISU Transmission** After the contents of the transmit FIFO (XFIFO) has been transmitted completely, FISUs are transmitted automatically. These FISUs contain the FSN and BSO of the last transmitted signaling unit. 0_B , Automatic FISU transmission disabled. 1_B , Automatic FISU transmission enabled.
CR	1	rw	**Command Response HDLC Channel 1** 0_B , CR bit = ´0´. 1_B , CR bit = ´1´.

Mode Register 2

MODE2_E	Offset	Reset Value
Mode Register 2	xx8E$_H$	00$_H$

7	6	5	4	3	2	1	0
MDS2			Res	HRAC2	DIV2	HDLCI2	TSFL2
rw				rw	rw	rw	rw

Field	Bits	Type	Description
MDS2	7:5	rw	**Mode Select - HDLC Channel 2** The operating mode of the HDLC controller is selected. 000_B , Reserved 001_B , Reserved 010_B , One-byte address comparison mode (RAL1, 2) 011_B , Two-byte address comparison mode (RAH1, 2 and RAL1, 2) 100_B , No address comparison 101_B , One-byte address comparison mode (RAH1, 2) 110_B , Reserved 111_B , No HDLC framing mode 1
HRAC2	3	rw	**Receiver Active - HDLC Channel 2** Switches the HDLC receiver to operational or inoperational state. 0_B , Receiver inactive 1_B , Receiver active
DIV2	2	rw	**Data Inversion - HDLC Channel 2** Setting this bit will invert the internal generated HDLC data stream. 0_B , Normal operation, HDLC data stream not inverted 1_B , HDLC data stream inverted
HDLCI2	1	rw	**Inverse HDLC Operation Selection for HDLC Channel 2** Setting this bit will switch the HDLC controller to the system side. 0_B , HDLC protocol is sent and received on line side. 1_B , HDLC protocol is sent and received on system side.
TSFL2	0	rw	**Enable Shared Flags in Transmit Direction for HDLC Channel 2** *Note: In receive direction shared flag is detected automatically.* 0_B , Both, an opening and a closing flag (7EH) are transmitted for each HDLC frame (normal operation). 1_B , The closing flag (7EH) of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one to be transmitted.

Mode Register 3

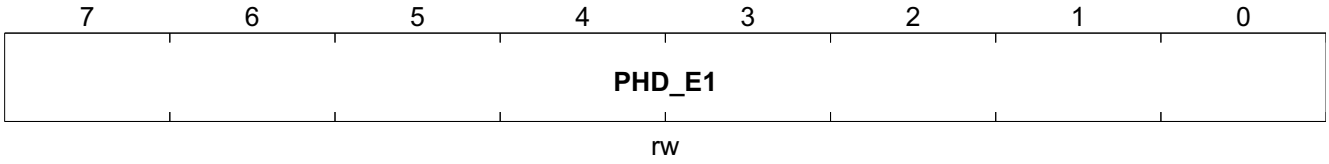
MODE3_E	Offset	Reset Value
Mode Register 3	xx8F$_H$	00$_H$

7	6	5	4	3	2	1	0
MDS3			Res	HRAC3	DIV3	HDLCI3	TSFL3
rw				rw	rw	rw	rw

Field	Bits	Type	Description
MDS3	7:5	rw	**Mode Select - HDLC Channel 3** The operating mode of the HDLC controller is selected. 000_B , Reserved 001_B , Reserved 010_B , One-byte address comparison mode (RAL1, 2) 011_B , Two-byte address comparison mode (RAH1, 2 and RAL1, 2) 100_B , No address comparison 101_B , One-byte address comparison mode (RAH1, 2) 110_B , Reserved 111_B , No HDLC framing mode 1
HRAC3	3	rw	**Receiver Active - HDLC Channel 3** Switches the HDLC receiver to operational or inoperational state. 0_B , Receiver inactive 1_B , Receiver active
DIV3	2	rw	**Data Inversion - HDLC Channel 3** Setting this bit will invert the internal generated HDLC data stream. 0_B , Normal operation, HDLC data stream not inverted 1_B , HDLC data stream inverted
HDLCI3	1	rw	**Inverse HDLC Operation Selection for HDLC Channel 3** Setting this bit will switch the HDLC controller to the system side. 0_B , HDLC protocol is sent and received on line side. 1_B , HDLC protocol is sent and received on system side.
TSFL3	0	rw	**Enable Shared Flags in Transmit Direction for HDLC Channel 3** *Note: In receive direction shared flag is detected automatically.* 0_B , Both, an opening and a closing flag (7EH) are transmitted for each HDLC frame (normal operation). 1_B , The closing flag (7EH) of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one to be transmitted.

Global Clock Mode Register 1

GCM1_E	Offset	Reset Value
Global Clock Mode Register 1	0092_H	00_H



Field	Bits	Type	Description
PHD_E1	7:0	rw	**Frequency Adjust for E1 (lower 8 bits, for highest 4 bits see GCM2)** For details see calculation formulas in register **GCM6_E** and **Table 90**.

Global Clock Mode Register 2

GCM2_E	Offset	Reset Value
Global Clock Mode Register 2	0093_H	10_H

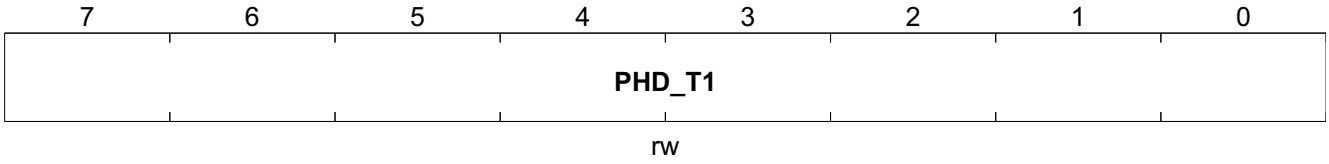
7	6	5	4	3	2	1	0
PHSDEM	PHSDIR	PHSDS	VFREQ_EN	PHD_E1			
rw	rw	rw	rw	rw			

Field	Bits	Type	Description
PHSDEM	7	rw	**RX Phase Decoder Demand** 0_B , default operation 1_B , see formulas in **GCM6_E**.
PHSDIR	6	rw	**RX Phase Decoder Direction** 0_B , default operation 1_B , see formulas in **GCM6_E**.
PHSDS	5	rw	**RX Phase Decoder Switch** 0_B , default operation 1_B , see formulas in **GCM6_E**.
VFREQ_EN	4	rw	**Variable Frequency Enable** If “fixed mode” mode is selected the clock frequency at the pin MCLK must be 2.048 for E1 or 1.544 MHz for T1/J1 respectively. The setting of the whole clock mode is done automatically: Register bits of GCM1, GCM2.PHSDEM, PHDIR, PHSDS, PHD_E1 and GCM3 to GCM8 are unused. If “fixed mode” mode is selected and the SPI- or SCI-interface is used as controller interface, the pinstrapping values at D(15:5) are also not used. See also **Chapter 3.4.6**. *Note: If “fixed mode “ is enabled all of the eight ports must work in the same mode, either in T1 or in E1 mode. A switching between E1 and T1 modes causes a reset of the whole clock system. If “fixed mode“ is disabled a switching between E1 and T1 mode (which can be done in this case individually for every port) does not cause reset of the whole clock system.* 0_B , Fixed clock frequency of 2.048 (E1) or 1.544 MHz (T1/J1) 1_B , Variable master clock frequency (normal operation, operation after reset)

Field	Bits	Type	Description
PHD_E1	3:0	rw	**Frequency Adjust for E1 (highest 4 bits, for lower 8 bits see GCM1)** The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6_E** and **Table 90**. 100000000000_B, -2048 .....B, 000000000000_B, 0 .....B, 011111111111_B, +2047

Global Clock Mode Register 3

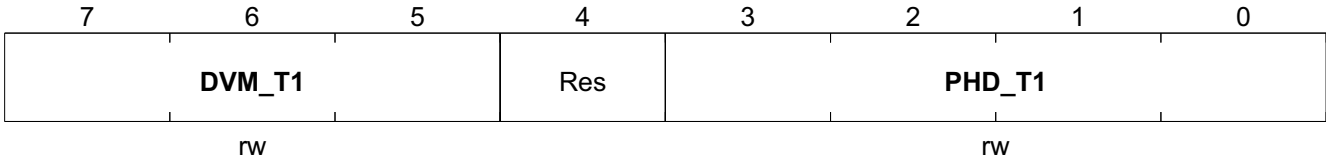
GCM3_E	Offset	Reset Value
Global Clock Mode Register 3	0094_H	00_H



Field	Bits	Type	Description
PHD_T1	7:0	rw	**Frequency Adjust for T1 (lower 8 bits, for highest 4 bits see GCM4)** The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6_E** and **Table 90**. 100000000000_B, -2048 .....$_B$, 000000000000_B, 0 .....$_B$, 011111111111_B, +2047

Global Clock Mode Register 4

GCM4_E	Offset	Reset Value
Global Clock Mode Register 4	0095_H	00_H



Field	Bits	Type	Description
DVM_T1	7:5	rw	**Divider Mode for T1** This bits can be write and read to be software compatible to QuadFALC®, but has no influence on the clock system
PHD_T1	3:0	rw	**Frequency Adjust for T1 (highest 4 bits, for lower 8 bits see GCM3)** The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6_E** and **Table 90**. 100000000000_B, -2048 .....$_B$, 000000000000_B, 0 .....$_B$, 011111111111_B, +2047

Global Clock Mode Register 5

Note: Write operations to GCM5 and GCM6 initiate a PLL reset if the asynchronous interface is selected (IM(1:0) = ´0x´) and if the "flexible master clocking mode" is selected (GCM2.VFREQ_EN = ´1´), see ***Chapter 3.4.6.1****.*

GCM5_E	Offset	Reset Value
Global Clock Mode Register 5	**0096_H**	**00_H**

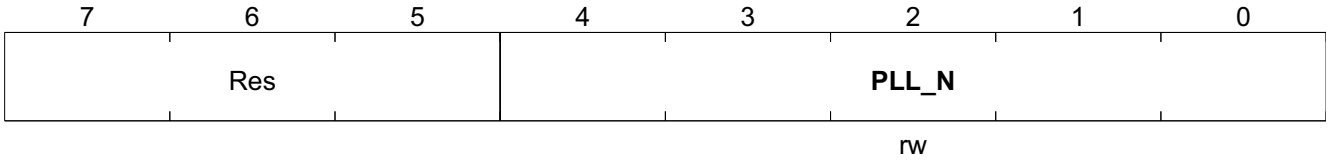
7	6	5	4	3	2	1	0
MCLK_LOW	Res		**PLL_M**				
rw			rw				

Field	Bits	Type	Description
MCLK_LOW	7	rw	**Master Clock Range Low** This bit can be write and read to be software compatible to QuadFALC®, but has no influence on the clock system.
PLL_M	4:0	rw	**PLL Dividing Factor M** For details see calculation formulas in register **GCM6_E** and **Table 90**. 00001_B, 1 .....B, 11111_B, 31

Global Clock Mode Register 6

Note: Write operations to GCM5 and GCM6 initiate a PLL reset if the asynchronous interface is selected (IM(1:0) = ´0x´) and if the "flexible master clocking mode" is selected (GCM2.VFREQ_EN = ´1´), see ***Chapter 3.4.6.1****.*

GCM6_E	Offset	Reset Value
Global Clock Mode Register 6	**0097_H**	**00_H**



Field	Bits	Type	Description
PLL_N	4:0	rw	**PLL Dividing Factor N** For details see calculation formulas in register **GCM6_E** and **Table 90**. 000001_B, 1 .....$_B$, 111111_B, 63

Flexible Clock Mode Settings:

If "flexible master clock mode" is used (VFREQ_EN = ´1´), the according register settings can be calculated as follows (a windows-based program for automatic calculation is available, see **Chapter 13.3**. For some of the standard frequencies see the table below.

1. The master clock MCLK must be in the following frequency range:

1.02 MHz ≤ f_{MCLK} ≤ 20 MHz

2. Generally the PLL of the master clocking unit includes an input divider with a dividing factor PLL_M +1 and a feedback divider with a dividing factor 4 x (PLL_N +1). So it generates a clock f_{PLL} of about

$f_{PLL} = f_{MCLK}$ x 4 x (PLL_N +1) / (PLL_M +1) .

3. The selection of PLL_N and PLL_M must be done in the following way:

The PLL frequency f_{PLL} must be in the following range:

200 MHz ≤ f_{PLL} ≤ 300 MHz.

The combinations of the values PLL_M and PLL_M must fulfill the equations:

2 MHz ≤ f_{MCLK} / (PLL_M +1) ≤ 6 MHz , if PLL_N is in the range 25 to 63.

5 MHz ≤ f_{MCLK} / (PLL_M +1) ≤ 15 MHz , if PLL_N is in the range 1 to 24.

4. The selection of PHSN_E1 and PHSX_E1 must be done in such a manner that the frequency for the receiver f_{RX_E1} has nearly the value 16 x f_{DATA_E1} x (1 + 100ppm) = 32.7713 MHz:

$f_{RX\_E1} = f_{PLL}$ / {PHSN_E1 + (PHSX_E1 / 6)} .

GCM2.PHSDEM, GCM2.PHSDIR, GCM2.PHSDS, PC5.PHDSX and PC5.PHDSR must be left to ´0´

5. To bring the "characteristic E1 frequency" f_{outE1} exact to 16 x f_{DATA_E1} = 32.7680 MHz a correction value PHD_E1 is necessary:

PHD_E1 = round **(**12288 x { [PHSN_E1 + (PHSX_E1 / 6)] - [f_{pll} / (16 x f_{DATA_E1})] }**)** .

Example: f_{MCLK} = 2.048 MHz

PLL_N = 33; PLL_M = 0 : f_{PLL} = 278.528 MHz

PHSN_E1 = 8; PHSN_E1 = 2: f_{RX_E1} = 33.42 MHz

PHD_E1 = -2048: f_{outE1} = 32.768 MHz

Table 90 Clock Mode Register Settings for E1 or T1/J1

fMCLK [MHz]	GCM1	GCM2	GCM3	GCM4	GCM5	GCM6	GCM7	GCM8
1.5440	$F0_H$	19_H	00_H	08_H	00_H	$2B_H$	98_H	DA_H
2.0480	00_H	18_H	$D2_H$	$0A_H$	00_H	21_H	$A8_H$	$9B_H$
8.1920	00_H	18_H	$D2_H$	$0A_H$	03_H	21_H	$A8_H$	$9B_H$
12.3520	$F0_H$	19_H	00_H	08_H	07_H	$2B_H$	98_H	DA_H
16.3840	00_H	18_H	$D2_H$	$0A_H$	07_H	21_H	$A8_H$	$9B_H$

Global Clock Mode Register 7

GCM7_E	Offset	Reset Value
Global Clock Mode Register 7	0098_H	80_H

7	6	5	4	3	2	1	0
1	PHSX_E1			PHSN_E1			
r	rw			rw			

Field	Bits	Type	Description
1	7	r	**Fixed ´1´**
PHSX_E1	6:4	rw	**Frequency Adjustment value E1** For details see calculation formulas in register **GCM6_E** and **Table 90**. 000_B , 0 .....B , 101_B , 5
PHSN_E1	3:0	rw	**Frequency Adjustment value E1** For details see calculation formulas in register **GCM6_E** and **Table 90**. 0001_B, 1 .....B , 1111_B, 15

Global Clock Mode Register 7

GCM8_E	Offset	Reset Value
Global Clock Mode Register 7	0099_H	80_H

7	6	5	4	3	2	1	0
1	PHSX_T1			PHSN_T1			
r	rw			rw			

Field	Bits	Type	Description
1	7	r	**Fixed ´1´**
PHSX_T1	6:4	rw	**Frequency Adjustment value T1** For details see calculation formulas in register **GCM6_E** and **Table 90**. 000_B , 0 .....$_B$, 101_B , 5
PHSN_T1	3:0	rw	**Frequency Adjustment value T1** For details see calculation formulas in register **GCM6_E** and **Table 90**. 0001_B, 1 .....$_B$, 1111_B, 15

Transmit FIFO 2 Lower Byte

Writing data to XFIFO of HDLC channel 2 can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first. Up to 32 bytes/16 words of transmit data can be written to the XFIFO following a XPR interrupt.

XFIFO2L_E	Offset	Reset Value
Transmit FIFO 2 Lower Byte	$xx9C_H$	00_H

7	6	5	4	3	2	1	0
XF7	XF6	XF5	XF4	XF3	XF2	XF1	XF0
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF7	7	w	**Transmit FIFO HDLC Channel 2**
XF6	6	w	
XF5	5	w	
XF4	4	w	
XF3	3	w	
XF2	2	w	
XF1	1	w	
XF0	0	w	

Transmit FIFO 2 Higher Byte

XFIFO2H_E	Offset	Reset Value
Transmit FIFO 2 Higher Byte	$xx9D_H$	00_H

7	6	5	4	3	2	1	0
XF15	**XF14**	**XF13**	**XF12**	**XF11**	**XF10**	**XF9**	**XF8**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF15	7	w	**Transmit FIFO for HDLC Channel 2** The function is equivalent to XFIFO2L.
XF14	6	w	
XF13	5	w	
XF12	4	w	
XF11	3	w	
XF10	2	w	
XF9	1	w	
XF8	0	w	

Transmit FIFO 3 Lower Byte

XFIFO3L_E	Offset	Reset Value
Transmit FIFO 3 Lower Byte	$xx9E_H$	00_H

7	6	5	4	3	2	1	0
XF7	XF6	XF5	XF4	XF3	XF2	XF1	XF0
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF7	7	w	**Transmit FIFO for HDLC Channel 3** The function is equivalent to XFIFO2L.
XF6	6	w	
XF5	5	w	
XF4	4	w	
XF3	3	w	
XF2	2	w	
XF1	1	w	
XF0	0	w	

Transmit FIFO 3 Higher Byte

XFIFO3H_E	Offset	Reset Value
Transmit FIFO 3 Higher Byte	$xx9F_H$	00_H

7	6	5	4	3	2	1	0
XF15	XF14	XF13	XF12	XF11	XF10	XF9	XF8
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF15	7	w	**Transmit FIFO for HDLC Channel 3** The function is equivalent to XFIFO2H.
XF14	6	w	
XF13	5	w	
XF12	4	w	
XF11	3	w	
XF10	2	w	
XF9	1	w	
XF8	0	w	

Time Slot Even/Odd Select

HDLC protocol data can be sent in even, odd or both frames of a multiframe. Even frames are frame number 2, 4,and so on, odd frames are frame number 1, 3, and so on. The selection refers to receive and transmit direction as well. Each multiframe starts with an odd frame and ends with an even frame. By default all frames are used for HDLC reception and transmission.

Note: The different HDLC channels have to be configured to use different time slots, bit positions or frames.

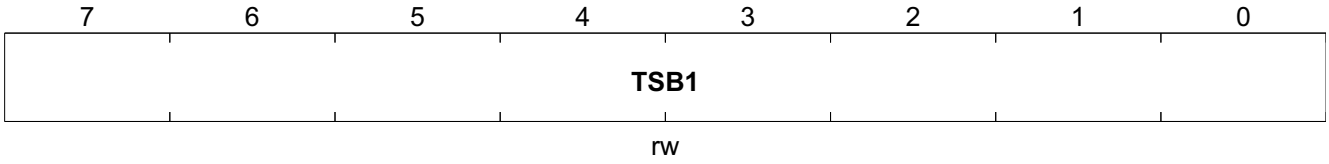
TSEO_E	Offset	Reset Value
Time Slot Even/Odd Select	$xxA0_H$	00_H

7	6	5	4	3	2	1	0
Res		EO3		EO2		EO1	
		rw		rw		rw	

Field	Bits	Type	Description
EO3	5:4	rw	**Even/Odd frame selection HDLC Channel 3** Channel 3 HDLC protocol data can be sent in even, odd or both frames of a multiframe. 00_B , Even and odd frames 01_B , Odd frames only 10_B , Even frames only 11_B , Undefined
EO2	3:2	rw	**Even/Odd frame selection HDLC Channel 2** Channel 2 HDLC protocol data can be sent in even, odd or both frames of a multiframe. 00_B , Even and odd frames 01_B , Odd frames only 10_B , Even frames only 11_B , Undefined
EO1	1:0	rw	**Even/Odd frame selection HDLC Channel 1** Channel 1 HDLC protocol data can be sent in even, odd or both frames of a multiframe. 00_B , Even and odd frames 01_B , Odd frames only 10_B , Even frames only 11_B , Undefined

Time Slot Bit Select 1

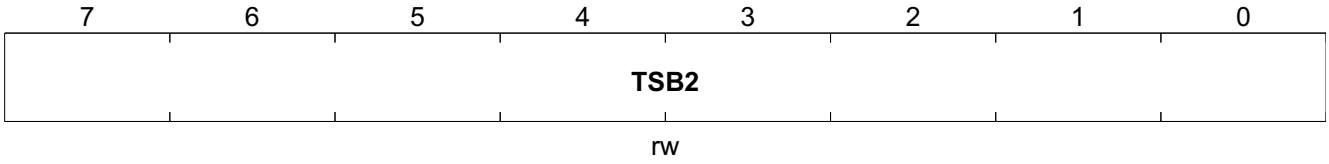
TSBS1_E	Offset	Reset Value
Time Slot Bit Select 1	$xxA1_H$	FF_H



Field	Bits	Type	Description
TSB1	7:0	rw	**Time Slot Bit Selection - HDLC Channel 1** Only bits selected by this register are used for HDLC channel 1 in selected time slots. Time slot selection is done by setting the appropriate bits in registers TTR(4:1) and RTR(4:1) independently for receive and transmit direction. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot(s) are enabled. 0_B , Bit position x in selected time slot(s) is not used for HDLC channel 1 reception and transmission. 1_B , Bit position x in selected time slot(s) is used for HDLC channel 1 reception and transmission.

Time Slot Bit Select 2

TSBS2_E	Offset	Reset Value
Time Slot Bit Select 2	$xxA2_H$	FF_H



Field	Bits	Type	Description
TSB2	7:0	rw	**Time Slot Bit Selection - HDLC Channel 2** Only bits selected by this register are used for HDLC channel 2 in selected time slots. Time slot selection is done by setting the appropriate bits in register TSS2. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot are enabled. 0_B , Bit position x in selected time slot(s) is not used for HDLC channel 2 reception and transmission. 1_B , Bit position x in selected time slot(s) is used for HDLC channel 2 reception and transmission.

Time Slot Bit Select 3

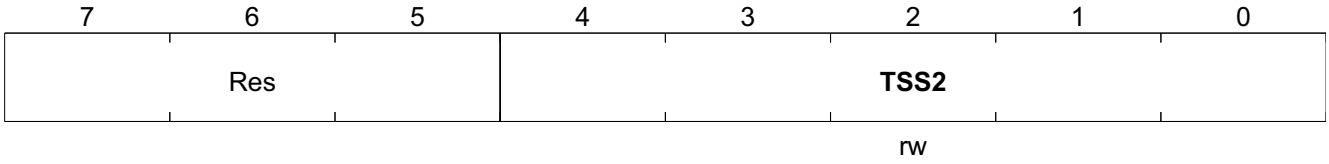
TSBS3_E	Offset	Reset Value
Time Slot Bit Select 3	$xxA3_H$	FF_H

7	6	5	4	3	2	1	0
TSB3							
rw							

Field	Bits	Type	Description
TSB3	7:0	rw	**Time Slot Bit Selection - HDLC Channel 3** Only bits selected by this register are used for HDLC channel 3 in selected time slots. Time slot selection is done by setting the appropriate bits in register TSS3. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot are enabled. 0_B , Bit position x in selected time slot(s) is not used for HDLC channel 3 reception and transmission. 1_B , Bit position x in selected time slot(s) is used for HDLC channel 3 reception and transmission.

Time Slot Select 2

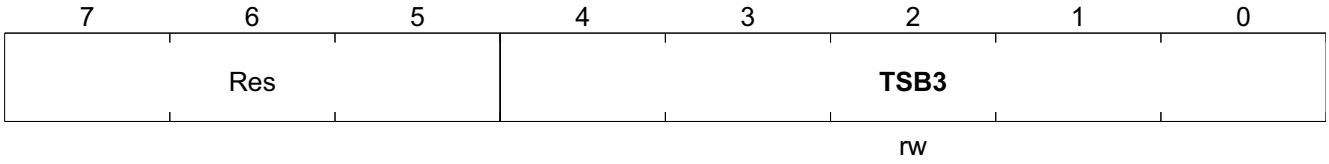
TSS2_E	Offset	Reset Value
Time Slot Select 2	**xxA4$_H$**	**00$_H$**



Field	Bits	Type	Description
TSS2	4:0	rw	**Time Slot Selection Code - HDLC Channel 2** Defines the time slot used by HDLC channel 2. *Note: Different HDLC channels must use different time slots.* 00000_B , No time slot selected 00001_B , Time slot 1 $_B$, ... 11111_B , Time slot 31

Time Slot Select 3

TSS3_E	Offset	Reset Value
Time Slot Select 3	$xxA5_H$	00_H



Field	Bits	Type	Description
TSB3	4:0	rw	**Time Slot Selection Code - HDLC Channel 3** Defines the time slot used by HDLC channel 3. *Note: Different HDLC channels must use different time slots.* 00000_B , No time slot selected 00001_B , Time slot 1 $_B$, ... 11111_B , Time slot 31

Global Interrupt Mask Register

GIMR_E	Offset	Reset Value
Global Interrupt Mask Register	$00A7_H$	FF_H

7	6	5	4	3	2	1	0
Res					**PLIL**	Res	**PLLL**
					rw		rw

Field	Bits	Type	Description
PLLL	0	rw	**PLL Locked Interrupt Mask** 0_B , GIS2.PLLLC is enabled. 1_B , GIS2.PLLLC is disabled.

Test Pattern Control Register 0

See **Chapter 4.7.1**.

TPC0_E	Offset	Reset Value
Test Pattern Control Register 0	**xxA8$_H$**	**00$_H$**

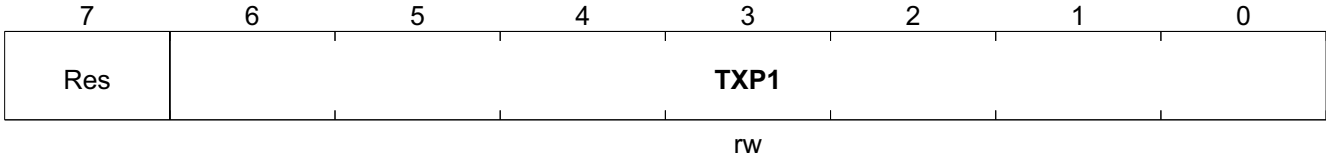
7	6	5	4	3	2	1	0
Res	**FRA**	**PRP**		**PRM**		Res	
	rw	rw		rw			

Field	Bits	Type	Description
FRA	6	rw	**Framed/Unframed Selection** 0_B , PRBS is generated/monitored unframed. Framing information is overwritten by the generator. 1_B , PRBS is generated/monitored framed. Time slot 0 is not overwritten by the generator and not observed by the monitor.
PRP	5:4	rw	**PRBS Pattern Selection** 00_B , PRBS11 pattern. 01_B , PRBS15 pattern. 10_B , PRBS20 pattern. 11_B , PRBS23 pattern.
PRM	3:2	rw	**PRBS Mode Selection** 00_B , PRBS controlled by LCR1 and TPC0.FRA. 01_B , n x 64 kbit/s PRBS. 10_B , reserved. 11_B , n x 56 kbit/s PRBS.

TX Pulse Template Register 1

See Chapter 3.7.5 and Chapter 3.7.5.2. This register contains the transmit amplitude of the 1st 1/16 of the transmit pulse. The contents of this register is ignored unless bit XPM2.XPDIS is set. By default, the values programmed in XPM0 to XPM2 are used to control the transmit pulse template.

TXP1_E	Offset	Reset Value
TX Pulse Template Register 1	**xxC1$_H$**	**38$_H$**



Field	Bits	Type	Description
TXP1	6:0	rw	**Transmit Pulse Amplitude** Two´s Complement number of pulse amplitude, see Table 25 and Table 26

Similar Registers

Registers TXP1to TXP16 have the same description and layout. Every register TXPn defines the amplitude of the part n of 16 of the transmit pulse. An overview is given is the next table.

Note that the reset values of the registers TXP1 to TXP8 are ´38$_H$´, that of the registers TXP9 to TXP16 are ´00$_H$´.

Table 91 TXP Overview

Register Short Name	Register Long Name	Offset Address	Page Number
TXP2	TX Pulse Template Register 2	C2$_H$	
TXP3	TX Pulse Template Register 3	C3$_H$	
TXP4	TX Pulse Template Register 4	C4$_H$	
TXP5	TX Pulse Template Register 5	C5$_H$	
TXP6	TX Pulse Template Register 6	C6$_H$	
TXP7	TX Pulse Template Register 7	C7$_H$	
TXP8	TX Pulse Template Register 8	C8$_H$	
TXP9	TX Pulse Template Register 9	C9$_H$	
TXP10	TX Pulse Template Register 10	CA$_H$	
TXP11	TX Pulse Template Register 11	CB$_H$	
TXP12	TX Pulse Template Register 12	CC$_H$	
TXP13	TX Pulse Template Register 13	CD$_H$	
TXP14	TX Pulse Template Register 14	CE$_H$	
TXP15	TX Pulse Template Register 15	CF$_H$	
TXP16	TX Pulse Template Register 16	D0$_H$	

Global Port Configuration Register 3

This register is only valid if COMP = ´0´ For COMP = ´1´ selection of source is not possible, always sourced by same channel. See **Chapter 3.6**.

GPC3_E	Offset	Reset Value
Global Port Configuration Register 3	**$00D3_H$**	**21_H**

7	6	5	4	3	2	1	0
Res	**R3S**			Res	**R2S**		
	rw				rw		

Field	Bits	Type	Description
R3S	6:4	rw	**RCLK3 Source Selection** 000_B , RCLK3 sourced by channel 1. 001_B , RCLK3 sourced by channel 2. 010_B , RCLK3 sourced by channel 3. 011_B , RCLK3 sourced by channel 4. 100_B , RCLK3 sourced by channel 5. 101_B , RCLK3 sourced by channel 6. 110_B , RCLK3 sourced by channel 7. 111_B , RCLK3 sourced by channel 8.
R2S	2:0	rw	**RCLK2 Source Selection** 000_B , RCLK2 sourced by channel 1. 001_B , RCLK2 sourced by channel 2. 010_B , RCLK2 sourced by channel 3. 011_B , RCLK2 sourced by channel 4. 100_B , RCLK2 sourced by channel 5. 101_B , RCLK2 sourced by channel 6. 110_B , RCLK2 sourced by channel 7. 111_B , RCLK2 sourced by channel 8.

Global Port Configuration Register 4

This register is only valid if COMP = ´0´. For COMP = ´1´ selection of source is not possible, always sourced by same channel. See **Chapter 3.6**.

GPC4_E	Offset	Reset Value
Global Port Configuration Register 4	**$00D4_H$**	**43_H**

7	6	5	4	3	2	1	0
Res	**R5S**			Res	**R4S**		
	rw				rw		

Field	Bits	Type	Description
R5S	6:4	rw	**RCLK5 Source Selection** 000_B , RCLK5 sourced by channel 1. 001_B , RCLK5 sourced by channel 2. 010_B , RCLK5 sourced by channel 3. 011_B , RCLK5 sourced by channel 4. 100_B , RCLK5 sourced by channel 5. 101_B , RCLK5 sourced by channel 6. 110_B , RCLK5 sourced by channel 7. 111_B , RCLK5 sourced by channel 8.
R4S	2:0	rw	**RCLK4 Source Selection** 000_B , RCLK4 sourced by channel 1. 001_B , RCLK4 sourced by channel 2. 010_B , RCLK4 sourced by channel 3. 011_B , RCLK4 sourced by channel 4. 100_B , RCLK4 sourced by channel 5. 101_B , RCLK4 sourced by channel 6. 110_B , RCLK4 sourced by channel 7. 111_B , RCLK4 sourced by channel 8.

Global Port Configuration Register 5

This register is only valid if COMP = ´0´. For COMP = ´1´ selection of source is not possible, always sourced by same channel. See **Chapter 3.6**.

GPC5_E	Offset	Reset Value
Global Port Configuration Register 5	**$00D5_H$**	**65_H**

7	6	5	4	3	2	1	0
Res	**R7S**			Res	**R6S**		
	rw				rw		

Field	Bits	Type	Description
R7S	6:4	rw	**RCLK7 Source Selection** 000_B , RCLK7 sourced by channel 1. 001_B , RCLK7 sourced by channel 2. 010_B , RCLK7 sourced by channel 3. 011_B , RCLK7 sourced by channel 4. 100_B , RCLK7 sourced by channel 5. 101_B , RCLK7 sourced by channel 6. 110_B , RCLK7 sourced by channel 7. 111_B , RCLK7 sourced by channel 8.
R6S	2:0	rw	**RCLK6 Source Selection** 000_B , RCLK6 sourced by channel 1. 001_B , RCLK6 sourced by channel 2. 010_B , RCLK6 sourced by channel 3. 011_B , RCLK6 sourced by channel 4. 100_B , RCLK6 sourced by channel 5. 101_B , RCLK6 sourced by channel 6. 110_B , RCLK6 sourced by channel 7. 111_B , RCLK6 sourced by channel 8.

Global Port Configuration Register 6

This register is only valid if COMP = ´0´. (For COMP = ´1´ selection of source is not possible, always sourced by same channel).

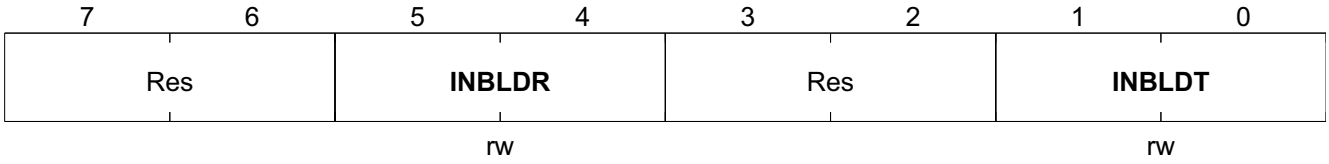
GPC6_E	Offset	Reset Value
Global Port Configuration Register 6	$00D6_H$	07_H

7	6	5	4	3	2	1	0
Res			SSI16	Res	R8S		
			rw		rw		

Field	Bits	Type	Description
SSI16	4	rw	**System Interface Multiplex Mode 16 Mbit/s** See **Chapter 4.6.1**. *Note: System data rate must be set to 16Mbit/s by SIC1.SSD(1:0) = ´11B´.* 0_B , QuadFALC® compatible multiplexed modes selected. 1_B , 16 Mbit/s, 8-to-1 multiplex system mode selected.
R8S	2:0	rw	**RCLK8 Source Selection** See **Chapter 3.6**. 000_B , RCLK8 sourced by channel 1. 001_B , RCLK8 sourced by channel 2. 010_B , RCLK8 sourced by channel 3. 011_B , RCLK8 sourced by channel 4. 100_B , RCLK8 sourced by channel 5. 101_B , RCLK8 sourced by channel 6. 110_B , RCLK8 sourced by channel 7. 111_B , RCLK8 sourced by channel 8.

In-Band Loop Detection Time Register

INBLDTR_E	Offset	Reset Value
In-Band Loop Detection Time Register	$00D7_H$	00_H



Field	Bits	Type	Description
INBLDR	5:4	rw	**In-Band Loop Detection Time for Line Side** See **Chapter 4.5.6** 00_B , at least 16 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 01_B , at least 32 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 10_B , “In-band loop sequences” must be valid for at least 4 seconds to perform automatic loop switching. 11_B , “In-band loop sequences” must be valid for at least 5 seconds to perform automatic loop switching.
INBLDT	1:0	rw	**In-Band Loop Detection Time for System Side** See **Chapter 4.5.6** 00_B , at least 16 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 01_B , at least 32 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 10_B , “In-band loop sequences” must be valid for at least 4 seconds to perform automatic loop switching. 11_B , “In-band loop sequences” must be valid for at least 5 seconds to perform automatic loop switching.

Automatic Loop Switching Register

Enabling of automatic loop switching by In-band loop codes, see **Chapter 4.5.6**, and enabling of automatic loop switching by Out-band loop codes (only in T1/J1 mode), see **Chapter 5.5.8**, is performed by this register.

ALS_E	Offset	Reset Value
Automatic Loop Switching Register	$xxD9_H$	00_H

7	6	5	4	3	2	1	0
Res				SOLS	LOLS	SILS	LILS
				rw	rw	rw	rw

Field	Bits	Type	Description
SOLS	3	rw	**System Out-Band Loop Switching (Payload Loop)** This bit controls if automatic switching of payload loop will be done by Out-Band loop codes from the line or the system side. *Note: Detection of BOM messages from the system side is only possible in "inverse configuration" of the HDLC/BOM controllers (MODE.HDLCI = ´1´). Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6).* 0_B , automatic out-band loop switching of payload is disabled (default). 1_B , automatic switching of payload loop by Out-Band loop codes (BOM messages) coming from the line side or system side is enabled if local loop is not active (LIM0.LL = ´0´). Enabling is not recommended for "inverse configuration" of the HDLC/BOM controller.
LOLS	2	rw	**Line Out-Band Loop Switching (Remote Loop)** This bit controls if automatic switching of remote loop will be done by Out-Band loop codes from the line or the system side. *Note: Detection of BOM messages from the system side is only possible in "inverse configuration" of the HDLC/BOM controllers (MODE.HDLCI = ´1´). Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6).* 0_B , automatic out-band loop switching of remote loop is disabled (default). 1_B , automatic switching of remote loop by Out-Band loop codes (BOM messages) coming from the line side or the system side is enabled if local loop is not active (LIM0.LL = ´0´).

Field	Bits	Type	Description
SILS	1	rw	**System In-Band Loop Switching (Local Loop)** This bit controls if automatic switching of the local loop will be done by In-Band loop codes from the system side, see **Chapter 4.5.6**. The necessary receiption time of In-band loop codes until an automatic loop switching is performed is configured by INBLDTR.INBLDT(1:0). *Note: This feature is not described in E1/T1/J1 standards. Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6). Setting both, SILS and LILS to ´1´ is forbidden.* 0_B , automatic switching of local loop (“on system side”) is disabled (default). 1_B , automatic switching of local loop (“on system side”) by In-band loop codes detected from the system side is enabled.
LILS	0	rw	**Line In-Band Loop Switching (Remote Loop)** This bit controls if automatic switching of the remote loop will be done by In-Band loop codes from the line side, see **Chapter 4.5.6**. The necessary receiption time of In-band loop codes until an automatic loop switching is performed is configured by INBLDTR.INBLDR(1:0). *Note: Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6). Setting both, SILS and LILS to ´1´ is forbidden.* 0_B , automatic switching of remote loop (“on line side”) is disabled (default). 1_B , automatic switching of remote loop (“on line side”) by In-band loop codes detected from the line side is enabled if local loop is not activated by LIM0.LL = ´1´.

PRBS Time Slot Register 1

Selects the used time slots for PRBS if TPC0.PRM is not ´00b´. See **Chapter 4.7.1**

PRBSTS1_E	Offset	Reset Value
PRBS Time Slot Register 1	$00DB_H$	00_H

7	6	5	4	3	2	1	0
TS0	**TS1**	**TS2**	**TS3**	**TS4**	**TS5**	**TS6**	**TS7**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS0	7	rw	**PRBS Time Slot 0 Selection** 0_B , no PRBS pattern in time slot 0. 1_B , pattern transmitted/received in time slot 0.
TS1	6	rw	**PRBS Time Slot 1 Selection** 0_B , no PRBS pattern in time slot 1. 1_B , pattern transmitted/received in time slot 1.
TS2	5	rw	**PRBS Time Slot 2 Selection** 0_B , no PRBS pattern in time slot 2. 1_B , pattern transmitted/received in time slot 2.
TS3	4	rw	**PRBS Time Slot 3 Selection** 0_B , no PRBS pattern in time slot 3. 1_B , pattern transmitted/received in time slot 3.
TS4	3	rw	**PRBS Time Slot 4 Selection** 0_B , no PRBS pattern in time slot 4. 1_B , pattern transmitted/received in time slot 4.
TS5	2	rw	**PRBS Time Slot 5 Selection** 0_B , no PRBS pattern in time slot 5. 1_B , pattern transmitted/received in time slot 5.
TS6	1	rw	**PRBS Time Slot 6 Selection** 0_B , no PRBS pattern in time slot 6. 1_B , pattern transmitted/received in time slot 6.
TS7	0	rw	**PRBS Time Slot 7 Selection** 0_B , no PRBS pattern in time slot 7. 1_B , pattern transmitted/received in time slot 7.

PRBS Time Slot Register 2

Selects the used time slots for PRBS.

PRBSTS2_E	Offset	Reset Value
PRBS Time Slot Register 2	$00DC_H$	00_H

7	6	5	4	3	2	1	0
TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS8	7	rw	**PRBS Time Slot 8 Selection** 0_B , no PRBS pattern in time slot 8. 1_B , pattern transmitted/received in time slot 8.
TS9	6	rw	**PRBS Time Slot 9 Selection** 0_B , no PRBS pattern in time slot 9. 1_B , pattern transmitted/received in time slot 9.
TS10	5	rw	**PRBS Time Slot 10 Selection** 0_B , no PRBS pattern in time slot 10. 1_B , pattern transmitted/received in time slot 10.
TS11	4	rw	**PRBS Time Slot 11 Selection** 0_B , no PRBS pattern in time slot 11. 1_B , pattern transmitted/received in time slot 11.
TS12	3	rw	**PRBS Time Slot 12 Selection** 0_B , no PRBS pattern in time slot 12. 1_B , pattern transmitted/received in time slot 12.
TS13	2	rw	**PRBS Time Slot 13 Selection** 0_B , no PRBS pattern in time slot 13. 1_B , pattern transmitted/received in time slot 13.
TS14	1	rw	**PRBS Time Slot 14 Selection** 0_B , no PRBS pattern in time slot 14. 1_B , pattern transmitted/received in time slot 14.
TS15	0	rw	**PRBS Time Slot 15 Selection** 0_B , no PRBS pattern in time slot 15. 1_B , pattern transmitted/received in time slot 15.

PRBS Time Slot Register 3

Selects the used time slots for PRBS.

PRBSTS3_E	Offset	Reset Value
PRBS Time Slot Register 3	$00DD_H$	00_H

7	6	5	4	3	2	1	0
TS16	**TS17**	**TS18**	**TS19**	**TS20**	**TS21**	**TS22**	**TS23**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS16	7	rw	**PRBS Time Slot 16 Selection** 0_B , no PRBS pattern in time slot 16. 1_B , pattern transmitted/received in time slot 16.
TS17	6	rw	**PRBS Time Slot 17 Selection** 0_B , no PRBS pattern in time slot 17. 1_B , pattern transmitted/received in time slot 17.
TS18	5	rw	**PRBS Time Slot 18 Selection** 0_B , no PRBS pattern in time slot 18. 1_B , pattern transmitted/received in time slot 18.
TS19	4	rw	**PRBS Time Slot 19 Selection** 0_B , no PRBS pattern in time slot 19. 1_B , pattern transmitted/received in time slot 19.
TS20	3	rw	**PRBS Time Slot 20 Selection** 0_B , no PRBS pattern in time slot 20. 1_B , pattern transmitted/received in time slot 20.
TS21	2	rw	**PRBS Time Slot 21 Selection** 0_B , no PRBS pattern in time slot 21. 1_B , pattern transmitted/received in time slot 21.
TS22	1	rw	**PRBS Time Slot 22 Selection** 0_B , no PRBS pattern in time slot 22. 1_B , pattern transmitted/received in time slot 22.
TS23	0	rw	**PRBS Time Slot 23 Selection** 0_B , no PRBS pattern in time slot 23. 1_B , pattern transmitted/received in time slot 23.

PRBS Time Slot Register 4

Selects the used time slots for PRBS. Not valid in channel translation mode.

PRBSTS4_E	Offset	Reset Value
PRBS Time Slot Register 4	$00DE_H$	00_H

7	6	5	4	3	2	1	0
TS24	**TS25**	**TS26**	**TS27**	**TS28**	**TS29**	**TS30**	**TS31**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS24	7	rw	**PRBS Time Slot 24 Selection** 0_B , no PRBS pattern in time slot 24. 1_B , pattern transmitted/received in time slot 24.
TS25	6	rw	**PRBS Time Slot 25 Selection** 0_B , no PRBS pattern in time slot 25. 1_B , pattern transmitted/received in time slot 25.
TS26	5	rw	**PRBS Time Slot 26 Selection** 0_B , no PRBS pattern in time slot 26. 1_B , pattern transmitted/received in time slot 26.
TS27	4	rw	**PRBS Time Slot 27 Selection** 0_B , no PRBS pattern in time slot 27. 1_B , pattern transmitted/received in time slot 27.
TS28	3	rw	**PRBS Time Slot 28 Selection** 0_B , no PRBS pattern in time slot 28. 1_B , pattern transmitted/received in time slot 29.
TS29	2	rw	**PRBS Time Slot 29 Selection** 0_B , no PRBS pattern in time slot 29. 1_B , pattern transmitted/received in time slot 29.
TS30	1	rw	**PRBS Time Slot 30 Selection** 0_B , no PRBS pattern in time slot 30. 1_B , pattern transmitted/received in time slot 30.
TS31	0	rw	**PRBS Time Slot 31 Selection** 0_B , no PRBS pattern in time slot 31. 1_B , pattern transmitted/received in time slot 31.

Interrupt Mask Register 7

Masks interrupt bits of register ISR7.

IMR7_E	Offset	Reset Value
Interrupt Mask Register 7	$xxDF_H$	FF_H

7	6	5	4	3	2	1	0
Res			XCLKSS1	XCLKSS0	Res		
			rw	rw			

Field	Bits	Type	Description
XCLKSS1	4	rw	**XCLKSS1 Interrupt Masking** 0_B , ISR7.XCLKSS1 is enabled. 1_B , ISR7.XCLKSS1 is disabled
XCLKSS0	3	rw	**XCLKSS0 Interrupt Masking** 0_B , ISR7.XCLKSS0 is enabled. 1_B , ISR7.XCLKSS0 is disabled

7.2 Detailed Description of E1 Status Registers

Receive FIFO - HDLC Channel 1 - Lower Byte

RFIFO1L_E	Offset	Reset Value
Receive FIFO - HDLC Channel 1 - Lower Byte	$xx00_H$	xx_H

7	6	5	4	3	2	1	0
RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF7	7	r	**RFIFO Data** Reading data from RFIFO of HDLC channel 1 can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface. The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT(1:0) and MODE.RFT2 (RFIFO threshold level), see Chapter 3.4.3. Data Transfer: Up to 64bytes/32 words of received data can be read from the RFIFO following an RPF or an RME interrupt. RPF Interrupt: A fixed number of bytes/words to be read (64, 32, 16, 4, 2 bytes). The message is not yet complete. RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers. RFIFO is released by issuing the RMC (Receive Message Complete) command.
RF6	6	r	
RF5	5	r	
RF4	4	r	
RF3	3	r	
RF2	2	r	
RF1	1	r	
RF0	0	r	

Receive FIFO - HDLC Channel 1 - Higher Byte

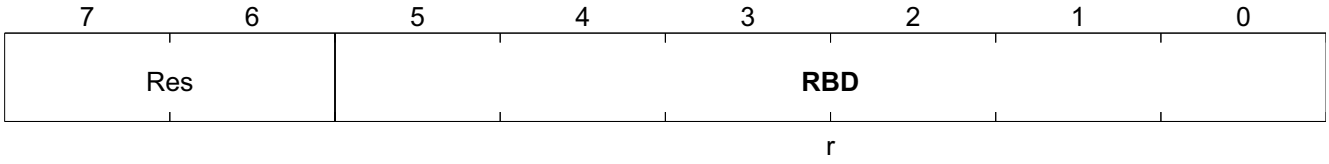
RFIFO1H_E	Offset	Reset Value
Receive FIFO - HDLC Channel 1 - Higher Byte	$xx01_H$	xx_H

7	6	5	4	3	2	1	0
RF15	**RF14**	**RF13**	**RF12**	**RF11**	**RF10**	**RF9**	**RF8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF15	7	r	**RFIFO Data** Reading data from RFIFO of HDLC channel 1 can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface. The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT(1:0) and MODE.RFT2 (RFIFO threshold level), see **Chapter 3.4.3**. Data Transfer: Up to 64bytes/32 words of received data can be read from the RFIFO following an RPF or an RME interrupt. RPF Interrupt: A fixed number of bytes/words to be read (64, 32, 16, 4, 2 bytes). The message is not yet complete. RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers. RFIFO is released by issuing the RMC (Receive Message Complete) command.
RF14	6	r	
RF13	5	r	
RF12	4	r	
RF11	3	r	
RF10	2	r	
RF9	1	r	
RF8	0	r	

Receive Buffer Delay

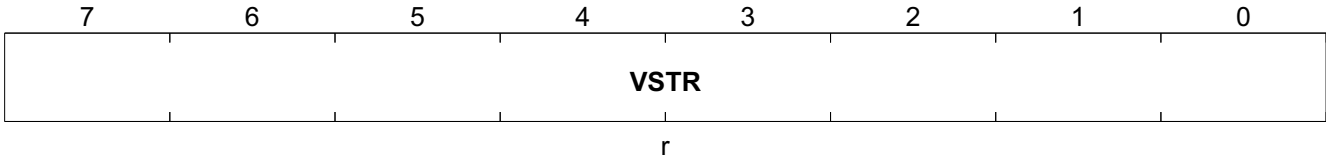
RBD_E	Offset	Reset Value
Receive Buffer Delay	$xx49_H$	00_H



Field	Bits	Type	Description
RBD	5:0	r	**Receive Elastic Buffer Delay** These bits informs the user about the current delay (in time slots) through the receive elastic buffer. The delay is updated every 512 or 256 bits (SIC1.RBS(1:0)). Before reading this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed. 000000_B , Delay < 1 time slot B , ... 111111_B , Delay > 63 time slot

Version Status Register

VSTR_E	Offset	Reset Value
Version Status Register	$004A_H$	H



Field	Bits	Type	Description
VSTR	7:0	r	**Version Number of Chip** Status information depends on the setting of input signal COMP. See **Figure 96** for more details.

Receive Equalizer Status

RES_E	Offset	Reset Value
Receive Equalizer Status	$xx4B_H$	00_H

7	6	5	4	3	2	1	0
EV		Res	**RES**				
r			r				

Field	Bits	Type	Description
EV	7:6	r	**Equalizer Status Valid** These bits informs the user about the current state of the receive equalization network. 00_B , Equalizer status not valid, still adapting 01_B , Equalizer status valid 10_B , Equalizer status not valid 11_B , Equalizer status valid but high noise floor
RES	4:0	r	**Receive Equalizer Status** The current line attenuation status in steps of about 1.7 dB are displayed in these bits. Only valid if bits EV(1:0) = ´01_b´. Accuracy: ± 2 digits, based on temperature influence and noise amplitude variations. 00000_B , Minimum attenuation: 0 dB $_B$, ... 11001_B , Maximum attenuation: -43 dB

Framer Receive Status Register 0

FRS0_E	Offset	Reset Value
Framer Receive Status Register 0	$xx4C_H$	00_H

7	6	5	4	3	2	1	0
LOS	**AIS**	**LFA**	**RRA**	Res	**NMF**	**LMFA**	Res
r	r	r	r		r	r	

Field	Bits	Type	Description
LOS	7	r	**Loss-of-Signal** • Detection: This bit is set when the incoming signal has “no transitions” (analog interface) or logical zeros (digital interface) in a time interval of T consecutive pulses, where T is programmable by register PCD. Total account of consecutive pulses: 16 ≤ T ≤ 4096. Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL(2:0). • Recovery: Analog interface: The bit is reset in short-haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL(2:0)) for at least M pulse periods defined by register PCR in the PCD time interval. In long-haul mode additionally bit RES.6 must be set for at least 250 µs. Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval. With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. The bit is also set during alarm simulation and reset, if FMR0.SIM is cleared and no alarm condition exists.
AIS	6	r	**Alarm Indication Signal** The function of this bit is determined by FMR0.ALM. • FMR0.ALM = ´0´: This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 ms and the OctalFALCTM is in asynchronous state (FRS0.LFA = ´1´). The bit is reset when no alarm condition is detected (according to ETSI standard). • FMR0.ALM = ´1´: This bit is set when the incoming signal has two or less Zeros in each of two consecutive double frame period (512 bits). This bit is cleared when each of two consecutive doubleframe periods contain three or more zeros or when the frame alignment signal FAS has been found. (ITU-T G.775) The bit is also set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set.

Field	Bits	Type	Description
LFA	5	r	**Loss of Frame Alignment** This bit is set after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (can be disabled). With the rising edge of this bit an interrupt status bit (ISR2.LFA) is set. The specification of the loss of synchronization conditions is done by bits RC0.SWD and RC0.ASY4. After loss of synchronization, the frame aligner resynchronizes automatically. The following conditions have to be detected to regain synchronous state: • The presence of the correct FAS word in frame n. • The presence of the correct service word (bit 2 = ´1´) in frame n+1. • For a second time the presence of a correct FAS word in frame n+2. The bit is cleared when synchronization has been regained (directly after the second correct FAS word of the procedure described above has been received).If the CRC-multiframe structure is enabled by setting bit FMR2.RFS1, multiframe alignment is assumed to be lost if pulseframe synchronization has been lost. The resynchronization procedure for multiframe alignment starts after the bit FRS0.LFA has been cleared.Multiframe alignment has been regained if two consecutive CRC-multiframes have been received without a framing error (refer to FRS0.LMFA).The bit is set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.If bit FRS0.LFA is cleared a loss of frame alignment recovery interrupt status ISR2.FAR is generated.
RRA	4	r	**Receive Remote Alarm** Set if bit 3 of the received service word is set. An alarm interrupt status ISR2.RA can be generated if the alarm condition is detected. FRS0.RRA is cleared if no alarm is detected. At the same time a remote alarm recovery interrupt status ISR2.RAR is generated. The bit RSW.RRA has the same function.Both status and interrupt status bits are set during alarm simulation.
NMF	2	r	**No Multiframe Alignment Found** This bit is only valid if the CRC4 interworking is selected (FMR2.RFS(1:0) = 11). Set if the multiframe pattern is not detected in a time interval of 400 ms after the framer has reached the doubleframe synchronous state. The receiver is then automatically switched to doubleframe format.This bit is reset if the basic framing has been lost.
LMFA	1	r	**Loss of Multiframe Alignment** Not used in doubleframe format (FMR2.RFS1 = ´0´). In this case LMFA is set.In CRC-multiframe mode (FMR2.RFS1 = ´1´), this bit is set • If force resynchronization is initiated by setting bit FMR0.FRS, or • If multiframe force resynchronization is initiated by setting bit FMR1.MFCS, or • If pulseframe alignment has been lost (FRS0.LFA). It is reset if two CRC-multiframes have been received at an interval of n x 2 ms (n = 1, 2, 3 and so forth) without a framing error. If bit FRS0.LMFA is cleared a loss of multiframe alignment recovery interrupt status ISR2.MFAR is generated.

Framer Receive Status Register 1

FRS1_E	Offset	Reset Value
Framer Receive Status Register 1	$xx4D_H$	xx_H

7	6	5	4	3	2	1	0
EXZD	TS16RA	TS16LOS	TS16AIS	TS16LFA	RDI	XLS	XLO
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
EXZD	7	r	**Excessive Zeros Detected** Significant only, if excessive zero detection has been enabled (FMR0.EXZE = ´1´). Set after detection of more than 3 (HDB3 code) or 15 (AMI code) contiguous zeros in the received data stream.This bit is cleared on read.
TS16RA	6	r	**Receive Time Slot 16 Remote Alarm** This bit contains the actual information of the received remote alarm bit RS1.2 in time slot 16. Setting and resetting of this bit causes an interrupt status change ISR3.RA16.
TS16LOS	5	r	**Receive Time Slot 16 Loss-of-Signal** This bit is set if the incoming TS16 data stream contains always zeros for at least 16 contiguously received time slots. A one in a time slot 16 resets this bit.
TS16AIS	4	r	**Receive Time Slot 16 Alarm Indication Signal** The detection of the alarm indication signal in time slot 16 is according to ITU-T G.775.This bit is set if the incoming TS16 contains less than 4 zeros in each of two consecutive TS16 multiframe periods. This bit is cleared if two consecutive received CAS multiframe periods contains more than 3 zeros or the multiframe pattern was found in each of them. This bit is cleared if TS0 synchronization is lost.
TS16LFA	3	r	**Receive Time Slot 16 Loss of Multiframe Alignment** 0_B , The CAS controller is in synchronous state after frame alignment is accomplished. 1_B , This bit is set if the framing pattern "0000" in 2 consecutive CAS multiframes were not found or in all TS16 of the preceding multiframe all bits were reset. An interrupt ISR3.LMFA16 is generated.

Field	Bits	Type	Description
RDI	2	r	**Remote Defect Indication** Remote Defect Indication (RDI) defect at 2048 kbit/s path termination functions is detected when the incoming signal has the "Remote alarm indication" bit set to binary ONE ("1") for z consecutive double frame periods. The RDI defect is cleared when the incoming signal has the "Remote alarm indication" bit set to binary ZERO ("0") for z consecutive double frame periods.The Remote alarm indication bit is the "A bit" in the 2048 kbit/s frame defined in Recommendation G.704. Configuring of the number z will be done by register bits RDICR.RDIC and RDICR.RDIS. 0_B , no RDI condition has been detected 1_B , RDI condition is present.
XLS	1	r	**Transmit Line Short** See **Chapter 3.7.6**. Significant only if the ternary line interface is selected by LIM1.DRS = ´0´. Note that shorts in generic transmit line interface mode are not detected and will not ham the device. 0_B , Normal operation. No short is detected. 1_B , The XL1 and XL2 are shortened for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high-impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high-impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen.
XLO	0	r	**Transmit Line Open** See also **Chapter 3.7.6**. 0_B , Normal operation 1_B , This bit is set if at least 32 consecutive zeros were sent on pins XL1/XL2 or XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen.

Receive Service Word Pulseframe

RSW_E	Offset	Reset Value
Receive Service Word Pulseframe	$xx4E_H$	xx_H

7	6	5	4	3	2	1	0
RSI	Res	**RRA**	**RY0**	**RY1**	**RY2**	**RY3**	**RY4**
r		r	r	r	r	r	r

Field	Bits	Type	Description
RSI	7	r	**Receive Spare Bit for International Use** First bit of the received service word. It is fixed to one if CRC-multiframe mode is enabled.
RRA	5	r	**Receive Remote Alarm** Equivalent to bit FRS0.RRA.
RY0	4	r	**Receive Spare Bits for National Use (Y-Bits, Sn-Bits, Sa-Bits)**
RY1	3		
RY2	2		
RY3	1		
RY4	0		

Receive Spare Bits/Additional Status

RSP_E	Offset	Reset Value
Receive Spare Bits/Additional Status	$xx4F_H$	xx_H

7	6	5	4	3	2	1	0
SI1	**SI2**	Res	**LLBDD**	**LLBAD**	**RSIF**	**RS13**	**RS15**
r	r		r	r	r	r	r

Field	Bits	Type	Description
SI1	7	r	**Submultiframe Error Indication 1, 2** Not valid if doubleframe format is enabled. In this case, both bits are set.When using CRC-multiframe format these bits are set to the following values. Both flags are updated with the beginning of every received CRC multiframe.If automatic transmission of submultiframe status is enabled by setting bit XSP.AXS, above status information is inserted automatically in Si-bit position of every outgoing CRC multiframe (under the condition that time slot 0 transparent modes are both disabled): SI1 → Si -bit of frame 13, SI2 → Si -bit of frame 15. 0_B , If multiframe alignment has been lost, or if the last multiframe has been received with CRC error(s). SI1 flags a CRC error in last submultiframe 1, SI2 flags a CRC error in last submultiframe 2. 1_B , If at multiframe synchronous state last assigned submultiframe has been received without a CRC error.
SI2	6		
LLBDD	4	r	**Line Loop-Back Deactivation Signal Detected** This bit is set in case of the LLB deactivate signal is detected and then received over a period of more than 25 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the time slot 0 is not taken into account for the error rate calculation.Any change of this bit causes an LLBSC interrupt.
LLBAD	3	r	**Line Loop-Back Activation Signal Detected** Depending on bit LCR1.EPRM the source of this status bit changed. • LCR1.EPRM = ´0´: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 25 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the time slot 0 is not taken into account for the error rate calculation. Any change of this bit causes an LLBSC interrupt. • LCR1.EPRM = ´1´: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of 10^{-1}. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo-random binary sequence.

Field	Bits	Type	Description
RSIF	2	r	**Receive Spare Bit for International Use (FAS Word)** First bit in FAS-word. Used only in doubleframe format, otherwise fixed to "1".
RS13	1	r	**Receive Spare Bit (Frame 13, CRC Multiframe)** First bit in service word of frame 13. Significant only in CRC-multiframe format, otherwise fixed to "0". This bit is updated with beginning of every received CRC multiframe.
RS15	0	r	**Receive Spare Bit (Frame 15, CRC Multiframe)** First bit in service word of frame 15. Significant only in CRC-multiframe format, otherwise fixed to "0". This bit is updated with beginning of every received CRC multiframe.

Framing Error Counter Lower Byte

FECL_E	Offset	Reset Value
Framing Error Counter Lower Byte	$xx50_H$	00_H

7	6	5	4	3	2	1	0
FE7	**FE6**	**FE5**	**FE4**	**FE3**	**FE2**	**FE1**	**FE0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FE7	7	r	**Framing Errors** This 16-bit counter is incremented when a FAS word has been received with an error.Framing errors are counted during basic frame synchronous state only (but even if multiframe synchronous state is not reached yet). During alarm simulation, the counter is incremented every 250 ms up to its saturation. The error counter does not roll over.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
FE6	6	r	
FE5	5	r	
FE4	4	r	
FE3	3	r	
FE2	2	r	
FE1	1	r	
FE0	0	r	

Framing Error Counter Higher Byte

FECH_E	Offset	Reset Value
Framing Error Counter Higher Byte	$xx51_H$	00_H

7	6	5	4	3	2	1	0
FE15	**FE14**	**FE13**	**FE12**	**FE11**	**FE10**	**FE9**	**FE8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FE15	7	r	**Framing Errors** This 16-bit counter is incremented when a FAS word has been received with an error.Framing errors are counted during basic frame synchronous state only (but even if multiframe synchronous state is not reached yet). During alarm simulation, the counter is incremented every 250 ms up to its saturation. The error counter does not roll over.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
FE14	6	r	
FE13	5	r	
FE12	4	r	
FE11	3	r	
FE10	2	r	
FE9	1	r	
FE8	0	r	

Code Violation Counter Lower Byte

CVCL_E	Offset	Reset Value
Code Violation Counter Lower Byte	$xx52_H$	00_H

7	6	5	4	3	2	1	0
CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CV7	7	r	**Code Violations** No function if NRZ code has been enabled. If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected . The error detection mode is determined by programming the bit FMR0.EXZE. If simple AMI coding is enabled (FMR0.RC(1:0) = ´01_b´) all bipolar violations are counted. If HDB3 code is enabled, counting of bipolar violations in substitution patterns is only done, if the violation bits of two consecutive substitution patterns have different polarities. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CV6	6	r	
CV5	5	r	
CV4	4	r	
CV3	3	r	
CV2	2	r	
CV1	1	r	
CV0	0	r	

Code Violation Counter Higher Byte

CVCH_E	Offset	Reset Value
Code Violation Counter Higher Byte	$xx53_H$	00_H

7	6	5	4	3	2	1	0
CV15	CV14	CV13	CV12	CV11	CV10	CV9	CV8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CV15	7	r	**Code Violations** No function if NRZ code has been enabled.If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit FMR0.EXTD. If simple AMI coding is enabled (FMR0.RC(1:0) = ´01_b´) all bipolar violations are counted. If HDB3 code is enabled, counting of bipolar violations in substitution patterns is only done, if the violation bits of two consecutive substitution patterns have different polarities. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CV14	6	r	
CV13	5	r	
CV12	4	r	
CV11	3	r	
CV10	2	r	
CV9	1	r	
CV8	0	r	

CRC Error Counter 1 Lower Byte

CEC1L_E	Offset	Reset Value
CRC Error Counter 1 Lower Byte	$xx54_H$	00_H

7	6	5	4	3	2	1	0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CR7	7	r	**CRC Errors** No function if doubleframe format is selected.In CRC-multiframe mode, the 16-bit counter is incremented when a CRC-submultiframe has been received with a CRC error. CRC errors are not counted during asynchronous state. The error counter does not roll over.During alarm simulation, the counter is incremented once per submultiframe up to its saturation.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC1 is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CR6	6	r	
CR5	5	r	
CR4	4	r	
CR3	3	r	
CR2	2	r	
CR1	1	r	
CR0	0	r	

CRC Error Counter 1 Higher Byte

CEC1H_E	Offset	Reset Value
CRC Error Counter 1 Higher Byte	$xx55_H$	00_H

7	6	5	4	3	2	1	0
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CR15	7	r	**CRC Errors** No function if doubleframe format is selected.In CRC-multiframe mode, the 16-bit counter is incremented when a CRC-submultiframe has been received with a CRC error. CRC errors are not counted during asynchronous state. The error counter does not roll over.During alarm simulation, the counter is incremented once per submultiframe up to its saturation.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC1 is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CR14	6	r	
CR13	5	r	
CR12	4	r	
CR11	3	r	
CR10	2	r	
CR9	1	r	
CR8	0	r	

E-Bit Error Counter Lower Byte

EBCL_E	Offset	Reset Value
E-Bit Error Counter Lower Byte	$xx56_H$	00_H

7	6	5	4	3	2	1	0
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
EB7	7	r	**E-Bit Errors** If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. The error counter does not roll over. During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
EB6	6	r	
EB5	5	r	
EB4	4	r	
EB3	3	r	
EB2	2	r	
EB1	1	r	
EB0	0	r	

E-Bit Error Counter Higher Byte

EBCH_E	Offset	Reset Value
E-Bit Error Counter Higher Byte	$xx57_H$	00_H

7	6	5	4	3	2	1	0
EB15	**EB14**	**EB13**	**EB12**	**EB11**	**EB10**	**EB9**	**EB8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
EB15	7	r	**E-Bit Errors** If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. The error counter does not roll over. During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
EB14	6	r	
EB13	5	r	
EB12	4	r	
EB11	3	r	
EB10	2	r	
EB9	1	r	
EB8	0	r	

CRC Error Counter 2 Lower Byte

CEC2L_E	Offset	Reset Value
CRC Error Counter 2 Lower Byte	$xx58_H$	00_H

7	6	5	4	3	2	1	0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CC7	7	r	**CRC Error Counter (reported from TE through Sa6 -Bit)** Depending on bit LCR1.EPRM the error counter increment is selected: • LCR1.EPRM = ´0´: If doubleframe format is selected, CEC2H/L has no function. If CRC-multiframe mode is enabled, CEC2H/L works as Sa6-bit error indication counter (16 bits) which counts the Sa6-bit sequence 0001 and 0011 in every received CRC submultiframe. Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = ´0´. Sa6-bit sequence: SA61, SA62, SA63, SA64 = 0001 or 0011 where SA61 is received in frame 1 or 9 in every multiframe. During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Pseudo-Random Binary Sequence Error Counter • LCR1.EPRM = ´1´: This 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state RSP.LLBAD = ´1´. The error counter does not roll over. During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC2 has to be set. With the rising edge of this bit updating of the buffer is stopped and the error counter is reset. Bit DEC.DCEC2 is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then reset automatically. The latched error counter state should be read within the next second.
CC6	6	r	
CC5	5	r	
CC4	4	r	
CC3	3	r	
CC2	2	r	
CC1	1	r	
CC0	0	r	

CRC Error Counter 2 Higher Byte

CEC2H_E	Offset	Reset Value
CRC Error Counter 2 Higher Byte	$xx59_H$	00_H

7	6	5	4	3	2	1	0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CC15	7	r	**CRC Error Counter (reported from TE through Sa6 -Bit)** Depending on bit LCR1.EPRM the error counter increment is selected: • LCR1.EPRM = ´0´: If doubleframe format is selected, CEC2H/L has no function. If CRC-multiframe mode is enabled, CEC2H/L works as Sa6-bit error indication counter (16 bits) which counts the Sa6-bit sequence 0001 and 0011 in every received CRC submultiframe. Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = ´0´. Sa6-bit sequence: SA61, SA62, SA63, SA64 = 0001 or 0011 where SA61 is received in frame 1 or 9 in every multiframe. During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Pseudo-Random Binary Sequence Error Counter • LCR1.EPRM = ´1´: This 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state RSP.LLBAD = ´1´. The error counter does not roll over. During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC2 has to be set. With the rising edge of this bit updating of the buffer is stopped and the error counter is reset. Bit DEC.DCEC2 is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then reset automatically. The latched error counter state should be read within the next second.
CC14	6	r	
CC13	5	r	
CC12	4	r	
CC11	3	r	
CC10	2	r	
CC9	1	r	
CC8	0	r	

CRC Error Counter 3 Lower Byte

CRC Error Counter (detected at T Reference Point in Sa6-Bit) for CE(15:0): GCR.ECMC = ´0´: If doubleframe format is selected, CEC3H/L has no function. If CRC-multiframe mode is enabled, CEC3H/L works as Sa6-bit error indication counter (16 bits) which counts the Sa6-bit sequence ´0010_b´ and ´0011_b´ in every received CRC submultiframe.

Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.Sa6-bit sequence: SA61, SA62, SA63, SA64 = ´0010_b´ or ´0011_b´ where SA61 is received in frame 1 or 9 in every multiframe. The error counter does not roll over.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

CEC3L_E	Offset	Reset Value
CRC Error Counter 3 Lower Byte	$xx5A_H$	00_H

7	6	5	4	3	2	1	0
CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CE7	7	r	**Multiframe Counter** GCR.ECMC = ´1´: This 6-bit counter increments with each multiframe period in the asynchronous state FRS0.LFA/LMFA = ´1´. During alarm simulation, the counter is incremented once per multiframe up to its saturation.
CE6	6		
CE5	5		
CE4	4		
CE3	3		
CE2	2		
CE1	1	r	**Change of Frame Alignment Counter** GCR.ECMC = ´1´: This 2-bit counter increments with each detected change of frame/multiframe alignment. The error counter does not roll over. During alarm simulation, the counter is incremented once per multiframe up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC3 has to be set. With the rising edge of this bit updating of the buffer is stopped and the error counter is reset. Bit DEC.DCEC3 is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CE0	0		

CRC Error Counter 3 Higher Byte

CRC Error Counter (detected at T Reference Point in Sa6-Bit) for CE(15:0): GCR.ECMC = ´0´: If doubleframe format is selected, CEC3H/L has no function. If CRC-multiframe mode is enabled, CEC3H/L works as Sa6-bit error indication counter (16 bits) which counts the Sa6-bit sequence 0010_b´ and 0011_b´ in every received CRC submultiframe.

Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = ´0´. Sa6-bit sequence: SA61, SA62, SA63, SA64 = ´0010_b´ or ´0011_b´ where SA61 is received in frame 1 or 9 in every multiframe. The error counter does not roll over.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

CEC3H_E	Offset	Reset Value
CRC Error Counter 3 Higher Byte	$xx5B_H$	00_H

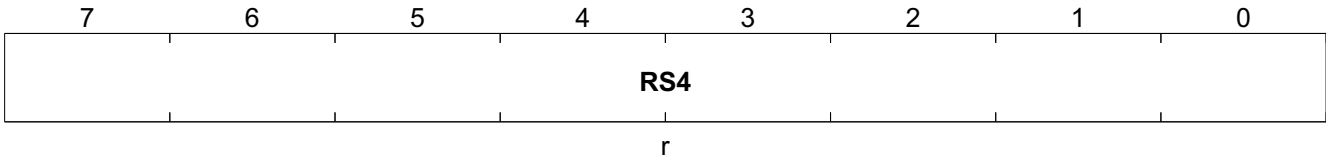
7	6	5	4	3	2	1	0
CE15	CE14	CE13	CE12	CE11	CE10	CE9	CE8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CE15	7	r	**CRC Error Counter/Multiframe Counter** Depending on bit GCR.ECMC the counter increment is selected: • GCR.ECMC = ´0´ (CRC error counter): If doubleframe format is selected, CEC3H/L has no function. If CRC-multiframe mode is enabled, CEC3H/L works as Sa6-bit error indication counter (16 bits) which counts the Sa6-bit sequence ´0010_b´ and ´0011_b´ in every received CRC submultiframe. Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = ´0´. Sa6-bit sequence: SA61, SA62, SA63, SA64 = ´0010_b´ or ´0011_b´ where SA61 is received in frame 1 or 9 in every multiframe. During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Pseudo-Random Binary Sequence Error Counter • GCR.ECMC = ´1´ (Multiframe counter): This 6-bit counter increments with each multiframe period in the asynchronous state FRS0.LFA/LMFA = ´1´. During alarm simulation, the counter is incremented once per multiframe up to its saturation.
CE14	6	r	
CE13	5	r	
CE12	4	r	
CE11	3	r	
CE10	2	r	
CE9	1	r	
CE8	0	r	

Receive Sa4-Bit Register

This register contains the information of the eight Sax bits (x = 4 to 8) of the previously received CRC multiframe. These registers are updated with every multiframe begin interrupt ISR0.RMB.Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = ´1´ or FMR2.RFS(1:0) = ´01_b´ (doubleframe format).

RSA4_E	Offset	Reset Value
Receive Sa4-Bit Register	$xx5C_H$	xx_H



Field	Bits	Type	Description
RS4	7:0	r	**Receive Sa4-Bit Data (Y-Bits)** RS40 is received in bit-slot 4 of every service word in frame 1, RS47 in frame 15

Similar Registers

Registers RSA5 to RSA8 have the same layout and description.

The Offset Addresses are listed in **RSAn Overview**, for bit names refer to **Receive San-Bit Registers**.

Table 92 RSAn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
RSA5	Receive Sa5-Bit Register	$5D_H$	
RSA6	Receive Sa6-Bit Register	$5E_H$	
RSA7	Receive Sa7-Bit Register	$5F_H$	
RSA8	Receive Sa8-Bit Register	60_H	

Table 93 Receive San-Bit Registers

	7	6	5	4	3	2	1	0
RSA4	RS47	RS46	RS45	RS44	RS43	RS42	RS41	RS40
RSA5	RS57	RS56	RS55	RS54	RS53	RS52	RS51	RS50
RSA6	RS67	RS66	RS65	RS64	RS63	RS62	RS61	RS60
RSA7	RS77	RS76	RS75	RS74	RS73	RS72	RS71	RS70
RSA8	RS87	RS86	RS85	RS84	RS83	RS82	RS81	RS80

Receive Sa6-Bit Status

Four consecutive received Sa6-bits are checked on the by ETS300233 defined Sa6-bit combinations. The OctalFALCTM detects the following “fixed” Sa6-bit combinations: SA61, SA62, SA63, SA64 = ´1000_b´, ´1010_b´, ´1100_b´, ´1110_b´, ´1111_b´. All other possible 4-bit combinations are grouped to status “X”.

A valid Sa6-bit combination must occur three times in a row. The corresponding status bit in this register is set. Even if the detected status is active for a short time the status bit remains active until this register is read. Reading the register resets all pending status information.

With any change of state of the Sa6-bit combinations an interrupt status ISR0.SA6SC is generated.

During the basic frame asynchronous state updating of this register and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the Sa6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synchronous state (FRS0.LMFA = ´0´). In asynchronous detection mode updating is independent to the multiframe synchronous state.

RSA6S_E	Offset	Reset Value
Receive Sa6-Bit Status	$xx61_H$	xx_H

7	6	5	4	3	2	1	0
Res		S_X	S_F	S_E	S_C	S_A	S_8
		r	r	r	r	r	r

Field	Bits	Type	Description
S_X	5	r	**Receive Sa6-Bit Status_X** If none of the fixed Sa6-bit combinations are detected this bit is set.
S_F	4	r	**Receive Sa6-Bit Status: "1111"** Receive Sa6-bit status “1111” is detected for three times in a row in the Sa6-bit positions.
S_E	3	r	**Receive Sa6-Bit Status: "1110"** Receive Sa6-bit status “1110” is detected for three times in a row in the Sa6-bit positions.
S_C	2	r	**Receive Sa6-Bit Status: "1100"** Receive Sa6-bit status “1100” is detected for three times in a row in the Sa6bit positions.
S_A	1	r	**Receive Sa6-Bit Status: "1010"** Receive Sa6-bit status “1010” is detected for three times in a row in the Sa6-bit positions.
S_8	0	r	**Receive Sa6-Bit Status: "1000"** Receive Sa6-bit status “1000” is detected for three times in a row in the Sa6-bit positions.

Receive Signaling Pointer 1

RSP1_E	Offset	Reset Value
Receive Signaling Pointer 1	$xx62_H$	00_H

7	6	5	4	3	2	1	0
RS8C	RS7C	RS6C	RS5C	RS4C	RS3C	RS2C	RS1C
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RS8C	7	r	**Receive Signaling Register RS(8:1) Changed** A one in each bit position indicates that the received signaling data in the corresponding RS(8:1) registers are updated. Bit RS1C is the pointer for register RS1, while RS8C points to RS8.
RS7C	6		
RS6C	5		
RS5C	4		
RS4C	3		
RS3C	2		
RS2C	1		
RS1C	0		

Receive Signaling Pointer 2

RSP2_E	Offset	Reset Value
Receive Signaling Pointer 2	$xx63_H$	00_H

7	6	5	4	3	2	1	0
RS16C	RS15C	RS14C	RS13C	RS12C	RS11C	RS10C	RS9C
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RS16C	7	r	**Receive Signaling Register RS9-16 Changed** A one in each bit position indicates that the received signaling data in the corresponding RS9-16 registers are updated. Bit RS9C is the pointer for register RS9, while RS16C points to RS16.
RS15C	6		
RS14C	5		
RS13C	4		
RS12C	3		
RS11C	2		
RS10C	1		
RS9C	0		

Signaling Status Register

SIS_E	Offset	Reset Value
Signaling Status Register	$xx64_H$	xx_H

7	6	5	4	3	2	1	0
XDOV	**XFW**	**XREP**	Res	**RLI**	**CEC**	**SFS**	Res
r	r	r		r	r	r	

Field	Bits	Type	Description
XDOV	7	r	**Transmit Data Overflow - HDLC Channel 1** More than 64 bytes have been written to the XFIFO. See also **Table 10**. This bit is cleared either • By a transmitter reset command XRES • When all bytes in the accessible half of the XFIFO have been moved in the inaccessible half (shadow register). 0_B , normal FIFO operation. 1_B , number of bytes written to the FIFO exceeds the FIFO size.
XFW	6	r	**Transmit FIFO Write Enable - HDLC Channel 1** Data can be written to the XFIFO.
XREP	5	r	**Transmission Repeat - HDLC Channel 1** Status indication of CMDR.XREP.
RLI	3	r	**Receive Line Inactive - HDLC Channel 1** Neither flags as interframe time fill nor frames are received through the signaling time slot.
CEC	2	r	**Command Executing - HDLC Channel 1** *Note: CEC is active for about 2.5 periods of the current system data rate.* 0_B , No command is currently executed, the CMDR register can be written to. 1_B , A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.
SFS	1	r	**Status Freeze Signaling** 0_B , Freeze signaling status inactive. 1_B , Freeze signaling status active.

Receive Signaling Status Register

RSIS relates to the last received HDLC frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

RSIS_E	Offset	Reset Value
Receive Signaling Status Register	$xx65_H$	xx_H

7	6	5	4	3	2	1	0
VFR	RDO	CRC16	RAB	HA		Res	LA
r	r	r	r	r			r

Field	Bits	Type	Description
VFR	7	r	**Valid Frame - HDLC Channel 1** Determines whether a valid frame has been received. An invalid frame is either • A frame which is not an integer number of 8-bits (nx8 bits) in length (e.g. 25 bits), or • A frame which is too short taking into account the operation mode selected by MODE (MDS(2:0)) and the selection of receive CRC on/off (CCR2.RCRC) as follows: MDS(2:0) = ´011_b´ (16-bit Address), RCRC = ´0´: 4 bytes; RCRC = ´1´: 3 or 4 bytes and MDS(2:0) = ´010_b´ (8-bit Address), RCRC = ´0´: 3 bytes; RCRC = 1, 2 or 3 bytes *Note: Shorter frames are not reported.* 1_B , Valid 0_B , Invalid
RDO	6	r	**Receive Data Overflow - HDLC Channel 1** A RFIFO data overflow has occurred during reception of the frame. Additionally, an interrupt can be generated (refer to ISR1.RDO/IMR1.RDO).
CRC16	5	r	**CRC16 Compare/Check - HDLC Channel 1** 0_B , CRC check failed; received frame contains errors. 1_B , CRC check o.k.; received frame is error-free.
RAB	4	r	**Receive Message Aborted - HDLC Channel 1** The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.This bit is set in SS7 mode, if the maximum number of octets (272+7) is exceeded.

Field	Bits	Type	Description
HA	3:2	r	**High Byte Address Compare - HDLC Channel 1** Significant only if 2-byte address mode or SS7 mode has been selected.In operating modes which provide high byte address recognition, the QuadFALC® compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FEH and FCH (broadcast address). Depending on the result of this comparison, the following bit combinations are possible (SS7 support not active): see table **HA Constant Values (Case 1)** **Notes** 1. *If RAH1, RAH2 contain identical values, a match is indicated by "10" or "11".* 2. *If Signaling System 7 support is activated (see MODE register), the bit functions are defined as follows: see table **HA Constant Values (Case 2)***
LA	0	r	**Low Byte Address Compare - HDLC Channel 1** Significant in HDLC modes only. The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared to two registers. (RAL1, RAL2). 0_B , RAL2 has been recognized 1_B , RAL1 has been recognized

Table 94 HA Constant Values (Case 1)

Name and Description	Value
High Byte Address Compare, SS7 support not active) RAH2 has been recognized	00_B
High Byte Address Compare, SS7 support not active) Broadcast address has been recognized	01_B
High Byte Address Compare, SS7 support not active) RAH1 has been recognized C/R = ´0´ (bit 1)	10_B
High Byte Address Compare, SS7 support not active) RAH1 has been recognized C/R = ´1´ (bit 1)	11_B

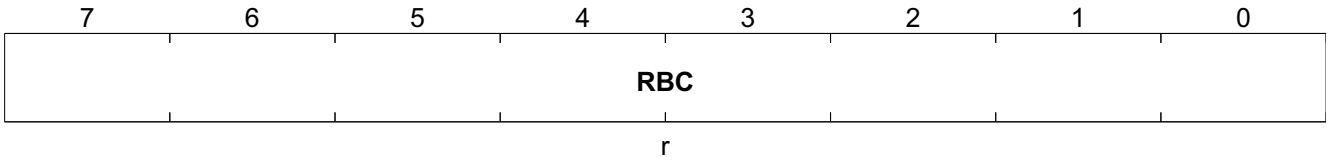
Table 95 HA Constant Values (Case 2)

Name and Description	Value
High Byte Address Compare, SS7 support active) Not valid	00_B
High Byte Address Compare, SS7 support active) Fill in signaling unit (FISU) detected	01_B
High Byte Address Compare, SS7 support active) Link status signaling unit (LSSU) detected	10_B
High Byte Address Compare, SS7 support active) Message signaling unit (MSU) detected	11_B

Receive Byte Count Low - HDLC Channel 1

Together with RBCH, bits RBC(11:8), indicates the length of a received frame (1 to 4095 bytes). Bits RBC(4:0) indicate the number of valid bytes currently in RFIFO. These registers must be read by the external micro controller following a RME interrupt.

RBCL_E	Offset	Reset Value
Receive Byte Count Low - HDLC Channel 1	$xx66_H$	00_H



Field	Bits	Type	Description
RBC	7:0	r	**Receive Byte Count - HDLC Channel 1 (least significant bits)** Together with RBCH(3:0), bits RBCL(7:0) indicates the length of the received frame.

Received Byte Count High - HDLC Channel 1

RBCH_E	Offset	Reset Value
Received Byte Count High - HDLC Channel 1	67_H	00_H

7	6	5	4	3	2	1	0
Res			**OV**	**RBC11**	**RBC10**	**RBC9**	**RBC8**
			r	r	r	r	r

Field	Bits	Type	Description
OV	4	r	**Counter Overflow - HDLC Channel 1** More than 4095 bytes received.
RBC11	3	r	**Receive Byte Count - HDLC Channel 1 (most significant bits)** Together with RBCL(7:0), bits RBCH(3:0) indicates the length of the received frame.
RBC10	2		
RBC9	1		
RBC8	0		

Interrupt Status Register 0

All bits are reset when ISR0 is read. If bit GCR.VIS is set, interrupt statuses in ISR0 are flagged although they are masked by register IMR0. However, these masked interrupt stati neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS, see Chapter 3.4.4.

ISR0_E	Offset	Reset Value
Interrupt Status Register 0	$xx68_H$	00_H

7	6	5	4	3	2	1	0
RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
RME	7	rsc	**Receive Message End - HDLC Channel 1** One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte. The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC(4:0). Additional information is available in the RSIS register.
RFS	6	rsc	**Receive Frame Start - HDLC Channel 1** This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS interrupt, the contents of • RAL1 • RSIS bits 3 to 1 are valid and can be read by the external micro controller.
T8MS	5	rsc	**Receive Time Out 8 ms** Only active if multiframing is enabled. The framer has found the double framing (basic framing) FRS0.LFA = ´0´ and is searching for the multiframing. This interrupt is set to indicate that no multiframing was found within a time window of 8 ms. In multiframe synchronous state this interrupt is not generated. Refer also to floating multiframe alignment window.
RMB	4	rsc	**Receive Multiframe Begin** This bit is set with the beginning of a received CRC multiframe related to the internal receive line timing. In CRC multiframe format FMR2.RFS1 = ´1´ or in doubleframe format FMR2.RFS(1:0) = ´01_b´ this interrupt occurs every 2 ms. If FMR2.RFS(1:0) = ´00_b´ this interrupt is generated every doubleframe (512 bits).

Field	Bits	Type	Description
CASC	3	rsc	**Received CAS Information Changed** This bit is set with the updating of a received CAS multiframe information in the registers RS(16:1). If the last received CAS information is different to the previous received one, this interrupt is generated after update has been completed. This interrupt only occurs only in TS0 and TS16 synchronous state. The registers RS(16:1) should be read within the next 2 ms otherwise the contents is lost.
CRC4	2	rsc	**Receive CRC4 Error** 0_B , No CRC4 error occurs. 1_B , The CRC4 check of the last received submultiframe failed.
SA6SC	1	rsc	**Receive Sa6-Bit Status Changed** With every change of state of the received Sa6-bit combinations this interrupt is set.
RPF	0	rsc	**Receive Pool Full** 32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

Interrupt Status Register 1

All bits are reset when ISR1 is read. If bit GCR.VIS is set, interrupt statuses in ISR1 are flagged although they are masked by register IMR1. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS, see **Chapter 3.4.4**.

ISR1_E	Offset	Reset Value
Interrupt Status Register 1	**xx69$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
LLBSC	**RDO**	**ALLS**	**XDU**	**XMB**	**SUEX**	**XLSC**	**XPR**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
LLBSC	7	rsc	**Line Loop-Back Status Change** Depending on bit LCR1.EPRM the source of this interrupt status changed: • LCR1.EPRM = 0: This bit is set, if the LLB activate signal or the LLB deactivate signal, respectively, is detected over a period of 25 ms with a bit error rate less than 10^{-2}. The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 10^{-2}. The actual detection status can be read from the RSP.LLBAD and RSP.LLBDD, respectively. • PRBS Status Change LCR1.EPRM = ´1´: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in RSP.LLBAD.
RDO	6	rsc	**Receive Data Overflow - HDLC Channel 1** This interrupt status indicates that the external micro controller did not respond fast enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again. *Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.*
ALLS	5	rsc	**All Sent - HDLC Channel 1** This bit is set if the last bit of the current frame has been sent completely and XFIFO is empty. This bit is valid in HDLC mode only.
XDU	4	rsc	**Transmit Data Underrun - HDLC Channel 1** Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued. *Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU should not be masked by register IMR1. Additionally, CMDR.SRES must be set after XDU occurs to reset the signalling transmitter.*

Field	Bits	Type	Description
XMB	3	rsc	**Transmit Multiframe Begin** This bit is set every 2 ms with the beginning of a transmitted multiframe related to the internal transmit line interface timing. Just before setting this bit registers XS(16:1) are copied in the transmit shift registers. The registers XS(16:1) are empty and has to be updated otherwise the contents is retransmitted.
SUEX	2	rsc	**Signaling Unit Error Threshold Exceeded - HDLC Channel 1** Masks the indication by interrupt that the selected error threshold for SS7 signaling units has been exceeded. *Note: SUEX is only valid, if SS7 mode is selected. If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).* 0_B , Signaling unit error count below selected threshold 1_B , Signaling unit error count exceeded selected threshold
XLSC	1	rsc	**Transmit Line Status Change** XLSC is set with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS. The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.
XPR	0	rsc	**Transmit Pool Ready - HDLC Channel 1** A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2

All bits are reset when ISR2 is read. If bit GCR.VIS is set, interrupt statuses in ISR2 are flagged although they are masked by register IMR2. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS, see Chapter 3.4.4.

ISR2_E	Offset	Reset Value
Interrupt Status Register 2	$xx6A_H$	00_H

7	6	5	4	3	2	1	0
FAR	**LFA**	**MFAR**	**T400MS**	**AIS**	**LOS**	**RAR**	**RA**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
FAR	7	rsc	**Frame Alignment Recovery** The framer has reached doubleframe synchronization. Set when bit FRS0.LFA is reset. It is set also after alarm simulation is finished and the receiver is still synchronous.
LFA	6	rsc	**Loss of Frame Alignment** The framer has lost synchronization and bit FRS0.LFA is set. It is set during alarm simulation.
MFAR	5	rsc	**Multiframe Alignment Recovery** Set when the framer has found two CRC-multiframes at an interval of n x 2 ms (n = 1, 2, 3, and so forth) without a framing error. At the same time bit FRS0.LMFA is reset.It is set also after alarm simulation is finished and the receiver is still synchronous. Only active if CRC-multiframe format is selected.
T400MS	4	rsc	**Receive Time Out 400 ms** Only active if multiframing is enabled. The framer has found the doubleframes (basic framing) FRS0.LFA = ´0´ and is searching for the multiframing. This interrupt is set to indicate that no multiframing was found within a time window of 400 ms after basic framing has been achieved. In multiframe synchronous state this interrupt is not generated.
AIS	3	rsc	**Alarm Indication Signal** This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. It is set during alarm simulation.If GCR.SCI is set high this interrupt status bit is set with every change of state of FRS0.AIS.
LOS	2	rsc	**Loss-of-Signal** This bit is set when a loss-of-signal alarm is detected in the received bit stream and FRS0.LOS is set. It is set during alarm simulation.If GCR.SCI is set high this interrupt status bit is set with every change of state of FRS0.LOS.
RAR	1	rsc	**Remote Alarm Recovery** Set if a remote alarm in TS0 is cleared and bit FRS0.RRA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

Field	Bits	Type	Description
RA	0	rsc	**Remote Alarm** Set if a remote alarm in TS0 is detected and bit FRS0.RRA is set. It is set during alarm simulation.

Interrupt Status Register 3

All bits are reset when ISR3 is read. If bit GCR.VIS is set, interrupt statuses in ISR3 are flagged although they are masked by register IMR3. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS, see **Chapter 3.4.4**.

ISR3_E	Offset	Reset Value
Interrupt Status Register 3	$xx6B_H$	00_H

7	6	5	4	3	2	1	0
ES	**SEC**	**LMFA16**	**AIS16**	**RA16**	**LTC**	**RSN**	**RSP**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rcs

Field	Bits	Type	Description
ES	7	rsc	**Errored Second** This bit is set if at least one enabled interrupt source by ESM is set during the time interval of one second. Interrupt sources of ESM register: • LFA = Loss of frame alignment detected (FRS0.LFA) • FER = Framing error received • CER = CRC error received • Alarm indication signal (FRS0.AIS) • Loss-of-signal (FRS0.LOS) • Code violation detected • Receive Slip positive/negative detected • E-Bit error detected (RSP.RS13/15)
SEC	6	rsc	**Second Timer** The internal one-second timer has expired. The timer is derived from clock RCLK or external pin SEC/FSC.
LMFA16	5	rsc	**Loss of Multiframe Alignment TS 16** Multiframe alignment of time slot 16 has been lost if two consecutive multiframe pattern are not detected or if in 16 consecutive time slot 16 all bits are reset.If register GCR.SCI is high this interrupt status bit is set with every change of state of FRS1.TS16LFA.
AIS16	4	rsc	**Alarm Indication Signal TS 16 Status Change** The alarm indication signal AIS in time slot 16 for the 64 kbit/s channel associated signaling is detected or cleared. A change in bit FRS1.TS16AIS sets this interrupt. (This bit is set if the incoming TS 16 signal contains less than 4 zeros in each of two consecutive TS16-multiframe periods.)
RA16	3	rsc	**Remote Alarm Time Slot 16 Status Change** A change in the remote alarm bit in CAS multiframe alignment word is detected.
LTC	2	rsc	**Loss of Transmit Clock** Transmit clock TCLK has been lost. Transmit clock switching is performed if CMR6.ATCS = ´1´, see **Chapter 3.7.3**. *Note: The actual status of TCLK is shown in the status bit CLKSTAT.TCLKLOS, see **CLKSTAT_E**.*

Field	Bits	Type	Description
RSN	1	rsc	**Receive Slip Negative** The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is skipped. It is set during alarm simulation. See **Chapter 4.1.7**.
RSP	0	rcs	**Receive Slip Positive** The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is repeated. It is set during alarm simulation. See **Chapter 4.1.7**.

Interrupt Status Register 4

All bits are reset when ISR4 is read. If bit GCR.VIS is set, interrupt statuses in ISR4 are flagged although they are masked by register IMR4. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS, see Chapter 3.4.4.

ISR4_E	Offset	Reset Value
Interrupt Status Register 4	$xx6C_H$	00_H

7	6	5	4	3	2	1	0
XSP	**XSN**	**RME2**	**RFS2**	**RDO2**	**ALLS2**	**XDU2**	**RPF2**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
XSP	7	rsc	**Transmit Slip Positive** The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is repeated. After a slip has performed writing of register XC1 is not necessary.
XSN	6	rsc	**Transmit Slip Negative** The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is skipped. After a slip has performed writing of register XC1 is not necessary.
RME2	5	rsc	**Receive Message End - HDLC Channel 2** One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO2, including the status byte. The complete message length can be determined reading register RBC2, the number of bytes currently stored in RFIFO2 is given by RBC2(6:0). Additional information is available in register RSIS2. 0_B , message receive in progress on HDLC channel 2. 1_B , one complete message has been stored in RFIFO2.
RFS2	4	rsc	**Receive Frame Start - HDLC Channel 2** This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS2 interrupt, the contents of • RAL1 • RSIS2 bits 3 to 1 are valid and can be read by the external micro controller. 0_B , no frame start has been detected on HDLC channel 2. 1_B , a frame start has been detected on HDLC channel 2, RAL1 and RSIS2(3:1) are valid.

Field	Bits	Type	Description
RDO2	3	rsc	**Receive Data Overflow - HDLC Channel 2** This interrupt status indicates that the external micro controller did not respond fast enough to an RPF2 or RME2 interrupt and that data in RFIFO2 has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO2 is available again. *Note: Whereas the bit RSIS2.RDO2 in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO2, the ISR4.RDO2 interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.* 0_B , no receive data overflow has been detected on HDLC channel 2. 1_B , a receive data overflow has been detected on HDLC channel 2.
ALLS2	2	rsc	**All Sent - HDLC Channel 2** This bit is set if the last bit of the current frame has been sent completely and XFIFO2 is empty. This bit is valid in HDLC mode only. 0_B , data transmission is in progress on HDLC channel 2. 1_B , data transmission is idle on HDLC channel 2, XFIFO2 is empty.
XDU2	1	rsc	**Transmit Data Underrun - HDLC Channel 2** Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO2 and no XME2 was issued. *Note: Transmitter and XFIFO2 are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU2 should not be masked via register IMR4. Additionally, CMDR3.SRES2 must be set after XDU occurs to reset the signaling transmitter.* 0_B , data transmission is in progress on HDLC channel 2. 1_B , data transmission has been stopped due to data underrun on HDLC channel 2.
RPF2	0	rsc	**Receive Pool Full - HDLC Channel 2** 32 bytes of a frame have arrived in the receive FIFO2. The frame is not yet completely received. 0_B , data reception is in progress on HDLC channel 2. 1_B , data has been stored in RFIFO2 and can be read.

Interrupt Status Register 5

All bits are reset when ISR5 is read. If bit GCR.VIS is set, interrupt statuses in ISR5 are flagged although they are masked via register IMR5. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS, see **Chapter 3.4.4**.

ISR5_E	Offset	Reset Value
Interrupt Status Register 5	**xx6D$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
XPR2	**XPR3**	**RME3**	**RFS3**	**RDO3**	**ALLS3**	**XDU3**	**RPF3**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
XPR2	7	rsc	**Transmit Pool Ready - HDLC Channel 2** A data block of up to 32 bytes can be written to the transmit FIFO2. XPR2 enables the fastest access to XFIFO2. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags. 0_B , message transmission in progress on HDLC channel 2, XFIFO2 is busy. 1_B , XFIFO2 is ready to receive data.
XPR3	6	rsc	**Transmit Pool Ready - HDLC Channel 3** A data block of up to 32 bytes can be written to the transmit FIFO3. XPR3 enables the fastest access to XFIFO3. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags. 0_B , message transmission in progress on HDLC channel 3, XFIFO32 is busy. 1_B , XFIFO3 is ready to receive data.
RME3	5	rsc	**Receive Message End - HDLC Channel 3** One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO3, including the status byte. The complete message length can be determined reading register RBC3, the number of bytes currently stored in RFIFO3 is given by RBC3(6:0). Additional information is available in register RSIS3. 0_B , message receive in progress on HDLC channel 3. 1_B , one complete message has been stored in RFIFO3.

Field	Bits	Type	Description
RFS3	4	rsc	**Receive Frame Start - HDLC Channel 3** This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS2 interrupt, the contents of • RAL1 • RSIS3 bits 3 to 1 are valid and can be read by the external micro controller. 0_B , no frame start has been detected on HDLC channel 3. 1_B , a frame start has been detected on HDLC channel 3, RAL1 and RSIS3(3:1) are valid.
RDO3	3	rsc	**Receive Data Overflow - HDLC Channel 3** This interrupt status indicates that the external micro controller did not respond fast enough to an RPF3 or RME3 interrupt and that data in RFIFO3 has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO3 is available again. *Note: Whereas the bit RSIS3.RDO3 in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO3, the ISR5.RDO3 interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.* 0_B , no receive data overflow has been detected on HDLC channel 3. 1_B , a receive data overflow has been detected on HDLC channel 3.
ALLS3	2	rsc	**All Sent - HDLC Channel 3** This bit is set if the last bit of the current frame has been sent completely and XFIFO3 is empty. This bit is valid in HDLC mode only. 0_B , data transmission is in progress on HDLC channel 3. 1_B , data transmission is idle on HDLC channel 3, XFIFO3 is empty.
XDU3	1	rsc	**Transmit Data Underrun - HDLC Channel 3** Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO3 and no XME3 was issued. *Note: Transmitter and XFIFO3 are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU3 should not be masked via register IMR5. Additionally, CMDR4.SRES3 must be set after XDU occurs to reset the signaling transmitter.* 0_B , data transmission is in progress on HDLC channel 3. 1_B , data transmission has been stopped due to data underrun on HDLC channel 3.
RPF3	0	rsc	**Receive Pool Full - HDLC Channel 3** 32 bytes of a frame have arrived in the receive FIFO3. The frame is not yet completely received. 0_B , data reception is in progress on HDLC channel 3. 1_B , data has been stored in RFIFO3 and can be read.

Global Interrupt Status Register

This status register points to pending interrupts sourced by ISR(7:0), see Chapter 3.4.4.

GIS_E	Offset	Reset Value
Global Interrupt Status Register	$xx6E_H$	00_H

7	6	5	4	3	2	1	0
ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
ISR7	7	rsc	**Interrupt Status Register 7 Pointer** 0_B , no interrupt is pending in ISR6. 1_B , at least one interrupt is pending in ISR6.
ISR6	6	rsc	**Interrupt Status Register 6 Pointer** 0_B , no interrupt is pending in ISR6. 1_B , at least one interrupt is pending in ISR6.
ISR5	5	rsc	**Interrupt Status Register 5 Pointer** 0_B , no interrupt is pending in ISR5. 1_B , at least one interrupt is pending in ISR5.
ISR4	4	rsc	**Interrupt Status Register 4 Pointer** 0_B , no interrupt is pending in ISR4. 1_B , at least one interrupt is pending in ISR4.
ISR3	3	rsc	**Interrupt Status Register 3 Pointer** 0_B , no interrupt is pending in ISR3. 1_B , at least one interrupt is pending in ISR3.
ISR2	2	rsc	**Interrupt Status Register 2 Pointer** 0_B , no interrupt is pending in ISR2. 1_B , at least one interrupt is pending in ISR2.
ISR1	1	rsc	**Interrupt Status Register 1 Pointer** 0_B , no interrupt is pending in ISR1. 1_B , at least one interrupt is pending in ISR1.
ISR0	0	rsc	**Interrupt Status Register 0 Pointer** 0_B , no interrupt is pending in ISR0. 1_B , at least one interrupt is pending in ISR0.

Channel Interrupt Status Register

This status register points to pending interrupts of channels 1to 8, see **Chapter 3.4.4**.

CIS_E	Offset	Reset Value
Channel Interrupt Status Register	$006F_H$	00_H

7	6	5	4	3	2	1	0
GIS8_PLLLS	GIS7	GIS6	GIS5	GIS4	GIS3	GIS2	GIS1
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
GIS8_PLLLS	7	rsc	**GIS 8: Global Interrupt Status of Channel 8** *Note: Different function of this bit: PLLLS if COMP = ´1´; GIS 8 if COMP = ´0´ , see **Figure 17** and **Figure 18**.* 0_B , no interrupt is pending on channel 8. 1_B , at least one interrupt is pending on channel 8, read GIS of channel 8 for more information. **PLLLS: PLL Lock Status** This bit shows the lock status of the internal PLL. *Note: PLLLS only if COMP = ´1´. PLLLS (for COMP = ´1´) has the same value as PLLLS in register GIS2 (which is used for COMP = ´0´). For both pseudo QuadFALCs (if COMP = ´1´) PLLLS has the same value.* 0_B , PLL is unlocked. 1_B , PLL is locked.
GIS7	6	rsc	**Global Interrupt Status of Channel 7** *Note: Only if COMP = ´0´, see **Figure 18**.* 0_B , no interrupt is pending on channel 7. 1_B , at least one interrupt is pending on channel 7, read GIS of channel 7 for more information.
GIS6	5	rsc	**Global Interrupt Status of Channel 6** *Note: Only if COMP = ´0´, see **Figure 18**.* 0_B , no interrupt is pending on channel 6. 1_B , at least one interrupt is pending on channel 6, read GIS of channel 6 for more information.

Field	Bits	Type	Description
GIS5	4	rsc	**Global Interrupt Status of Channel 5** *Note: Only if COMP = ´0´, see Figure 18.* 0_B , no interrupt is pending on channel 5. 1_B , at least one interrupt is pending on channel 5, read GIS of channel 5 for more information.
GIS4	3	rsc	**Global Interrupt Status of Channel 4** 0_B , no interrupt is pending on channel 4. 1_B , at least one interrupt is pending on channel 4, read GIS of channel 4 for more information.
GIS3	2	rsc	**Global Interrupt Status of Channel 3** 0_B , no interrupt is pending on channel 3. 1_B , at least one interrupt is pending on channel 3, read GIS of channel 3 for more information.
GIS2	1	rsc	**Global Interrupt Status of Channel 2** 0_B , no interrupt is pending on channel 2. 1_B , at least one interrupt is pending on channel 2, read GIS of channel 2 for more information.
GIS1	0	rsc	**Global Interrupt Status of Channel 1** 0_B , no interrupt is pending on channel 1. 1_B , at least one interrupt is pending on channel 1, read GIS of channel 1 for more information.

Receive CAS Register 1

Each register except RS1 contains the received CAS bits for two time slots, see **Chapter 4.3.5.3**. The received CAS multiframe is compared to the previously received one. If the contents changed a CAS multiframe changed interrupt (ISR0.CASC) is generated and informs the user that a new multiframe has to be read within the next 2 ms. If requests for reading the RS(16:1) register are ignored, the received data is lost. RS1 contains frame 0 of the CAS multiframe. MSB is received first.

Additionally a receive signaling data change pointer indicates an update of register RS(16:1). Refer also to register RSP(2:1). Access to RS(16:1) registers is only valid if the serial receive signaling access on the system highway is disabled.

RS1_E	Offset	Reset Value
Receive CAS Register 1	$xx70_H$	xx_H

7	6	5	4	3	2	1	0
0				X1	Y1	X2	Y2
r				r	r	r	r

Field	Bits	Type	Description
0	7:4	r	**Receive CAS bits**
X1	3	r	
Y1	2	r	
X2	1	r	
Y2	0	r	

Receive CAS Register 2

See description of **Receive CAS Register 1**

RS2_E	Offset	Reset Value
Receive CAS Register 2	**xx71$_H$**	**xx$_H$**

7	6	5	4	3	2	1	0
A1	**B1**	**C1**	**D1**	**A16**	**B16**	**C16**	**D16**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
A1	7	r	**Receive CAS bits**
B1	6		
C1	5		
D1	4		
A16	3		
B16	2		
C16	1		
D16	0		

Similar Registers

Registers RS3 to RS16 have the same layout and description.

The Offset Addresses are listed in **RSn Overview**, for bit names refer to **Receive CAS Registers**.

Table 96 RSn Overview

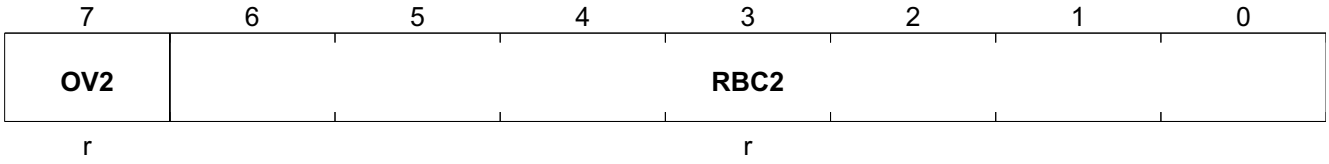
Register Short Name	Register Long Name	Offset Address	Page Number
RS3	Receive CAS Register 3	72$_H$	
RS4	Receive CAS Register 4	73$_H$	
RS5	Receive CAS Register 5	74$_H$	
RS6	Receive CAS Register 6	75$_H$	
RS7	Receive CAS Register 7	76$_H$	
RS8	Receive CAS Register 8	77$_H$	
RS9	Receive CAS Register 9	78$_H$	
RS10	Receive CAS Register 10	79$_H$	
RS11	Receive CAS Register 11	7A$_H$	
RS12	Receive CAS Register 12	7B$_H$	
RS13	Receive CAS Register 13	7C$_H$	
RS14	Receive CAS Register 14	7D$_H$	
RS15	Receive CAS Register 15	7E$_H$	
RS16	Receive CAS Register 16	7F$_H$	

Table 97 Receive CAS Registers

	7	6	5	4	3	2	1	0
RS1	0	0	0	0	X1	Y	X2	X2
RS2	A1	B1	C1	D1	A16	B16	C16	D16
RS3	A2	B2	C2	D2	A17	B17	C17	D17
RS4	A3	B3	C3	D3	A18	B18	C18	D18
RS5	A4	B4	C4	D4	A19	B19	C19	D19
RS6	A5	B5	C5	D5	A20	B20	C20	D20
RS7	A6	B6	C6	D6	A21	B21	C21	D21
RS8	A7	B7	C7	D7	A22	B22	C22	D22
RS9	A8	B8	C8	D8	A23	B23	C23	D23
RS10	A9	B9	C9	D9	A24	B24	C24	D24
RS11	A10	B10	C10	D10	A25	B25	C25	D25
RS12	A11	B11	C11	D11	A26	B26	C26	D26
RS13	A12	B12	C12	D12	A27	B27	C27	D27
RS14	A13	B13	C13	D13	A28	B28	C28	D28
RS15	A14	B14	C14	D14	A29	B29	C29	D29
RS16	A15	B15	C15	D15	A30	B30	C30	D30

Receive Byte Count Register 2

RBC2_E	Offset	Reset Value
Receive Byte Count Register 2	90_H	00_H



Field	Bits	Type	Description
OV2	7	r	**Counter Overflow - HDLC Channel 2** 0_B , Less than or equal to 128 bytes received 1_B , More than 128 bytes received
RBC2	6:0	r	**Receive Byte Count - HDLC Channel 2** Indicates the length of a received frame.

Receive Byte Count Register 3

RBC3_E	Offset	Reset Value
Receive Byte Count Register 3	$xx91_H$	00_H

7	6	5	4	3	2	1	0
OV3	RBC3						
r	r						

Field	Bits	Type	Description
OV3	7	r	**Counter Overflow - HDLC Channel 3** 0_B , Less than or equal to 128 bytes received 1_B , More than 128 bytes received
RBC3	6:0	r	**Receive Byte Count - HDLC Channel 3** Indicates the length of a received frame.

Signaling Status Register 3

SIS3_E	Offset	Reset Value
Signaling Status Register 3	$xx9A_H$	00_H

7	6	5	4	3	2	1	0
XDOV3	**XFW3**	**XREP3**	Res	**RLI3**	**CEC3**	Res	
r	r	r		r	r		

Field	Bits	Type	Description
XDOV3	7	r	**Transmit Data Overflow - HDLC Channel 3** More than 32 bytes (if CCR4.RFT23 = ´0´) or 64 bytes (if CCR4.RFT23 = ´1´) have been written to the XFIFO. See also **Chapter 3.4.3**. This bit is cleared either • By a transmitter reset command XRES • When all bytes in the accessible half of the XFIFO have been moved in the inaccessible half (shadow register). 0_B , normal FIFO operation. 1_B , number of bytes written to the FIFO exceeds the FIFO size.
XFW3	6	r	**Transmit FIFO Write Enable - HDLC Channel 3** 0_B , FIFO is not ready, don't write to FIFO. 1_B , FIFO is ready to accept data.
XREP3	5	r	**Transmission Repeat - HDLC Channel 3** 0_B , no repeated transmission in progress. 1_B , repeated transmission in progress.
RLI3	3	r	**Receive Line Inactive - HDLC Channel 3** 0_B , HDLC data or interframe time fill are being received. 1_B , neither data nor flags as interframe time fill are received.
CEC3	2	r	**Command Executing - HDLC Channel 3** *Note: CEC3 will be active up to 2.5 periods of the current system data rate after a command has been written to CMDR4.* 0_B , No command is currently executed, the CMDR4 register can be written to. 1_B , A command (written previously to CMDR4) is currently executed, no further command can be temporarily written in CMDR4 register.

Receive Signaling Status Register 3

RSIS3 relates to the last received HDLC channel 3 frame; it is copied into RFIFO3 when end-of-frame is recognized (last byte of each stored frame).

RSIS3_E	Offset	Reset Value
Receive Signaling Status Register 3	$xx9B_H$	00_H

7	6	5	4	3	2	1	0
VFR3	**RDO3**	**CRC163**	**RAB3**	**HA13**	**HA03**	Res	**LA3**
rsc	rsc	rsc	rsc	rsc	rsc		rsc

Field	Bits	Type	Description
VFR3	7	rsc	**Valid Frame - HDLC Channel 3** Determines whether a valid frame has been received. An invalid frame is either • A frame which is not an integer number of 8 bits (nx8 bits) in length (e.g. 25 bits), or • A frame which is too short taking into account the operation mode selected via MODE3 (MDS3(2:0)) and the selection of receive CRC ON/OFF (CCR4.RCRC3) as follows: MDS3(2:0) = ´011_b´ (16-bit Address), RCRC3 = ´0´: 4 bytes; RCRC3 = ´1´: 3 or 4 bytes or MDS3(2:0) = ´010_b´ (8-bit Address), RCRC3 = ´0´: 3 bytes; RCRC3 = ´1´: 2 or 3 bytes *Note: Shorter frames are not reported.* 0_B , Received frame is invalid 1_B , Received frame is valid
RDO3	6	rsc	**Receive Data Overflow - HDLC Channel 3** A data overflow has occurred during reception of the frame.Additionally, an interrupt can be generated (refer to ISR5.RDO3/IMR5.RDO3). 0_B , normal receive operation. 1_B , data overflow has occurred during reception.
CRC163	5	rsc	**CRC16 Compare/Check - HDLC Channel 3** 0_B , CRC check failed; received frame contains errors. 1_B , CRC check o.k.; received frame is error-free.
RAB3	4	rsc	**Receive Message Aborted - HDLC Channel 3** This bit is set, if more than 5 contiguous 1-bits are detected. 0_B , data reception is in progress. 1_B , data reception has been aborted.

Field	Bits	Type	Description
HA13	3	rsc	**High Byte Address Compare - HDLC Channel 3** Significant only if 2-byte address mode is selected.In operating modes which provide high byte address recognition, the OctalFALCTM compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values ´FE_H´ and FC_H (broadcast address). Depending on the result of this comparison, the following bit combinations are possible: *Note: If RAH1, RAH2 contain identical values, a match is indicated by "10" or "11".* 00_B , RAH2 has been recognized 01_B , Broadcast address has been recognized 10_B , RAH1 has been recognized C/R = ´0´ (bit 1) 11_B , RAH1 has been recognized C/R = ´1´ (bit 1)
HA03	2		
LA3	0	rsc	**Low Byte Address Compare - HDLC Channel 3** Significant in HDLC modes only. The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2). 0_B , RAL2 has been recognized 1_B , RAL1 has been recognized

Receive FIFO 2 Lower Byte

RFIFO2L_E	Offset	Reset Value
Receive FIFO 2 Lower Byte	$xx9C_H$	xx_H

7	6	5	4	3	2	1	0
RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF7	7	r	**Receive FIFO - HDLC Channel 2** The function is equivalent to RFIFO1L of HDLC channel 1.
RF6	6	r	
RF5	5	r	
RF4	4	r	
RF3	3	r	
RF2	2	r	
RF1	1	r	
RF0	0	r	

Receive FIFO 2 Higher Byte

RFIFO2H_E	Offset	Reset Value
Receive FIFO 2 Higher Byte	$xx9D_H$	xx_H

7	6	5	4	3	2	1	0
RF15	**RF14**	**RF13**	**RF12**	**RF11**	**RF10**	**RF9**	**RF8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF15	7	r	**Receive FIFO - HDLC Channel 2** The function is equivalent to RFIFO1H of HDLC channel 1.
RF14	6	r	
RF13	5	r	
RF12	4	r	
RF11	3	r	
RF10	2	r	
RF9	1	r	
RF8	0	r	

Receive FIFO 3 Lower Byte

RFIFO3L_E	Offset	Reset Value
Receive FIFO 3 Lower Byte	$xx9E_H$	xx_H

7	6	5	4	3	2	1	0
RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF7	7	r	**Receive FIFO - HDLC Channel 3** The function is equivalent to RFIFO1L of HDLC channel 1.
RF6	6	r	
RF5	5	r	
RF4	4	r	
RF3	3	r	
RF2	2	r	
RF1	1	r	
RF0	0	r	

Receive FIFO 3 Higher Byte

RFIFO3H_E	Offset	Reset Value
Receive FIFO 3 Higher Byte	$xx9F_H$	xx_H

7	6	5	4	3	2	1	0
RF15	RF14	RF13	RF12	RF11	RF10	RF9	RF8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF15	7	r	**Receive FIFO - HDLC Channel 3** The function is equivalent to RFIFO1H of HDLC channel 1.
RF14	6	r	
RF13	5	r	
RF12	4	r	
RF11	3	r	
RF10	2	r	
RF9	1	r	
RF8	0	r	

Signaling Status Register 2

SIS2_E	Offset	Reset Value
Signaling Status Register 2	$xxA9_H$	00_H

7	6	5	4	3	2	1	0
XDOV2	**XFW2**	**XREP2**	Res	**RLI2**	**CEC2**	Res	
rsc	rsc	rsc		rsc	rsc		

Field	Bits	Type	Description
XDOV2	7	rsc	**Transmit Data Overflow - HDLC Channel 2** More than 32 bytes (if CCR3.RFT22 = ´0´) or 64 bytes (if CCR3.RFT22 = ´1´) have been written to the XFIFO.This bit is cleared either • By a transmitter reset command XRES or • When all bytes in the accessible half of the XFIFO have been moved in the inaccessible half (shadow register). 0_B , normal FIFO operation. 1_B , number of bytes written to the FIFO exceeds the FIFO size.
XFW2	6	rsc	**Transmit FIFO Write Enable - HDLC Channel 2** 0_B , FIFO is not ready, don't write to FIFO. 1_B , FIFO is ready to accept data.
XREP2	5	rsc	**Transmission Repeat - HDLC Channel 2** 0_B , no repeated transmission in progress. 1_B , repeated transmission is in progress.
RLI2	3	rsc	**Receive Line Inactive - HDLC Channel 2** 0_B , HDLC data or interframe time fill are being received. 1_B , neither data nor flags as interframe time fill are received.
CEC2	2	rsc	**Command Executing - HDLC Channel 2** *Note: CEC2 will be high for about 2.5 periods of the system data rate after a command has been written to CMDR3.* 0_B , no command is currently executing, CMDR3 can be written. 1_B , a command is in progress, don't write to CMDR3.

Receive Signaling Status Register 2

RSIS2_E	Offset	Reset Value
Receive Signaling Status Register 2	$xxAA_H$	00_H

7	6	5	4	3	2	1	0
VFR2	**RDO2**	**CRC162**	**RAB2**	**HA2**		Res	**LA2**
rsc	rsc	rsc	rsc	rsc			rsc

Field	Bits	Type	Description
VFR2	7	rsc	**Valid Frame - HDLC Channel 2** Indicates whether a valid frame has been received. An invalid frame is flagged if - the frame length is not an integer multiple of 8 bytes - the frame is too short (the lower limit depends on the selection of MODE2.MDS2 and CCR3.RCRC2). 1_B , received frame is invalid. 0_B , received frame is valid.
RDO2	6	rsc	**Receive Data Overflow - HDLC Channel 2** 0_B , normal receive operation. 1_B , data overflow has occurred during reception.
CRC162	5	rsc	**CRC16 Compare/Check - HDLC Channel 2** 0_B , CRC error check failed on the received frame. 1_B , received frame if free of CRC errors.
RAB2	4	rsc	**Receive Message Aborted- HDLC Channel 2** Message abortion is declared, if more than five contiguous ´1´ bits are received. 0_B , data reception is in progress. 1_B , data reception has been aborted.
HA2	3:2	rsc	**High Byte Address Compare - HDLC Channel 2** These bits are used in two-byte addressing mode only. In addressing modes using high byte recognition, the high byte of the received address is compared with two individually programmable registers (RAH1 and RAH2) as well as with the fixed values ´FE_H´ and ´FC_H´ (broadcast address). *Note: If RAH1 and RAH2 are set to identical values, a match is indicated by either “10” or “11”.* 00_B , RAH2 has been recognized. 01_B , broadcast address has been recognized. 10_B , RAH1 has been recognized, C/R = ´0´. 11_B , RAH1 has been recognized, C/R = ´1´.

Field	Bits	Type	Description
LA2	0	rsc	**Low Byte Address Compare - HDLC Channel 2** This bit is used in HDLC modes only. The low byte address of a two-byte address or a single-byte address are compared with two programmable values (RAL1 and RAL2). 1_B , received low address byte matches the value programmed to RAL2. 0_B , received low address byte matches the value programmed to RAL1.

Multi Function Port Input Register

This register always reflects the state of the multi function ports, see **Chapter 3.8**. If used as an input, the according port should be switched to general purpose input mode. If not, the programmed output signal can be monitored through this register (see registers PC1 to PC4).

MFPI_E	Offset	Reset Value
Multi Function Port Input Register	**$xxAB_H$**	**xx_H**

7	6	5	4	3	2	1	0
Res	**RPC**	**RPB**	**RPA**	Res		**XPB**	**XPA**
	r	r	r			r	r

Field	Bits	Type	Description
RPC	6	r	**RPC Input Level** 0_B , Low level on pin RPC. 1_B , High level on pin RPC.
RPB	5	r	**RPB Input Level** 0_B , Low level on pin RPB. 1_B , High level on pin RPB.
RPA	4	r	**RPA Input Level** 0_B , Low level on pin RPA. 1_B , High level on pin RPA.
XPB	1	r	**XPB Input Level** 0_B , Low level on pin XPB. 1_B , High level on pin XPB.
XPA	0	r	**XPA Input Level** 0_B , Low level on pin XPA. 1_B , High level on pin XPA.

Interrupt Status Register 6

For T1/J1: Note that detection of Out-Band Loop messages (BOM codes) is only possible either on the line side or the system side, dependent on the configuration of the HDLC/BOM controller 1: If the HDLC/BOM controller 1is attached to the line side (MODE.HDLCI = ´0´ for HDLC channel1) only BOM messages on the line side can be detected. If the HDLC/BOM controller 1 is attached to the system side (MODE.HDLCI = ´1´) only BOM messages on the system side can be detected, see also **Chapter 5.5.8**.

ISR6_E	Offset	Reset Value
Interrupt Status Register 6	$xxAC_H$	00_H

7	6	5	4	3	2	1	0
SOLSU	**SOLSD**	**LOLSU**	**LOLSD**	**SILSU**	**SILSD**	**LILSU**	**LILSD**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
SOLSU	7	rsc	**System Out-Band Loop Switching Up detected** Only for T1, see **Chapter 5.5.8**. System loop up code (payload loopback activate message) detected and payload loop is switched on if ALS.SOLS is set.
SOLSD	6	rsc	**System Out-Band Loop Switching Down detected** Only for T1, see **Chapter 5.5.8**. System loop down code (payload loopback deactivate message) detected and payload loop is switched off if ALS.SOLS is set.
LOLSU	5	rsc	**Line Out-Band Loop Switching Up detected** Only for T1, see **Chapter 5.5.8**. Line loop up code (line loopback activate message) detected and line loop is switched on if ALS.LOLS is set.
LOLSD	4	rsc	**Line Out-Band Loop Switching Down detected** Only for T1, see **Chapter 5.5.8**. Line loop down code (line loopback deactivate message) detected and line loop is switched off if ALS.LOLS is set.
SILSU	3	rsc	**System In-Band Loop Switching Up detected** See **Chapter 4.5.6**. System loop up code detected and payload loop is switched on if ALS.SILS is set.
SILSD	2	rsc	**System In-Band Loop Switching Down detected** See **Chapter 4.5.6**. System loop down code detected and payload loop is switched off if ALS.SILS is set.
LILSU	1	rsc	**Line In-Band Loop Switching Up Interrupt** See **Chapter 4.5.6**. Line loop up code detected and line loop is switched on if ALS.LILS is set.
LILSD	0	rsc	**Line In-Band Loop Switching Down Interrupt** See **Chapter 4.5.6**. Line loop down code detected and line loop is switched off if ALS.LILS is set.

Global Interrupt Status 2

Interrupt status register for the PLL of the master clocking unit.

GIS2_E	Offset	Reset Value
Global Interrupt Status 2	$00AD_H$	00_H

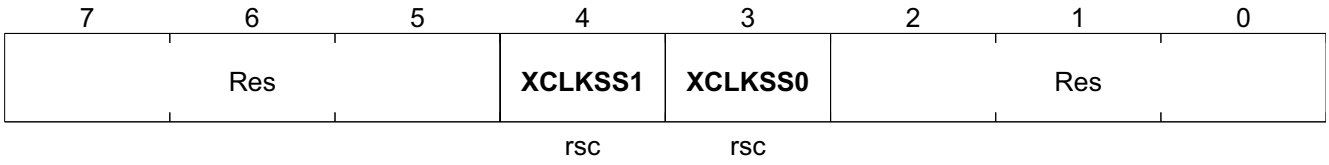
7	6	5	4	3	2	1	0
Res					PLLIC	PLLLS	PLLLC
					rsc	r	rsc

Field	Bits	Type	Description
PLLLS	1	r	**PLL Locked Status Information** *Note: PLLLS is only a status bit, not an interrupt status bit, so type is r and not rsc. This bit is valid independent on value of COMP. For COMP = ´0´ this bit must be used instead of bit 7 of register CIS which has then the function GIS8.* 0_B , PLL is unlocked. 1_B , PLL is locked
PLLLC	0	rsc	**PLL Locked Status Change** 0_B , no change of PLL lock status since last read of this register. 1_B , PLL lock status has changed since last read. Status information is available in bit PLLLS.

Interrupt Status Register 7

All bits are reset when ISR7 is read. If bit GCR.VIS is set, interrupt statuses in ISR7 are flagged although they are masked by register IMR7. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS, see **Chapter 3.4.4**.

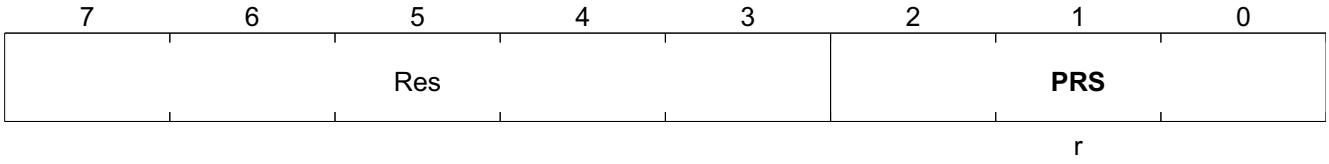
ISR7_E	Offset	Reset Value
Interrupt Status Register 7	**xxD8$_H$**	**00$_H$**



Field	Bits	Type	Description
XCLKSS1	4	rsc	**XCLK Source Switched 1** See **Chapter 3.7.3**. Shows if an automatically switching of the DCO-X reference between TCLK and SCLK was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in register **CLKSTAT_E**.
XCLKSS0	3	rsc	**XCLK Source Switched 0** See **Chapter 3.7.3**. Shows if an automatically switching of the XCLK source between TCLK and DCO-X output was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in register **CLKSTAT_E**.

PRBS Status Register

PRBSSTA_E	Offset	Reset Value
PRBS Status Register	$xxDA_H$	$0x_H$

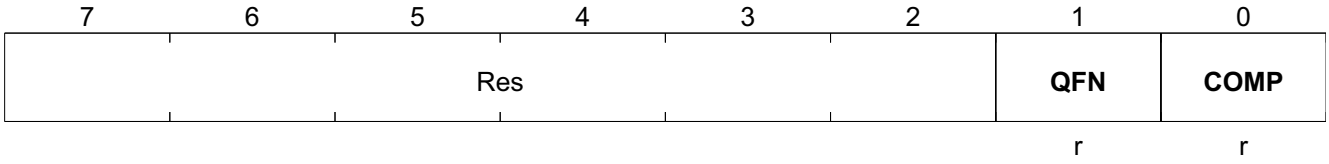


Field	Bits	Type	Description
PRS	2:0	r	**PRBS Status Information** *Note: Every change of the bits PRS sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected in case alarm simulation is performed by the device. Detection of all_zero or all_ones is done over 12, 16, 21 or 24 consecutive bits, dependent on the choosed PRBS polynomial (11, 15, 20 or 23). Because every bit error in the PRBS increments the bit error counter BEC, no special status information like “PRBS detected with errors” is given here.* 000_B , no pattern detected. 001_B , reserved. 010_B , PRBS pattern detected. 011_B , inverted PRBS pattern detected. 100_B , reserved. 101_B , reserved. 110_B , all-zero pattern detected. 111_B , all-ones pattern detected.

Device Status Register

See **Figure 96**.

DSTR_E	Offset	Reset Value
Device Status Register	$00E7_H$	$0x_H$



Field	Bits	Type	Description
QFN	1	r	**QuadFALC® Number** *Note: See **Figure 96** for more detail. This bit is valid only if COMP = ´1´.* 0_B , A10/CS2 is low (pseudo QuadFALC® #0 has been selected). 1_B , pseudo QuadFALC® #1 has been selected.
COMP	0	r	**COMP Input Signal Status** *Note: See **Figure 96** for more detail.* 0_B , COMP input signal is low, OctalFALC mode is selected. 1_B , COMP input signal is high, QuadFALC® compatibility mode is selected.

Clock Status Register

The bits show the current status of the input clocks TCLK and SCLKX.

CLKSTAT_E	Offset	Reset Value
Clock Status Register	$xxFE_H$	xx_H

7	6	5	4	3	2	1	0
Res			TCLKLOS	SCLKXLOS	Res		
			r	r			

Field	Bits	Type	Description
TCLKLOS	4	r	**Loss of TCLK** Status of TCLK. *Note: See **Chapter 3.7.3** for more detail.* 0_B , TCLK is active. 1_B , TCLK is lost.
SCLKXLOS	3	r	**Loss of SCLKX** Status of SCLKX. *Note: See **Chapter 3.7.3** for more detail.* 0_B , SCLKX is active. 1_B , SCLKX is lost.

8 T1/J1 Registers

After reset all control registers except the XFIFO and XS(12:1) are initialized to defined values.

Unused bits have to be cleared.

The address 0XF8 of the register RAMTEST3 is a global and not an offset address.

Table 98 Registers Address Space

Module	Base Address	End Address	Note
T1/J1 Registers	$xx00_H$	$_H$	xx = is the channel no. (0 to 7)

Table 99 Registers Overview T1/J1

Register Short Name	Register Long Name	Offset Address	Page Number
XFIFO1L_T	Transmit FIFO - HDLC Channel 1 Lower Byte	$xx00_H$	426
XFIFO1H_T	Transmit FIFO - HDLC Channel 1 - Higher Byte	$xx01_H$	427
CMDR_T	Command Register	$xx02_H$	428
MODE_T	Mode Register	$xx03_H$	430
RAH1_T	Receive Address Byte High Register 1	$xx04_H$	432
RAH2_T	Receive Address Byte High Register 2	$xx05_H$	433
RAL1_T	Receive Address Byte Low Register 1	$xx06_H$	434
RAL2_T	Receive Address Byte Low Register 2	$xx07_H$	435
CCR2_T	Common Configuration Register 2	$xx0A_H$	440
RTR1_T	Receive Time Slot Register 1	$xx0C_H$	441
TTR1_T	Transmit Time Slot Register 1	$xx10_H$	443
IMR0_T	Interrupt Mask Register 0	$xx14_H$	445
IERR_T	Single Bit Defect Insertion Register	$xx1B_H$	447
FMR0_T	Framer Mode Register 0	$xx1C_H$	448
FMR1_T	Framer Mode Register 1	$xx1D_H$	450
FMR2_T	Framer Mode Register 2	$xx1E_H$	453
LOOP_T	LOOP	$xx1F_H$	456
FMR4_T	Framer Mode Register 4	$xx20_H$	457
FMR5_T	Framer Mode Register 5	$xx21_H$	459
XC0_T	Transmit Control 0	$xx22_H$	461
XC1_T	Transmit Control 1	$xx23_H$	462
RC0_T	Receive Control 0	$xx24_H$	463
RC1_T	Receive Control 1	$xx25_H$	465
XPM0_T	Transmit Pulse Mask0	$xx26_H$	467
XPM1_T	Transmit Pulse Mask1	$xx27_H$	468
XPM2_T	Transmit Pulse-Mask Register 2	$xx28_H$	469
SIC4_T	System Interface Control Register 4	$xx2A_H$	470
IDLE_T	Idle Channel Code Register	$xx2B_H$	471
XDL1_T	Transmit DL-Bit Register 1	$xx2C_H$	472
CCB1_T	Clear Channel Register 1	$xx2F_H$	473
ICB1_T	Idle Channel Register 1	$xx32_H$	474

Table 99 Registers Overview T1/J1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
LIM0_T	Line Interface Mode 0	$xx36_H$	475
LIM1_T	Line Interface Mode 1	$xx37_H$	477
PCD_T	Pulse Count Detection Register	$xx38_H$	479
PCR_T	Pulse Count Recovery	$xx39_H$	480
LIM2_T	Line Interface Mode 2	$xx3A_H$	481
LCR1_T	Loop Code Register 1	$xx3B_H$	483
LCR2_T	Loop Code Register 2	$xx3C_H$	485
LCR3_T	Loop Code Register 3	$xx3D_H$	486
SIC1_T	System Interface Control 1	$xx3E_H$	487
SIC2_T	System Interface Control 2	$xx3F_H$	489
SIC3_T	System Interface Control 3	$xx40_H$	491
CMR4_T	Clock Mode Register 4	$xx41_H$	493
CMR5_T	Clock Mode Register 5	$xx42_H$	494
CMR6_T	Clock Mode Register 6	$xx43_H$	495
CMR1_T	Clock Mode Register 1	$xx44_H$	497
CMR2_T	Clock Mode Register 2	$xx45_H$	499
ESM_T	Errored Second Mask	$xx47_H$	502
CMR3_T	Clock Mode Register 3	$xx48_H$	503
DEC_T	Disable Error Counter	$xx60_H$	504
XS1_T	Transmit Signaling Register 1	$xx70_H$	505
PC1_T	Port Configuration 1	$xx80_H$	507
PC5_T	Port Configuration 5	$xx84_H$	511
PC6_T	Port Configuration 6	$xx86_H$	513
CMDR2_T	Command Register 2	$xx87_H$	514
CMDR3_T	Command Register 3	$xx88_H$	515
CMDR4_T	Command Register 4	$xx89_H$	516
CCR3_T	Common Configuration Register 3	$xx8B_H$	518
CCR4_T	Common Configuration Register 4	$xx8C_H$	520
CCR5_T	Common Configuration Register 5	$xx8D_H$	522
MODE2_T	Mode Register 2	$xx8E_H$	524
MODE3_T	Mode Register 3	$xx8F_H$	525
XFIFO2L_T	Transmit FIFO 2 Lower Byte	$xx9C_H$	536
XFIFO2H_T	Transmit FIFO 2 Higher Byte	$xx9D_H$	537
XFIFO3L_T	Transmit FIFO 3 Lower Byte	$xx9E_H$	538
XFIFO3H_T	Transmit FIFO 3 Higher Byte	$xx9F_H$	539
TSEO_T	Time Slot Even/Odd Select	$xxA0_H$	540
TSBS1_T	Time Slot Bit Select 1	$xxA1_H$	541
TSBS2_T	Time Slot Bit Select 2	$xxA2_H$	542
TSBS3_T	Time Slot Bit Select 3	$xxA3_H$	543
TSS2_T	Time Slot Select 2	$xxA4_H$	544
TSS3_T	Time Slot Select 3	$xxA5_H$	545

Table 99 Registers Overview T1/J1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TPC0_T	Test Pattern Control Register 0	xxA8$_H$	547
TXP1_T	TX Pulse Template Register 1	xxC1$_H$	548
ALS_T	Automatic Loop Switching Register	xxD9$_H$	554
IMR7_T	Interrupt Mask Register 7	xxDF$_H$	561
RFIFO1L_T	Receive FIFO - HDLC Channel 1 - Lower Byte	xx00$_H$	562
RFIFO1H_T	Receive FIFO - HDLC Channel 1 - Higher Byte	xx01$_H$	563
RBD_T	Receive Buffer Delay	xx49$_H$	564
VSTR_T	Version Status Register	xx4A$_H$	565
RES_T	Receive Equalizer Status	xx4B$_H$	566
FRS0_T	Framer Receive Status Register 0	xx4C$_H$	567
FRS1_T	Framer Receive Status Register 1	xx4D$_H$	569
FRS2_T	Framer Receive Status Register 2	xx4E$_H$	571
FECL_T	Framing Error Counter Lower Byte	xx50$_H$	573
FECH_T	Framing Error Counter Higher Byte	xx51$_H$	574
CVCL_T	Code Violation Counter Lower Byte	xx52$_H$	575
CVCH_T	Code Violation Counter Higher Byte	xx53$_H$	576
CEC1L_T	CRC Error Counter 1 Lower Byte	xx54$_H$	577
CEC1H_T	CRC Error Counter 1 Higher Byte	xx55$_H$	578
EBCL_T	E-Bit Error Counter Lower Byte	xx56$_H$	579
EBCH_T	E-Bit Error Counter Higher Byte	xx57$_H$	580
BECL_T	Bit Error Counter Lower Bytes	xx58$_H$	581
BECH_T	Bit Error Counter Higher Bytes	xx59$_H$	582
COEC_T	COFA Event Counter	xx5A$_H$	583
RDL1_T	Receive DL-Bit Register 1	xx5C$_H$	584
RDL2_T	Receive DL-Bit Register 2	xx5D$_H$	585
RDL3_T	Receive DL-Bit Register 3	xx5E$_H$	586
RSP1_T	Receive Signaling Pointer 1	xx62$_H$	587
RSP2_T	Receive Signaling Pointer 2	xx63$_H$	588
SIS_T	Signaling Status Register	xx64$_H$	589
RSIS_T	Receive Signaling Status Register	xx65$_H$	591
RBCL_T	Receive Byte Count Low - HDLC Channel 1	xx66$_H$	593
RBCH_T	Received Byte Count High - HDLC Channel 1	xx67$_H$	594
ISR0_T	Interrupt Status Register 0	xx68$_H$	595
ISR1_T	Interrupt Status Register 1	xx69$_H$	597
ISR2_T	Interrupt Status Register 2	xx6A$_H$	599
ISR3_T	Interrupt Status Register 3	xx6B$_H$	600
ISR4_T	Interrupt Status Register 4	xx6C$_H$	602
ISR5_T	Interrupt Status Register 5	xx6D$_H$	604
GIS_T	Global Interrupt Status Register	xx6E$_H$	606
RS1_T	Receive Signaling Register 1	xx70$_H$	609
RBC2_T	Receive Byte Count Register 2	xx90$_H$	611

Table 99 Registers Overview T1/J1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
RBC3_T	Receive Byte Count Register 3	xx91$_H$	612
SIS3_T	Signaling Status Register 3	xx9A$_H$	613
RSIS3_T	Receive Signaling Status Register 3	xx9B$_H$	614
RFIFO2L_T	Receive FIFO 2 Lower Byte	xx9C$_H$	616
RFIFO2H_T	Receive FIFO 2 Higher Byte	xx9D$_H$	617
RFIFO3L_T	Receive FIFO 3 Lower Byte	xx9E$_H$	618
RFIFO3H_T	Receive FIFO 3 Higher Byte	xx9F$_H$	619
SIS2_T	Signaling Status Register 2	xxA9$_H$	620
RSIS2_T	Receive Signaling Status Register 2	xxAA$_H$	621
MFPI_T	Multi Function Port Input Register	xxAB$_H$	623
ISR6_T	Interrupt Status Register 6	xxAC$_H$	624
PPR0_T	PPR Data 0	xxD1$_H$	627
PPR1_T	PPR Data 1	xxD2$_H$	628
ISR7_T	Interrupt Status Register 7	xxD8$_H$	629
PRBSSTA_T	PRBS Status Register	xxDA$_H$	630
CLKSTAT_T	Clock Status Register	xxFE$_H$	632
IPC_T	Interrupt Port Configuration	0008$_H$	436
CCR1_T	Common Configuration Register 1	09$_H$	437
RTR2	Receive Time Slot Register 2	0D$_H$	441
RTR3	Receive Time Slot Register 3	0E$_H$	441
RTR4	Receive Time Slot Register 4	0F$_H$	441
TTR2	Transmit Time Slot Register 2	11$_H$	443
TTR3	Transmit Time Slot Register 3	12$_H$	443
TTR4	Transmit Time Slot Register 4	13$_H$	443
IMR0	Interrupt Mask Register 0	14$_H$	445
IMR1	Interrupt Mask Register 1	15$_H$	445
IMR2	Interrupt Mask Register 2	16$_H$	445
IMR3	Interrupt Mask Register 3	17$_H$	445
IMR4	Interrupt Mask Register 4	18$_H$	445
IMR5	Interrupt Mask Register 5	19$_H$	445
IMR6	Interrupt Mask Register 6	1A$_H$	445
XDL2	Transmit DL-Bit Register 2	2D$_H$	472
XDL3	Transmit DL-Bit Register 3	2E$_H$	472
CCB2	Clear Channel Register 2	30$_H$	473
CCB3	Clear Channel Register 3	31$_H$	473
ICB2	Idle Channel Register 2	33$_H$	474
ICB3	Idle Channel Register 3	34$_H$	474
GCR_T	Global Configuration Register	0046$_H$	501
CIS_T	Channel Interrupt Status Register	006F$_H$	607
XS2	Transmit Signaling Register 2	71$_H$	505
RS2	Receive Signaling Register 2	71$_H$	609

Table 99 Registers Overview T1/J1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
XS3	Transmit Signaling Register 3	72_H	505
RS3	Receive Signaling Register 3	72_H	609
XS4	Transmit Signaling Register 4	73_H	505
RS4	Receive Signaling Register 4	73_H	609
XS5	Transmit Signaling Register 5	74_H	505
RS5	Receive Signaling Register 5	74_H	609
XS6	Transmit Signaling Register 6	75_H	505
RS6	Receive Signaling Register 6	75_H	609
XS7	Transmit Signaling Register 7	76_H	505
RS7	Receive Signaling Register 7	76_H	609
XS8	Transmit Signaling Register 8	77_H	505
RS8	Receive Signaling Register 8	77_H	609
XS9	Transmit Signaling Register 9	78_H	505
RS9	Receive Signaling Register 9	78_H	610
XS10	Transmit Signaling Register 10	79_H	506
RS10	Receive Signaling Register 10	79_H	610
XS11	Transmit Signaling Register 11	$7A_H$	506
RS11	Receive Signaling Register 11	$7A_H$	610
XS12	Transmit Signaling Register 12	$7B_H$	506
RS12	Receive Signaling Register 12	$7B_H$	610
PC2	Port Configuration Register 2	81_H	509
PC3	Port Configuration Register 3	82_H	509
PC4	Port Configuration Register 4	83_H	509
GPC1_T	Global Port Configuration 1	0085_H	512
GPC2_T	Global Port Configuration Register 2	$008A_H$	517
GCM1_T	Global Clock Mode Register 1	0092_H	526
GCM2_T	Global Clock Mode Register 2	0093_H	527
GCM3_T	Global Clock Mode Register 3	0094_H	529
GCM4_T	Global Clock Mode Register 4	0095_H	530
GCM5_T	Global Clock Mode Register 5	0096_H	531
GCM6_T	Global Clock Mode Register 6	0097_H	532
GCM7_T	Global Clock Mode Register 7	0098_H	534
GCM8_T	Global Clock Mode Register 7	0099_H	535
GIMR_T	Global Interrupt Mask Register	$00A7_H$	546
GIS2_T	Global Interrupt Status 2	$00AD_H$	626
TXP1	TX Pulse Template Register 1	$C1_H$	548
TXP2	TX Pulse Template Register 2	$C2_H$	548
TXP3	TX Pulse Template Register 3	$C3_H$	548
TXP4	TX Pulse Template Register 4	$C4_H$	548
TXP5	TX Pulse Template Register 5	$C5_H$	548
TXP6	TX Pulse Template Register 6	$C6_H$	548

Table 99 Registers Overview T1/J1 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TXP7	TX Pulse Template Register 7	$C7_H$	548
TXP8	TX Pulse Template Register 8	$C8_H$	548
TXP9	TX Pulse Template Register 9	$C9_H$	548
TXP10	TX Pulse Template Register 10	CA_H	548
TXP11	TX Pulse Template Register 11	CB_H	548
TXP12	TX Pulse Template Register 12	CC_H	548
TXP13	TX Pulse Template Register 13	CD_H	548
TXP14	TX Pulse Template Register 14	CE_H	548
TXP15	TX Pulse Template Register 15	CF_H	548
TXP16	TX Pulse Template Register 16	$D0_H$	548
GPC3_T	Global Port Configuration Register 3	$00D3_H$	549
GPC4_T	Global Port Configuration Register 4	$00D4_H$	550
GPC5_T	Global Port Configuration Register 5	$00D5_H$	551
GPC6_T	Global Port Configuration Register 6	$00D6_H$	552
INBLDTR_T	In-Band Loop Detection Time Register	$00D7_H$	553
PRBSTS1_T	PRBS Time Slot Register 1	$00DB_H$	556
PRBSTS2_T	PRBS Time Slot Register 2	$00DC_H$	558
PRBSTS3_T	PRBS Time Slot Register 3	$00DD_H$	559
PRBSTS4_T	PRBS Time Slot Register 4	$00DE_H$	560
IMR7	Interrupt Mask Register 7	DF_H	445
DSTR_T	Device Status Register	$00E7_H$	631

The register is addressed wordwise.

See **Registers Access Types**

8.1 Detailed Description of T1/J1 Control Registers

Transmit FIFO - HDLC Channel 1 - Lower Byte

Writing data to XFIFO of HDLC channel 1 can be done in 8-bit (byte) or 16-bit (word) access, see **Chapter 3.4.3**. The LSB is transmitted first. Up to 64bytes/32 words of transmit data can be written to the XFIFO following a XPR interrupt.

XFIFO1L_T	Offset	Reset Value
Transmit FIFO - HDLC Channel 1 Lower Byte	**$xx00_H$**	**xx_H**

7	6	5	4	3	2	1	0
XF7	**XF6**	**XF5**	**XF4**	**XF3**	**XF2**	**XF1**	**XF0**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF7	7	w	**Transmit FIFO HDLC Channel 1, lower byte**
XF6	6	w	
XF5	5	w	
XF4	4	w	
XF3	3	w	
XF2	2	w	
XF1	1	w	
XF0	0	w	

Transmit FIFO - HDLC Channel 1 _ Higher Byte

Writing data to XFIFO of HDLC channel 1 can be done in 8-bit (byte) or 16-bit (word) access, see **Chapter 3.4.3**. The LSB is transmitted first. Up to 64bytes/32 words of transmit data can be written to the XFIFO following a XPR interrupt.

XFIFO1H_T	Offset	Reset Value
Transmit FIFO - HDLC Channel 1 - Higher Byte	**$xx01_H$**	**xx_H**

7	6	5	4	3	2	1	0
XF15	**XF14**	**XF13**	**XF12**	**XF11**	**XF10**	**XF9**	**XF8**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF15	7	w	**Transmit FIFO HDLC Channel 1, higher byte**
XF14	6	w	
XF13	5	w	
XF12	4	w	
XF11	3	w	
XF10	2	w	
XF9	1	w	
XF8	0	w	

Receive Address Byte High Register 1

See **Receive Address Byte High Register 1**

Command Register

CMDR_T	Offset	Reset Value
Command Register	$xx02_H$	00_H

7	6	5	4	3	2	1	0
RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RMC	7	w	**Receive Message Complete - HDLC Channel 1** Confirmation from external micro controller to OctalFALCTM that the current frame or data block has been fetched following a RPF or RME interrupt, thus the occupied space in the RFIFO can be released. If RMC is given while RFIFO is already cleared, the next incoming data block is cleared instantly, although interrupts are generated.
RRES	6	w	**Receiver Reset** The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one-second timer and the receive signaling controller are reset. However the contents of the control registers is not deleted. A receiver reset should be made after switching from power down to power up (GCR.PD ´1´ -> ´0´).
XREP	5	w	**Transmission Repeat - HDLC Channel 1** If XREP is set together with XTF (write ´24_H´ to CMDR), the OctalFALCTM repeatedly transmits the contents of the XFIFO (1 up to 64 bytes) without HDLC framing fully transparently, i.e. without flag, CRC. If XREP is set together with XME (write ´22_H´ to CMDR), the OctalFALCTM repeatedly transmits the contents of the XFIFO (1 up to 64 bytes) including HDLC framing and calculated CRC. The cyclic transmission is stopped with a SRES command or by resetting XREP. *Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.*
XRES	4	w	**Transmitter Reset** The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper are reset. However the contents of the control registers is not deleted.
XHF	3	w	**Transmit HDLC Frame - HDLC Channel 1** After having written up to 32 or 64 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.
XTF	2	w	**Transmit Transparent Frame - HDLC Channel 1** Initiates the transmission of a transparent frame without HDLC framing.

Field	Bits	Type	Description
XME	1	w	**Transmit Message End - HDLC Channel 1** Indicates that the data block written last to the transmit FIFO completes the current frame. The OctalFALC™ can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.
SRES	0	w	**Signaling Transmitter Reset - HDLC Channel 1** The transmitter of the signaling controller is reset. XFIFO is cleared of any data and an abort sequence (seven ´1's) followed by interframe time fill is transmitted. In response to SRES a XPR interrupt is generated. This command can be used by the external micro controller external micro controller to abort a frame currently in transmission. **Notes** *1. The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the external micro controller operates with a very high clock rate in comparison with the OctalFALC™´s clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.* *2. If SCLKX is used to clock the transmission path, commands to the HDLC transmitter should only be sent while this clock is available. If SCLKX is missing, the command register is blocked after an HDLC command is given.*

Mode Register

With this register the mode of the HDLC controller 1 is defined.

MODE_T	Offset	Reset Value
Mode Register	$xx03_H$	00_H

7	6	5	4	3	2	1	0
MDS			BRAC	HRAC	DIV	HDLCI	RFT2
rw			rw	rw	rw	rw	rw

Field	Bits	Type	Description
MDS	7:5	rw	**Mode Select - HDLC Channel 1** The operating mode of the HDLC controller is selected. See **Chapter 5.3.2** 000_B , Reserved 001_B , Signaling System 7 (SS7) support[1)] 010_B , One-byte address comparison mode (RAL1,2) 011_B , Two-byte address comparison mode (RAH1,2 and RAL1,2) 100_B , No address comparison 101_B , One-byte address comparison mode (RAH1,2) 110_B , Reserved 111_B , No HDLC framing mode
BRAC	4	rw	**BOM Receiver Active - HDLC Channel 1** Switches the BOM receiver to operational or inoperational state. See **Chapter 5.3.1** and **Chapter 5.3.4**. 0_B , BOM Receiver inactive 1_B , BOM Receiver active
HRAC	3	rw	**Receiver Active - HDLC Channel 1** Switches the HDLC receiver to operational or inoperational state. See **Chapter 5.3.1** and **Chapter 5.3.4**. 0_B , HDLC Receiver inactive 1_B , HDLC Receiver active
DIV	2	rw	**Data Inversion - HDLC Channel 1** Setting this bit inverts the internal generated HDLC channel 1 data stream. 0_B , Normal operation, HDLC data stream not inverted 1_B , HDLC data stream inverted
HDLCI	1	rw	**Inverse HDLC Operation Selection** Setting this bit switches the HDLC channel to the system side (”inverse” HDLC configuration), see **Figure 39**. 0_B , HDLC protocol is sent and received on line side. 1_B , HDLC protocol is sent and received on system side.

Field	Bits	Type	Description
RFT2	0	rw	**HDLC Receive FIFO Size Selection - HDLC channel 1** This bit selects the receive FIFO size of HDLC channel 1, see **Table 10**. 0_B , HDLC receive FIFO is 32, 16, 4 or 2 byte deep, dependent on CCR1.RFT(1:0). *Note: Use this mode for software compatibility with QuadFALC®.* 1_B , HDLC receive FIFO is 64 byte deep to improve the HDLC performance) *Note: Use this mode to improve the HDLC performance. No dependency from CCR1.RFT(1:0).*

1) CCR2.RADD must be set, if SS7 mode is selected

Receive Address Byte High Register 1

In operating modes that provide high byte address recognition, the high byte of the received address is compared to the individually programmable values in RAH1 and RAH2. The address registers are used by all HDLC channels in common.

RAH1_T	Offset	Reset Value
Receive Address Byte High Register 1	$xx04_H$	FD_H

7	6	5	4	3	2	1	0
RAH17	**RAH16**	**RAH15**	**RAH14**	**RAH13**	**RAH12**	**0**	**RAH10**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RAH17	7	rw	**Value of First Individual High Address Bit** RAH17.
RAH16	6	rw	**Value of First Individual High Address Bit** RAH16.
RAH15	5	rw	**Value of First Individual High Address Bit** RAH15.
RAH14	4	rw	**Value of First Individual High Address Bit** RAH14.
RAH13	3	rw	**Value of First Individual High Address Bit** RAH13.
RAH12	2	rw	**Value of First Individual High Address Bit** RAH12.
0	1	rw	**Fixed ´0´** This bit (C/R bit) is excluded from the address comparison.
RAH10	0	rw	**Value of First Individual High Address Bit** RAH10.

Receive Address Byte High Register 2

RAH2_T	Offset	Reset Value
Receive Address Byte High Register 2	$xx05_H$	FF_H

7	6	5	4	3	2	1	0
RAH25	**RAH24**	**RAH23**	**RAH22**	**RAH21**	**RAH20**	**RAH19**	**RAH18**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RAH25	7	rw	**Value of Second Individual High Address Bit** RAH25.
RAH24	6	rw	**Value of Second Individual High Address Bit** RAH24.
RAH23	5	rw	**Value of Second Individual High Address Bit** RAH23.
RAH22	4	rw	**Value of Second Individual High Address Bit** RAH22.
RAH21	3	rw	**Value of Second Individual High Address Bit** RAH21.
RAH20	2	rw	**Value of Second Individual High Address Bit** RAH20.
RAH19	1	rw	**Value of Second Individual High Address Bit** RAH19.
RAH18	0	rw	**Value of Second Individual High Address Bit** RAH18.

Receive Address Byte Low Register 1

RAL1_T	Offset	Reset Value
Receive Address Byte Low Register 1	$xx06_H$	FF_H

7	6	5	4	3	2	1	0
RAL17	**RAL16**	**RAL15**	**RAL14**	**RAL13**	**RAL12**	**RAL11**	**RAL10**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RAL17	7	rw	**Value of First Individual Low Address Byte** RAL17
RAL16	6	rw	**Value of First Individual Low Address Bit** RAL16.
RAL15	5	rw	**Value of First Individual Low Address Bit** RAH15.
RAL14	4	rw	**Value of First Individual Low Address Bit** RAL14.
RAL13	3	rw	**Value of First Individual Low Address Bit** RAL13.
RAL12	2	rw	**Value of First Individual Low Address Bit** RAL12.
RAL11	1	rw	**Value of First Individual Low Address Bit** RAL11.
RAL10	0	rw	**Value of First Individual Low Address Bit** RAL10.

Receive Address Byte Low Register 2

RAL2_T	Offset	Reset Value
Receive Address Byte Low Register 2	$xx07_H$	FF_H

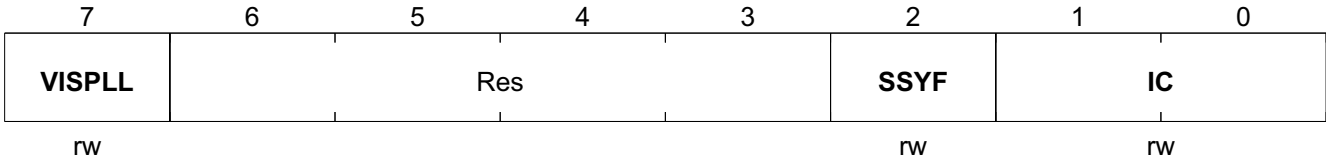
7	6	5	4	3	2	1	0
RAL25	**RAL24**	**RAL23**	**RAL22**	**RAL21**	**RAL20**	**RAL19**	**RAL18**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RAL25	7	rw	**Value of Second Individual Low Address Bit** RAL25.
RAL24	6	rw	**Value of Second Individual Low Address Bit** RAL24.
RAL23	5	rw	**Value of Second Individual Low Address Bit** RAL23.
RAL22	4	rw	**Value of Second Individual Low Address Bit** RAL22.
RAL21	3	rw	**Value of Second Individual Low Address Bit** RAL21.
RAL20	2	rw	**Value of Second Individual Low Address Bit** RAL20.
RAL19	1	rw	**Value of Second Individual Low Address Bit** RAL19.
RAL18	0	rw	**Value of Second Individual Low Address Bit** RAL18.

Interrupt Port Configuration

Unused bits have to be cleared.

IPC_T	Offset	Reset Value
Interrupt Port Configuration	0008_H	00_H



Field	Bits	Type	Description
VISPLL	7	rw	**Masked PLL Interrupts Visible** See **Chapter 3.4.4**. 0_B , Masked interrupt status bit PLLLC is not visible in register GIS2. 1_B , Masked interrupt status bit PLLLC is visible in GIS2.
SSYF	2	rw	**Select SYNC Frequency** Only applicable in master mode (LIM0.MAS = ´1´) and bit CMR2.DCF is cleared.See also **Chapter 3.6.5**. *Note: If COMP = ´1´ the bits SSYF of both pseudo QuadFALCs are logically ored.* 0_B , Reference clock on port SYNC is 1.544/2.048 MHz (see LIM1.DCOC) 1_B , Reference clock on port SYNC is 8 kHz
IC	1:0	rw	**Interrupt Port Configuration** These bits define the function of the interrupt output pins: If COMP = ´1´, pins INT1 and INT2 of the pseudo QuadFALC1 and pseudo QuadFALC2 respectively; if COMP = ´0´, pin INT, see **Chapter 3.4.4**: $X0_B$, Open drain output 01_B , Push/pull output, active low 11_B , Push/pull output, active high

Common Configuration Register 1

CCR1_T	Offset	Reset Value
Common Configuration Register 1	09_H	00_H

7	6	5	4	3	2	1	0
RSCC	BRM	EDLX	EITS	ITF	XMFA	RFT	
rw	rw	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
RSCC	7	rw	**Serial CAS Format Selection** Selects if RSC interrupt is generated or suppressed. 0_B , RSC interrupt is generated for all channels. 1_B , RSC interrupt is suppressed for cleared channels.
BRM	6	rw	**BOM Receive Mode - HDLC Channel 1** (significant in BOM mode only). See **Chapter 5.3.4**. 0_B , 10-byte packets 1_B , Continuous reception
EDLX	5	rw	**Enable DL-Bit Access through the Transmit FIFO - HDLC Channel 1** A one in this bit position enables the internal DL-bit access through the receive/transmit FIFO of the signaling controller. FMR1.EDL has to be cleared. See also **Chapter 5.3.4**.
EITS	4	rw	**Enable Internal Time Slot 0 to 31 Signaling - HDLC Channel 1** 0_B , Internal signaling in time slots 0 to 31 defined by registers RTR(4:1) or TTR(4:1) is disabled. 1_B , Internal signaling in time slots 0 to 31 defined by registers RTR(4:1) or TTR(4:1) is enabled.
ITF	3	rw	**Interframe Time Fill - HDLC Channel 1** Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller. 0_B , Continuous logical 1 is output 1_B , Continuous flag sequences are output (01111110 bit patterns)

Field	Bits	Type	Description
XMFA	2	rw	**Transmit Multiframe Aligned - HDLC Channel 1** Determines the synchronization between the framer and the corresponding signaling controller. *Note: During the transmission of the XFIFO content, the $\overline{SYPX}$ or XMFS interval time should not be changed, otherwise the XFIFO data has to be retransmitted.* 0_B , The contents of the XFIFO is transmitted without multiframe alignment. 1_B , The contents of the XFIFO is transmitted multiframe aligned. If CCR1.EDLXis set, transmission of DL-bits is started in F72 format with frame 26. The first byte in XFIFO is transmitted in the first time slot selected by TTR(4:1) and so on. After receiving a complete multiframe in the time slot mode (RTR(4:1)) an ISR0.RME interrupt is generated, if no HDLC or BOM mode is enabled. In DL-bit access (CCR1.EDLX/EITS = ´10b´) XMFA is not valid.
RFT	1:0	rw	**RFIFO Threshold Level - HDLC Channel 1** The size of the accessible part of RFIFO can be determined by programming these bits and the bit MODE.RFT2, see **Chapter 3.4.3**. If MODE.RFT2 = ´1´ these bits are not valid and the accessible receive FIFO size is 64 byte. The value of RFT(2:0) can be changed dynamically • If reception is not running or • After the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer). *Note: Changing of the the value of RFT(2:0) is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after an RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by an RMC command (see table **RFT Constant Values (Case 2)**):* 000_B , 32 bytes (default value) 001_B , 16 bytes 010_B , 4 bytes 011_B , 2 bytes $1xx_B$, 64 bytes

Table 100 RFT Constant Values (Case 2)

Name and Description	Value
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(5:0)	$1xx_B$
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(4:0)	000_B
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(3:0)	001_B

Table 100 RFT Constant Values (Case 2) (cont'd)

Name and Description	Value
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC(1:0)	010_B
Bit Positions in RBCL Reset by a CMDR.RMC Command RBC0	011_B

Common Configuration Register 2

Unused bits have to be cleared.

CCR2_T	Offset	Reset Value
Common Configuration Register 2	$xx0A_H$	00_H

7	6	5	4	3	2	1	0
Res		TSFL	RADD	RBFE	RCRC	XCRC	Res
		rw	rw	rw	rw	rw	

Field	Bits	Type	Description
TSFL	5	rw	**Enable Shared Flags in Transmit Direction** In receive direction shared flag is detected automatically 0_B , Both, an opening and a closing flag (´7EH´) are transmitted for each HDLC frame (normal operation). 1_B , The closing flag (´7E´) of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one to be transmitted.
RADD	4	rw	**Receive Address Pushed to RFIFO - HDLC Channel 1** If this bit is set, the received HDLC address information (1 or 2 bytes, depending on the address mode selected by MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode and transparent mode 1. RADD must be set, if SS7 mode is selected. See also Chapter 5.3.2.
RBFE	3	rw	**Receive BOM Filter Enable - HDLC Channel 1** Setting this bit the bit oriented message (BOM) receiver only accepts BOM frames after detecting 7 out of 10 equal BOM pattern. The BOM pattern is stored in the RFIFO adding a receive status byte marking a BOM frame (RSIS.HFR) and an interrupt ISR0.RME is generated. The current state of the BOM receiver is indicated in register SIS.IVB. When the valid BOM pattern disappears an interrupt ISR0.BIV is generated. See Chapter 5.3.4.
RCRC	2	rw	**Receive CRC on/off - HDLC Channel 1** Only applicable in non-auto mode. If this bit is set, the received CRC checksum is written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If non-auto mode is selected, the limits for “valid frame” check are modified (refer to RSIS.VFR).
XCRC	1	rw	**Transmit CRC on/off - HDLC Channel 1** If this bit is set, the CRC checksum is not generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame is closed automatically with a closing flag. *Note: The OctalFALCTM does not check whether the length of the frame, i.e., the number of bytes to be transmitted, makes sense or not.*

Receive Time Slot Register 1

See **Chapter 5.6.3** and **Chapter 5.6.4**.

RTR1_T	Offset	Reset Value
Receive Time Slot Register 1	**$xx0C_H$**	**00_H**

7	6	5	4	3	2	1	0
TS0	**TS1**	**TS2**	**TS3**	**TS4**	**TS5**	**TS6**	**TS7**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS0	7	rw	**Time Slot Register** These bits define the received time slots on the system highway port RDO to be extracted. Additionally these registers control the RSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.A one in the RTR(4:1) bits samples the corresponding time slot in the RFIFO of the signaling controller, if bit CCR1.EITS is set. Assignments: • SIC2.SSC2 = ´0´: (32 time slots/frame): TS0 → time slot 0,TS31 → time slot 31 • SIC2.SSC2 = ´1´: (24 time slots/frame): TS0 → time slot 0,TS23 → time slot 23 0_B , The corresponding time slot is not extracted and stored in the RFIFO. 1_B , The contents of the selected time slot is stored in the RFIFO. Although the idle time slots can be selected. This function is only active, if bits CCR1.EITS is set. The corresponding time slot is forced high on pin RSIGM.
TS1	6		
TS2	5		
TS3	4		
TS4	3		
TS5	2		
TS6	1		
TS7	0		

Similar Registers

Registers RTR2 to RTR4 have the same layout and description. Their reset values are ´00_H´.

The Offset Addresses are listed in **RTRn Overview**, for bit names refer to **Receive Time Slot Registers**

Table 101 RTRn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
RTR2	Receive Time Slot Register 2	$0D_H$	
RTR3	Receive Time Slot Register 3	$0E_H$	
RTR4	Receive Time Slot Register 4	$0F_H$	

Table 102 Receive Time Slot Registers

	7	6	5	4	3	2	1	0
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS7	TS7
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15

Table 102 Receive Time Slot Registers (cont'd)

RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

Transmit Time Slot Register 1

See **Chapter 5.6.3** and **Chapter 5.6.4**.

TTR1_T	Offset	Reset Value
Transmit Time Slot Register 1	$xx10_H$	00_H

7	6	5	4	3	2	1	0
TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS0	7	rw	**Transmit Time Slot Register** These bits define the transmit time slots on the system highway to be inserted. Additionally these registers control the XSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.A one in the TTR(4:1) bits inserts the corresponding time slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EDLX/EITS = 00, insertion of data received on port XSIG is controlled by this registers.Assignments: • SIC2.SSC2 = ´0´: (32 time slots/frame): TS0 → time slot 0, TS31 → time slot 31 • SIC2.SSC2 = ´1´: (24 time slots/frame): TS0 → time slot 0, TS23 → time slot 23 0_B , The selected time slot is not inserted into the outgoing data stream. 1_B , The contents of the selected time slot is inserted into the outgoing data stream from XFIFO. This function is only active, if bits CCR1.EITS is set. The corresponding time slot are forced high on marker pin XSIGM.
TS1	6		
TS2	5		
TS3	4		
TS4	3		
TS5	2		
TS6	1		
TS7	0		

Similar Registers

Registers TTR2 to TTR4 have the same layout and description.

The Offset Addresses are listed in **TTRn Overview**, for bit names refer to **Transmit Time Slot Registers**

Table 103 TTRn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
TTR2	Transmit Time Slot Register 2	11_H	
TTR3	Transmit Time Slot Register 3	12_H	
TTR4	Transmit Time Slot Register 4	13_H	

Table 104 Transmit Time Slot Registers

	7	6	5	4	3	2	1	0
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS7	TS7

Table 104 Transmit Time Slot Registers (cont'd)

TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

Interrupt Mask Register 0

Each interrupt source can generate an interrupt signal on port INT (characteristics of the output stage are defined by register IPC). A “1” in a bit position of IMR(7:0) sets the mask active for the interrupt status in ISR(7:0). Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are not displayed in the Interrupt Status Register if bit GCR.VIS is cleared or displayed in the Interrupt Status Register if bit GCR.VIS is set, see **Chapter 3.4.4**. After reset, all interrupts are disabled masked.

IMR0_T	Offset	Reset Value
Interrupt Mask Register 0	$xx14_H$	FF_H

7	6	5	4	3	2	1	0
RME	BIF/RFS	ISF	RMB	RSC	CRC6	PDEN	RPF
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RME	7	rw	**Interrupt Mask Bits** Each interrupt source can generate an interrupt signal on port INT (or INT1 and INT2 respectively). Characteristics of the output stage are defined by register IPC. A ´1´ in a bit position of IMR(7:0) sets the mask active for the interrupt status in ISR(7:0). Mask interrupt statuses neither generate a signal on INT (INT1, INT2), not are thy visible in register GIS. Moreover they are not displayed in the interrupt status register if bit GCR.VIS is cleared; they are displayed in the interrupt status register if bit GCR.VIS is set.
BIF/RFS	6		
ISF	5		
RMB	4		
RSC	3		
CRC6	2		
PDEN	1		
RPF	0		

Similar Registers

Registers IMR1 to IMR7 have the same description.

The Offset Addresses are listed in **IMRn Overview**, for bit names and layout refer to **Interrupt Mask Registers**

Table 105 IMRn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
IMR0	Interrupt Mask Register 0	14_H	
IMR1	Interrupt Mask Register 1	15_H	
IMR2	Interrupt Mask Register 2	16_H	
IMR3	Interrupt Mask Register 3	17_H	
IMR4	Interrupt Mask Register 4	18_H	
IMR5	Interrupt Mask Register 5	19_H	
IMR6	Interrupt Mask Register 6	$1A_H$	
IMR7	Interrupt Mask Register 7	DF_H	

Table 106 Interrupt Mask Registers

	7	6	5	4	3	2	1	0
IMR0	RME	RFS	ISF	RMB	RSC	CRC6	PDEN	RPF

Table 106 Interrupt Mask Registers (cont'd)

IMR1	CASE	RDO	ALLS	XDU	XMB	SUEX	XLSC	XPR
IMR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA
IMR3	ES	SEC			LLBSC	LTC	RSN	RSP
IMR4	XSP	XSN	RME2	RFS2	RDO2	ALLS2	XDU2	RPF2
IMR5	XPR2	XPR3	RME3	RFS3	RDO3	ALLS3	XDU3	RPF3
IMR6	SOLSU	SOLSD	LOLSU	LOLSD	SILSU	SILSD	LILSU	LILSD
IMR7				XCLKSS1	XCLKSS0			SEFEI

IMR3.LTC masks the status bit ISR3.LTC.

Single Bit Defect Insertion Register

After setting the corresponding bit, the selected defect is inserted into the transmit data stream at the next possible position. After defect insertion is completed, the bit is reset automatically.

IERR_T	Offset	Reset Value
Single Bit Defect Insertion Register	**xx1B$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res		**IFASE**	**IMFE**	**ICRCE**	**ICASE**	**IPE**	**IBV**
		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IFASE	5	rw	**Insert single FAS defect**
IMFE	4	rw	**Insert single multiframe defect**
ICRCE	3	rw	**Insert single CRC defect**
ICASE	2	rw	**Insert single CAS defect**
IPE	1	rw	**Insert single PRBS defect**
IBV	0	rw	**Insert bipolar violation** *Note: Except for CRC defects, CRC checksum calculation is done after defect insertion.*

Framer Mode Register 0

FMR0_T	Offset	Reset Value
Framer Mode Register 0	$xx1C_H$	00_H

7	6	5	4	3	2	1	0
XC		RC		FRS	SRAF	EXLS	SIM
rw		rw		rw	rw	rw	rw

Field	Bits	Type	Description
XC	7:6	rw	**Transmit Code** Serial line code for the transmitter, independent of the receiver. After changing XC(1:0), a transmitter software reset is required (CMDR.XRES = ´1´). 00_B , NRZ (optical interface) 01_B , CMI (1T2B+B8ZS), (optical interface) 10_B , AMI coding with Zero Code Suppression (ZCS, B7-stuffing). Disabling of the ZCS is done by activating the clear channel mode by register CCB(3:1). (ternary or digital interface) 11_B , B8ZS Code (ternary or digital dual-rail interface).
RC	5:4	rw	**Receive Code** Serial code receiver is independent to the transmitter. After changing RC(1:0), a receiver software reset is required (CMDR.RRES = ´1´). 00_B , NRZ (optical interface) 01_B , CMI (1T2B+B8ZS), (optical interface) 10_B , AMI coding with Zero Code Suppression (ZCS, B7-stuffing), (ternary or digital dual-rail interface) 11_B , B8ZS Code (ternary or digital dual-rail interface)
FRS	3	rw	**Force Resynchronization** A transition from low to high forces the frame aligner to execute a resynchronization of the pulse frame. In the asynchronous state, a new frame position is assumed at the next candidate if there is one. Otherwise, a new frame search with the meaning of a general reset is started. In the synchronous state this bit has the same meaning as bit FMR0.EXLS except if FMR2.MCSP = 1.
SRAF	2	rw	**Select Remote (Yellow) Alarm Format for F12 and ESF Format** 0_B , F12: bit2 = ´0´ in every channel. ESF: pattern “1111 1111 0000 0000” in data link channel. 1_B , F12: FS-bit of frame 12. ESF: bit2 = ´0´ in every channel

Field	Bits	Type	Description
EXLS	1	rw	**External Loss Of Frame** With a low to high transition a new frame search is started. This has the meaning of a general reset of the internal frame alignment unit. Synchronous state is reached only if there is one definite framing candidate. In the case of multiple candidates, the setting of the bit FMR0.FRS forces the receiver to lock onto the next available framing position.
SIM	0	rw	**Alarm Simulation** Setting/resetting this bit initiates internal error simulation of: AIS (blue alarm), loss-of-signal (red alarm), loss of frame alignment, remote (yellow) alarm, slip, framing errors, CRC errors, code violations. The error counters FEC, CVC, CEC, EBC are incremented.The selection of simulated alarms is done by the error simulation counter: FRS2.ESC(2:0) which is incremented with each setting of bit FMR0.SIM. For complete checking of the alarm indications eight simulation steps are necessary (FRS2.ESC(2:0) = ´0´ after a complete simulation). SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

Framer Mode Register 1

FMR1_T	Offset	Reset Value
Framer Mode Register 1	$xx1D_H$	00_H

7	6	5	4	3	2	1	0
CTM	Res	**EDL**	**PMOD**	**CRC**	**ECM**	**SSD0**	**XAIS**
rw		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CTM	7	rw	**Channel Translation Mode** The different channel translation modes are described in Table 43. 0_B , Channel translation mode 0 1_B , Channel translation mode 1
EDL	5	rw	**Enable DL-Bit Access through Register XDL(3:1)** Only applicable in F4, F24 or F72 frame format. 0_B , Normal operation. The DL-bits are taken from system highway or if enabled by CCR1.EDLX from the XFIFO of the signaling controller. 1_B , DL-bit register access. The DL-bit information are taken from the registers XDL(3:1) and overwrite the DL-bits received on the system highway (pin XDI) or from the internal XFIFO of the signaling controller. However, transmission of the contents of registers XDL(3:1) is disabled if transparent mode is enabled (FMR4.TM).
PMOD	4	rw	**PCM Mode** For E1 application this bit must be set low. Switching from E1 to T1 or vice versa the device needs up to 20 µs to settle up to the internal clocking. 0_B , PCM 30 or E1 mode. 1_B , PCM 24 or T1/J1 mode (see RC0.SJR for T1/J1 selection).
CRC	3	rw	**Enable CRC6** This bit is only significant when using the ESF format. 0_B , CRC6 check/generation disabled. For transmit direction, all CRC bit positions are set. 1_B , CRC6 check/generation enabled.

Field	Bits	Type	Description
ECM	2	rw	**Error Counter Mode** The function of the error counters (FEC,CEC,CVC,EBC) is determined by this bit. 0_B , Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8-bit access the low byte of the error counter should always be read before the high byte. The error counters are reset with the rising edge of the corresponding bits in the DEC register. 1_B , Every second the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided (do not access an error counter within 1 µs after the one-second interrupt occurs).
SSD0	1	rw	**Select System Date Rate 0** SIC1.SSD1, FMR1.SSD0 and SIC2.SSC2 define the data rate on the system highway. Programming SSD1/SSD0 and corresponding data rate is shown below. SIC2.SSC2 = 0: see table **SSD0 Constant Values (Case 1)** *Note: SIC2.SSC2 = 1: see table **SSD0 Constant Values (Case 2)***
XAIS	0	rw	**Transmit AIS Towards Remote End** Sends AIS (blue alarm) on ports XL1, XL2 towards the remote end. If Local Loop Mode is enabled the transmitted data is looped back to the system internal highway without any changes.

Table 107 SSD0 Constant Values (Case 1)

Name and Description	Value
System Data Rate 0 2.048 Mbit/s	00_B
System Data Rate 0 4.096 Mbit/s	01_B
System Data Rate 0 8.192 Mbit/s	10_B
System Data Rate 0 16.384 Mbit/s	11_B

Table 108 SSD0 Constant Values (Case 2)

Name and Description	Value
System Data Rate 0 1.544 Mbit/s	00_B
System Data Rate 0 3.088 Mbit/s	01_B

Table 108 SSD0 Constant Values (Case 2) (cont'd)

Name and Description	Value
System Data Rate 0 6.176 Mbit/s	10_B
System Data Rate 0 12.352 Mbit/s	11_B

Framer Mode Register 2

FMR2_T	Offset	Reset Value
Framer Mode Register 2	$xx1E_H$	00_H

7	6	5	4	3	2	1	0
AFRS	**MCSP**	**SSP**	**DAIS**	**SAIS**	**PLB**	**AXRA**	**EXZE**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AFRS	7	rw	**Automatic Force Resynchronization** For automatic handling (searching and resynchronization) of multiple candidates F12/F72 0_B , no automatic handling will be done. 1_B , automatic handling will be done.
MCSP	6	rw	**Multiple Candidates Synchronization Procedure** Together with bit FMR2.SSP the synchronization mode of the receive framer is defined, see **Chapter 5.4.6.1**.
SSP	5	rw	**Select Synchronization/Resynchronization Procedure** Together with bit FMR2.MCSP the synchronization mode of the receive framer is defined, see **Chapter 5.4.6.1**: • For constants in F12/F72 format see table **MCSP/SSP Constant Values (Case 1)** • For constant in F24 format see table **MCSP/SSP Constant Values (Case 2)**
DAIS	4	rw	**Disable AIS to System Interface** See also **Chapter 5.5.9**. 0_B , AIS is automatically inserted into the data stream to RDO if OctalFALCTM channel is in asynchronous state. 1_B , Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.
SAIS	3	rw	**Send AIS Towards System Interface** Sends AIS (blue alarm) on output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

Field	Bits	Type	Description
PLB	2	rw	**Payload Loop-Back** See **Chapter 5.7.3**. *Note: PLB is logically ored with the loop switching performed by automatic loop switching by BOM messages.* 0_B , Normal operation. Payload loop is disabled. 1_B , The payload loop-back loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, $\overline{\text{SYPX}}$ and XMFS is ignored. With FMR4.TM = ´1´ all 193-bits per frame are looped back. If FMR4.TM = ´0´ the DL- or FS- or CRC-bits are generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. During payload loop is active the receive time slot offset (registers RC(1:0)) should not be changed. It is recommended to write the actual value of XC1 into this register once again, because a write access to register XC1 sets the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation (the write operation forces a slip).
AXRA	1	rw	**Automatic Transmit Remote Alarm** 0_B , Normal operation 1_B , The remote alarm (yellow alarm) bit is set automatically in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is reset.
EXZE	0	rw	**Excessive Zeros Detection Enable** Selects error detection mode in the bipolar receive bit stream. 0_B , Only bipolar violations are detected. 1_B , Bipolar violations and zero strings of 8 or more contiguous zeros in B8ZS code or more than 15 contiguous zeros in AMI code are detected additionally and counted in the code violation counter CVC.

Table 109 MCSP/SSP Constant Values (Case 1)

Name and Description	Value
Synchronization/Resynchronization Procedure (F12/F72) Specified number of errors in both FT framing and FS framing lead to loss of sync (FRS0.LFA is set). In the case of FS-bit framing errors, bit FRS0.LMFA is set additionally. A complete new synchronization procedure is initiated to regain pulseframe alignment and then multiframe alignment.	00_B

Table 109 MCSP/SSP Constant Values (Case 1) (cont'd)

Name and Description	Value
Synchronization/Resynchronization Procedure (F12/F72) Specified number of errors in FT framing has the same effect as above. Specified number of errors in FS framing only initiates a new search for multiframe alignment without influencing pulseframe synchronous state (FRS0.LMFA is set).	01_B
Synchronization/Resynchronization Procedure (F12) (not in F72 format) A one enables a synchronization mode which is able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS leads to synchronization on the next candidate available. However, only the previously assumed candidate is discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer locks on the right pattern (no extensive CRC errors). Therefore bit FMR1.CRC must be set.	10_B

Table 110 MCSP/SSP Constant Values (Case 2)

Name and Description	Value
Synchronization/Resynchronization Procedure (F24) normal operation: synchronization is achieved only on verification the framing pattern.	00_B
Synchronization/Resynchronization Procedure (F24) Synchronous state is reached when three consecutive multiframe pattern are correctly found independent of the occurrence of CRC6 errors.	01_B
Synchronization/Resynchronization Procedure (F24) A one enables a synchronization mode which is able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS leads to synchronization on the next candidate available. However, only the previously assumed candidate is discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer locks on the right pattern (no extensive CRC errors). Therefore bit FMR1.CRC must be set.	10_B
Synchronization/Resynchronization Procedure (F24) Synchronization is achieved on verification the framing pattern and the CRC6 bits. Synchronous state is reached when framing pattern and CRC6 checksum are correctly found. For correct operation the CRC check must be enabled by setting bit FMR1.CRC.	11_B

LOOP

LOOP_T **Offset** **Reset Value**
LOOP **xx1F$_H$** **00$_H$**

7	6	5	4	3	2	1	0
Res	**RTM**	**ECLB**	**CLA**				
	rw	rw	rw				

Field	Bits	Type	Description
RTM	6	rw	**Receive Transparent Mode** Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of resynchronization of the receiver. This function can be used together with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.This bit should be enabled in case of unframed data reception mode. See also **Chapter 5.5.9**.
ECLB	5	rw	**Enable Channel Loop-Back** 0_B , Disables the channel loop-back. 1_B , Enables the channel loop-back selected by this register. *Note: CAS-BR must be switched off (FMR5.EIBR = ´0´) while channel loop back is enabled.*
CLA	4:0	rw	**Channel Address For Loop-Back** CLA values 1 to 24 selects the channel. During loop-back, the contents of the associated outgoing channel on ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed in register IDLE.

Framer Mode Register 4

FMR4_T	Offset	Reset Value
Framer Mode Register 4	$xx20_H$	00_H

7	6	5	4	3	2	1	0
AIS3	TM	XRA	SSC		AUTO	FM	
rw	rw	rw	rw		rw	rw	

Field	Bits	Type	Description
AIS3	7	rw	**Select AIS Condition** 0_B , AIS (blue alarm) is indicated (FRS0.AIS) when two or less zeros in the received bit stream are detected in a time interval of 12 frames (F4, F12, F72) or 24 frames (ESF). 1_B , AIS (blue alarm) detection is only enabled when OctalFALCTM is in asynchronous state. The alarm is indicated (FRS0.AIS) when three or less zeros within a time interval of 12 frames (F4, F12, F72), or five or less zeros within a time interval of 24 frames (ESF) are detected in the received bit stream.
TM	6	rw	**Transparent Mode** Setting this bit enables the transparent mode: In transmit direction bit 8 of every FS/DL time slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. Internal framing generation, insertion of CRC and DL data is disabled.
XRA	5	rw	**Transmit Remote Alarm (Yellow Alarm)** If high, remote alarm is sent on the PCM route. Clearing the bit removes the remote alarm pattern. Remote alarm indication depends on the multiframe structure as follows: • F4: Bit2 = ´0´ in every speech channel • F12: If FMR0.SRAF = ´0´: bit2 = ´0´ in every speech channel; If FMR0.SRAF = ´1´: FS-bit of frame 12 is forced to “1” • ESF: If FMR0.SRAF = ´0´: pattern “ ´1111111100000000 11111111000$_b$´ in data link channel; if FMR0.SRAF = ´1´: bit2 = ´0´ in every speech channelF72: Bit2 = ´0´ in every speech channel

Field	Bits	Type	Description
SSC	4:3	rw	**Select Sync Conditions** Loss of Frame Alignment (FRS0.LFA or opt. FRS0.LMFA) is declared if the following constants are incorrect. It depends on the selected multiframe format and optionally on bit FMR2.SSP which framing bits are observed, see **Chapter 5.4.2**: • FT-bits → FRS0.LFA • F12, F72:SSP = ´0´: FT-bits → FRS0.LFA and FS-bits → FRS0.LFA and FRS0.LMFA • F12, F72:SSP = ´1´: FT → FRS0.LFA and FS → FRS0.LMFA • ESF: ESF framing bits → FRS0.LFA 00_B , 2 out of 4 framing bits 01_B , 2 out of 5 framing bits 10_B , 2 out of 6 framing bits in F4/12/72 format 10_B , 2 out of 6 framing bits per multiframe period in ESF format 11_B , 4 consecutive multiframe pattern in ESF format
AUTO	2	rw	**Enable Auto Resynchronization** See **Chapter 5.4.2**. 0_B , The receiver does not re synchronize automatically. Starting a new synchronization procedure is possible by the bits FMR0.EXLS or FMR0.FRS. 1_B , Auto-resynchronization is enabled.
FM	1:0	rw	**Select Frame Mode** See **Chapter 5.4.1**, see also **Table 49**. 00_B , 12-frame multiframe format (F12, D3/4) 01_B , 4-frame multiframe format (F4) 10_B , 24-frame multiframe format (ESF) 11_B , 72-frame multiframe format (F72, remote switch mode)

Framer Mode Register 5

FMR5_T	Offset	Reset Value
Framer Mode Register 5	$xx21_H$	00_H

7	6	5	4	3	2	1	0
DLM	**EIBR**	**XLD**	**XLU**	Res	**XTM**	**SSC2**	Res
rw	rw	rw	rw		rw	rw	

Field	Bits	Type	Description
DLM	7	rw	**DL Bit Access Mode** See **Chapter 5.3.6.1**. 0_B , DL bit access as for QuadFALC®. 1_B , improved DL bit access.
EIBR	6	rw	**Enable Internal Bit Robbing Access** 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to send the bit robbing signaling information stored in the XS(12:1) (ESF, F12, 72) registers or serial CAS in the corresponding time slots.
XLD	5	rw	**Transmit Line Loop-Back (LLB) Down Code** 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down code is overwritten by the framing/DL/CRC bits optionally.
XLU	4	rw	**Transmit LLB Up Code** 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB up (activate) code continuously until this bit is reset. The LLB up code is optionally overwritten by the framing/DL/CRC bits. For proper operation bit FMR5.XLD must be cleared.

Field	Bits	Type	Description
XTM	2	rw	**Transmit Transparent Mode** 0_B , Ports $\overline{SYPX}$/XMFS define the frame/multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FS/DL-bits according to this framing. Any change of the transmit time slot assignment subsequently produces a change of the FS/DL-bit positions. 1_B , Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to actualize the multiframe position. The framing (FS/DL-bits) generated by the transmitter are not “disturbed“ (in case of changing the transmit time slot assignment) by the transmit system highway unless register XC1 is written. This bit should be set if loop-timed application is selected. For proper operation the transmit elastic buffer (2 frames, SIC1.XBS(1:0) = ´10b´) has to be enabled.
SSC2	1	rw	**Select Sync Conditions** Only valid in ESF framing format. Loss of Frame Alignment FRS0.LFA is declared if more than 320 CRC6 errors per second interval are detected.

Transmit Control 0

XC0_T	Offset	Reset Value
Transmit Control 0	$xx22_H$	00_H

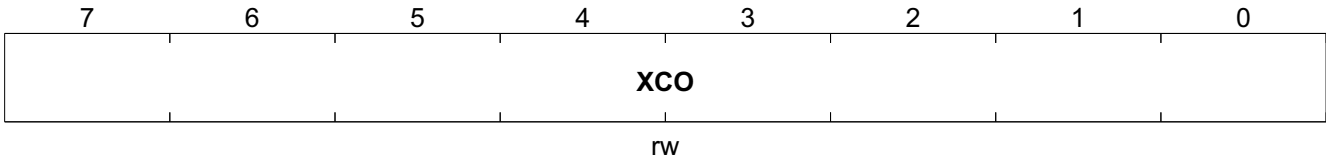
7	6	5	4	3	2	1	0
BRM	MFBS	BRIF	BRFO		XCO10	XCO9	XCO8
rw	rw	rw	rw		rw	rw	rw

Field	Bits	Type	Description
BRM	7	rw	**Enable Bit Robbing Marker** A one in this bit marks the robbed bit positions on the system highway. RSIGM marks the receive and XSIGM marks the transmit robbed bits.
MFBS	6	rw	**Enable pure Multiframe Begin Signals** Only valid if ESF or F72 format is selected. 0_B , RMFB marks the beginning of every received superframe. Additional pulses are provided every 12 frames when using ESF/F24 or F72 format. 1_B , RMFB marks the beginning of every received multiframe.
BRIF	5	rw	**Bit Robbing Idle Function** Note that the bit robbing idle feature is not operational in serial CAS together with F72 mode. 0_B , bit robbing information is overwritten in idle channels. 1_B , bit robbing information is not overwritten in idle channels.
BRFO	4:3	rw	**Bit Robbing Force One** Setting this bit forces the robbed bits high transmitted on port RDO. The received signaling data stream for the signaling controller is not influenced by this bit.(CAS-BR information can be transferred to the system interface or be set to a fixed value.) 00_B , robbed bits are transferred on RDO as they are received (default). 01_B , robbed bits are forced high on RDO, even if marked as "cleared channels". 10_B , reserved. 11_B , robbed bits are forced high on RDO except for those channels which are marked as "cleared channels".
XCO10	2	rw	**Transmit Offset** Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse on port $\overline{\text{SYPX}}$ or XMFS is active Refer to register XC1.
XCO9	1		
XCO8	0		

Transmit Control 1

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating the value should only be done when the OctalFALCTM is initialized or when the buffer should be centered. As a consequence a transmit slip will occur. See **Chapter 5.6.3.1**.

XC1_T	Offset	Reset Value
Transmit Control 1	$xx23_H$	$9C_H$



Field	Bits	Type	Description
XCO	7:0	rw	**Transmit Offset** Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse on port SYPX/XMFS is active.Calculation of delay time T (SCLKX cycles) depends on the value X of the transmit offset register XC(1:0): • System clocking rate: Modulo 2.048 MHz (SIC2.SSC2 = 0): 0 ≤ T ≤ 4: X = 4 - T and 5 ≤ T ≤ maximum delay: X = 256 x SC/SD - T + 4) with maximum delay = (256 x SC/SD) -1, with SC = system clock defined by SIC1.SSC(1:0)+SIC2.SSC2 and with SD = 2.048 Mbit/s (system clocking n x 2.048 MHz). • System clocking rate: modulo 1.544 MHz (SIC2.SSC2 = 1): 0 ≤ T ≤ 4: X = 4- T + 7 x SC/BF and 5 ≤ T ≤ maximum delay: X = 200 x SC/BF - T + 3 with SC = system clock defined by SIC1.SSC(1:0)+SIC2.SSC2, SD = 1.544 Mbit/s (system clocking n x 1.544 MHz) and with BF = basic frequency = 1.544 MHz. T = Time between the active edge of SCLKX after $\overline{SYPX}$ pulse begin and beginning of the next frame (F-bit, channel phase 0), measured in number of SCLKX clock intervals; maximum delay: T_{max} = (200 x SC/BF) - (7 x SC/BF) - 1. See **Chapter 5.6.3.1** for further description.

Receive Control 0

RC0_T	Offset	Reset Value
Receive Control 0	$xx24_H$	00_H

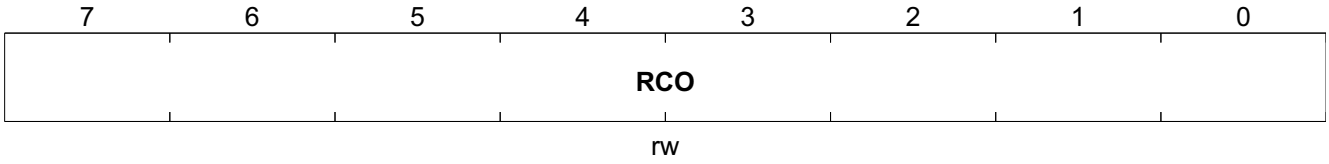
7	6	5	4	3	2	1	0
SJR	RRAM	CRCI	XCRCI	RDIS	RCO10	RCO9	RCO8
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SJR	7	rw	**Select Japanese ITU-T Requirements** 0_B , T1: Alarm handling is done according ITU-T G. 704+706 1_B , J1: Alarm handling is done according ITU-T JG. 704+706
RRAM	6	rw	**Receive Remote Alarm Mode** The conditions for remote (yellow) alarm (FRS0.RRA) detection can be selected by this bit to allow detection even in the presence of a bit error rate of up to 10^{-3}. 0_B : Detection: F4: Bit2 = ´0´ in every speech channel per frame. F12: FMR0.SRAF = ´0´: bit2 = ´0´ in every speech channel per frame; FMR0.SRAF = ´1´: S-bit of frame 12 is forced to ´1´ ESF: FMR0.SRAF = ´0´: pattern “1111 1111 0000 0000” in data link channel; FMR0.SRAF = ´1´: bit2 = ´0´ in every speech channel F72: Bit2 = ´0´ in every speech channel per frame. Release: The alarm is reset when above conditions are no longer detected 1_B : Detection, bit error rate 10^{-3}: F4: Bit2 = ´0´ in 255 consecutive speech channels. F12: FMR0.SRAF = ´0´: bit 2 = ´0´ in 255 consecutive speech channels; FMR0.SRAF = ´1´: S-bit of frame 12 is forced to ´1´ ESF: FMR0.SRAF = ´0´: pattern “1111 1111 0000 0000” in data link channel; FMR0.SRAF = 1: bit 2 = ´0´ in 255 consecutive speech channels F72: Bit 2 = ´0´ in 255 consecutive speech channels. Release: Depending on the selected multiframe format the alarm is reset when OctalFALCTM does not detect - the “bit 2 = 0" condition for three consecutive pulse frames (all formats if selected) - the "FS-bit" condition for three consecutive multiframes (F12) - the "DL pattern" for three times in a row (ESF)

Field	Bits	Type	Description
CRCI	5	rw	**Automatic CRC6 Bit Inversion** If set, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe. This function is logically ored with RC0.XCRCI.
XCRCI	4	rw	**Transmit CRC6 Bit Inversion** If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ored with RC0.CRCI.
RDIS	3	rw	**Receive Data Input Sense** Digital interface, dual-rail: 0_B , Inputs RDIP/RDIN are active low 1_B , Inputs RDIP/RDIN are active high **Receive Data Input Sense** Digital interface, CMI: 0_B , Input ROID is active high 1_B , Input ROID is active low
RCO10	2	rw	**Receive Offset/Receive Frame Marker Offset** Depending on the RP(A to D) pin function different offsets can be programmed. The SYPR and the RFM pin function cannot be selected in parallel. Receive Offset (PC(3:1).RPC(3:0) = ´0000_b´) Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse on port SYPR is active.Calculation of delay time T (SCLKR cycles) depends on the value X of the receive offset register RC(1:0). Refer to register RC1.
RCO9	1		
RCO8	0		

Receive Control 1

RC1_T	Offset	Reset Value
Receive Control 1	$xx25_H$	$9C_H$



Field	Bits	Type	Description
RCO	7:0	rw	**Receive Offset/Receive Frame Marker Offset** Depending on the RP(A to D) pin function different offsets can be programmed. The SYPR and the RFM pin function cannot be selected in parallel. **Receive Offset** **Receive Frame Marker Offset**

Receive Offset

PC(3:1).RPC(3:0) =´0000_b´): Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse on port $\overline{\text{SYPR}}$ is active. Calculation of delay time T (SCLKR cycles) depends on the value X of the receive offset register RC(1:0).

CASE A: system clocking rate: modulo 2.048 MHz (SIC2.SSC2 = ´0´)

$0 \leq T \leq 4$: X = 4 - T

$5 \leq T \leq$ maximum delay: X = 2052 - T

- Maximum delay = (256 x SC/SD) -1
- SC = system clock defined by SIC1.SSC(1:0)+SIC2.SSC
- SD = system data rate

CASE B: system clocking rate: modulo 1.544 MHz (SIC2.SSC2 = ´1´)

$0 \leq T \leq 4$: X = 4 - T + (7 x SC/SD)

$5 \leq T \leq$ maximum delay: X = (200 x SC/SD) + 4 - T

- Maximum delay = 193 x SC/SD - 1
- SC = system clock defined by SIC1.SSC(1:0) and SIC2.SSC2
- SD = system data rate
- Delay time T = time between beginning of time slot 0 at RDO and the initial edge of SCLKR after $\overline{\text{SYPR}}$ goes active.

See **Chapter 5.6.2.1** for further description.

Receive Frame Marker Offset

PC(3:1).RPC(3:0) = ´0001_b´: Offset programming of the receive frame marker which is output on multifunction port RFM. The receive frame marker can be activated during any bit position of the entire frame and depends on the selected system clock rate.Calculation of the value X of the receive offset register RC(1:0) depends on the bit position which should be marked at marker position MP:

CASE A: System clocking rate: modulo 2.048 MHz (SIC2.SSC2 = ´0´):

0 ≤ MP ≤ 2045: X = MP + 2

2046 ≤ MP ≤ 2047: X = MP - 2046) :

e.g: 2.048 MHz: MP = 0 to 255; 4.096 MHz: MP = 0 to 511, 8.192 MHz: MP = 0 to 1023, 16.384 MHz: MP = 0 to 2047.

CASE B: System clocking rate: modulo 1.544 MHz (SIC2.SSC2 = ´1´) :

0 ≤ MP ≤ 193 x (SC/SD) - 3: X = MP + 2 + 7 x SC/SD

193 x (SC/SD) -2 ≤ MP ≤ maximum delay: X = MP + 2 - 186 x SC/SD

- Maximum delay = 193 x SC/SD - 1
- SC = system clock defined by SIC1.SSC(1:0) and SIC2.SSC2
- SD = system data rate

See **Chapter 5.6.2.1** for further description.

Transmit Pulse Mask 0

See Chapter 3.7.5 and Chapter 3.7.5.1. The transmit pulse shape which is defined in ITU-T G.703 is output on pins XL1 and XL2. The level of the pulse shape can be programmed by registers XPM(2:0) if XPM2.XPDIS is set to ´0´ to create a custom waveform. If XPM2.XPDIS is set to ´1´, the custom waveform can be programed by the registers TXP(16:1) and the register bits of XPM(2:0) are unused with exception of the bits XPM2.XLT, XPM2.DAXLT and XPM2.XPDIS. In order to get an optimized pulse shape for the external transformers each pulse shape is internally divided into four sub pulse shapes if XPM2.XPDIS is set to ´0´. In each sub pulse shape a programmed 5-bit value defines the level of the analog voltage on pins XL1/2. Together four 5-bit values have to be programmed to form one complete transmit pulse shape. The four 5-bit values are sent in the following sequence:

XP04 to 00: First pulse shape level

XP14 to 10: Second pulse shape level

XP24 to 20: Third pulse shape level

XP34 to 30: Fourth pulse shape level.

Changing the LSB of each subpulse in registers XPM(2:0) changes the amplitude of the differential voltage on XL1/2 by approximately 80 mV. Recommended values for standard applications are given in Table 22 and Table 23.

Note that in the special cases were the LBO pulse masks are performed in T1 mode, the programming of the pulse masks is done internally, independent on the settings in XPM(2:0).

XPM0_T	Offset	Reset Value
Transmit Pulse Mask0	$xx26_H$	$7B_H$

7	6	5	4	3	2	1	0
XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XP12	7	rw	**Bit 2 of second pulse shape level**
XP11	6	rw	**Bit 1 of second pulse shape level**
XP10	5	rw	**Bit 0 (LSB) of second pulse shape level**
XP04	4	rw	**Bit 4 (MSB) of first pulse shape level**
XP03	3	rw	**Bit 3 of first pulse shape level**
XP02	2	rw	**Bit 2 of first pulse shape level**
XP01	1	rw	**Bit 1 of first pulse shape level**
XP00	0	rw	**Bit 0 (LSB) of first pulse shape level**

Transmit Pulse Mask 1

For description see **Transmit Pulse Mask 0**

XPM1_T	Offset	Reset Value
Transmit Pulse Mask1	**$xx27_H$**	**03_H**

7	6	5	4	3	2	1	0
XP30	**XP24**	**XP23**	**XP22**	**XP21**	**XP20**	**XP14**	**XP13**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XP30	7	rw	**Bit 0 (LSB) of fourth pulse shape level**
XP24	6	rw	**Bit 4 (MSB) of third pulse shape level**
XP23	5	rw	**Bit 3 of third pulse shape level**
XP22	4	rw	**Bit 2 of third pulse shape level**
XP21	3	rw	**Bit 1of third pulse shape level**
XP20	2	rw	**Bit 0 (LSB) of third pulse shape level**
XP14	1	rw	**Bit 4 (MSB) of second pulse shape level**
XP13	0	rw	**Bit 3 of second pulse shape level**

Transmit Pulse-Mask Register 2

For description see **Transmit Pulse Mask 0**

XPM2_T	Offset	Reset Value
Transmit Pulse-Mask Register 2	**xx28$_H$**	**40$_H$**

7	6	5	4	3	2	1	0
0	**XLT**	**DAXLT**	**XPDIS**	**XP34**	**XP33**	**XP32**	**XP31**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
0	7	rw	**Fixed 0**
XLT	6	rw	**Transmit Line Tristate** 0_B , Normal operation 1_B , Transmit line XL1/XL2 or XDOP/XDON are switched into high-impedance state. If this bit is set the transmit line monitor status information is frozen (default value after hardware reset).
DAXLT	5	rw	**Disable Automatic Tristating of XL1/2** 0_B , Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high-impedance state. 1_B , If a short is detected on pins XL1/2, the automatic setting of these pins into a high-impedance state (by the XL-monitor) is disabled.
XPDIS	4	rw	**Disable XPM Values** 0_B , XP values from registers XPM(2:0) are used for pulse shaping. 1_B , TXP values from registers TXP(16:1) are used for pulse shaping.
XP34	3	rw	**Bit 4 (MSB) of second pulse shape level**
XP33	2	rw	**Bit 3 of fourth pulse shape level**
XP32	1	rw	**Bit 2 of fourth pulse shape level**
XP31	0	rw	**Bit 1 of fourth pulse shape level**

Table 111 Transmit Pulse-Mask Registers

	7	6	5	4	3	2	1	0
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13
XPM2	0	XLT	DAXLT	XPDIS	XP34	XP33	XP32	XP31

System Interface Control Register 4

This register configures the clock edge selection of the system interface signals $\overline{\text{SYPR}}$ and $\overline{\text{SYPX}}$ in relation to the clock edge used for the data.

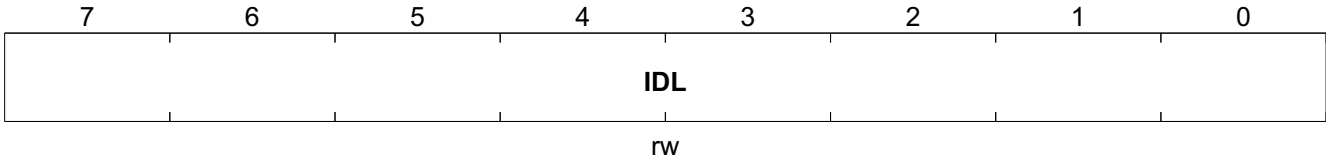
SIC4_T	Offset	Reset Value
System Interface Control Register 4	$xx2A_H$	00_H

7	6	5	4	3	2	1	0
Res					CES	SYPRCE	SYPXCE
					rw	rw	rw

Field	Bits	Type	Description
CES	2	rw	**Clock Edge Selection Enable** This bit enables the function of SYPRCE and $\overline{\text{SYPX}}$CE. 0_B , SYPRCE and SYPXCE are disabled. ($\overline{\text{SYPR}}$ and $\overline{\text{SYPX}}$ are clocked by the same edge as receive interface data and marker.) 1_B , SYPRCE and SYPXCE are enabled.
SYPRCE	1	rw	**SYPR Clock Edge Selection** See **Chapter 5.6**. 0_B , $\overline{\text{SYPR}}$ is clocked by the same edge as receive interface data and marker, see **SIC1_T**. 1_B , $\overline{\text{SYPR}}$ is clocked by the opposite edge as receive interface data and marker, see **SIC1_T**.
SYPXCE	0	rw	**SYPX Clock Edge Selection** See **Chapter 5.6**. 0_B , $\overline{\text{SYPX}}$ is clocked by the same edge as transmit interface data and marker, see **SIC1_T**. 1_B , $\overline{\text{SYPX}}$ is clocked by the opposite edge as transmit interface data and marker, see **SIC1_T**.

Idle Channel Code Register

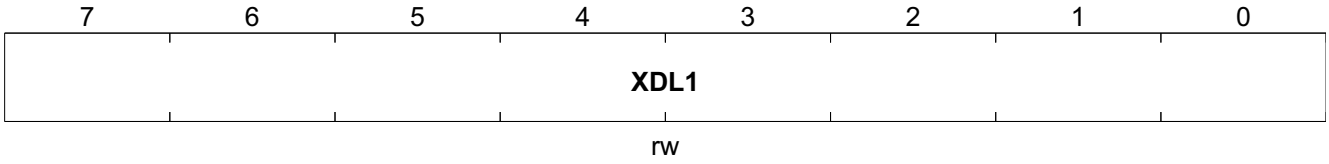
IDLE_T	Offset	Reset Value
Idle Channel Code Register	$xx2B_H$	00_H



Field	Bits	Type	Description
IDL	7:0	rw	**Idle Channel Code** If channel loop-back is enabled by programming the register LOOP.ECLB = ´1´, the contents of the assigned outgoing channel on ports XL1/XL2 or XDOP/XDON is set equal to the idle channel code selected by this register. Additionally, the specified pattern overwrites the contents of all channels of the outgoing PCM frame selected by the idle channel registers ICB(3:1). IDL7 is transmitted first.

Transmit DL-Bit Register 1

XDL1_T	Offset	Reset Value
Transmit DL-Bit Register 1	xx2C$_H$	00$_H$



Field	Bits	Type	Description
XDL1	7:0	rw	**Transmit FS/DL-Bit Data** The DL-bit register access is enabled by setting bits FMR1.EDL = ´1´. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XDL(3:1) is copied into a shadow register. The contents is subsequently sent out in the data stream of the next outgoing multiframe if no transparent mode is enabled. XDL10 is sent out first. In F4 frame format only XDL10+XDL11 are transmitted. In F24 frame format XDL10 to 23 are shifted out. In F72 frame format XDL10 to 37 are transmitted. The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, the current contents is repeated.

Similar Registers

Registers XDL2 and XDL3 have the same layout and description.

The Offset Addresses are listed in **XDLn Overview**, for bit names refer to **Transmit DL-Bit Registers**

Table 112 XDLn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
XDL2	Transmit DL-Bit Register 2	2D$_H$	
XDL3	Transmit DL-Bit Register 3	2E$_H$	

Table 113 Transmit DL-Bit Registers

	7	6	5	4	3	2	1	0
XDL1	XDL17	XDL16	XDL15	XDL14	XDL13	XDL12	XDL11	XDL10
XDL2	XDL27	XDL26	XDL25	XDL24	XDL23	XDL22	XDL21	XDL20
XDL3	XDL37	XDL36	XDL35	XDL34	XDL33	XDL32	XDL31	XDL30

Clear Channel Register 1

CCB1_T	Offset	Reset Value
Clear Channel Register 1	$xx2F_H$	00_H

7	6	5	4	3	2	1	0
CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CH1	7	rw	**Channel Selection Bits**
CH2	6		
CH3	5		0_B , Normal operation. Bit robbing information and zero code suppression (ZCS, B7 stuffing) can change contents of the selected speech/data channel if assigned modes are enabled by bits FMR5.EIBR and FMR0.XC(1:0).
CH4	4		
CH5	3		
CH6	2		1_B , Clear channel mode. Contents of selected speech/data channel are not overwritten by internal or external bit robbing and ZCS information. Transmission of channel assigned signaling and control of pulse-density is applied by the user.
CH7	1		
CH8	0		

Similar Registers

Registers CCB2 and CCB3 have the same description.

The Offset Addresses are listed in **CCBn Overview**, for layout and bit names refer to **Clear Channel Registers**

Table 114 CCBn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CCB2	Clear Channel Register 2	30_H	
CCB3	Clear Channel Register 3	31_H	

Table 115 Clear Channel Registers

	7	6	5	4	3	2	1	0
CCB1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
CCB2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
CCB3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24

Idle Channel Register 1

ICB1_T	Offset	Reset Value
Idle Channel Register 1	$xx32_H$	00_H

7	6	5	4	3	2	1	0
IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IC1	7	rw	**Idle Channel Selection Bits** These bits define the channels (time slots) of the outgoing PCM frame to be altered. 0_B , Normal operation. 1_B , Idle channel mode. The contents of the selected channel is overwritten by the idle channel code defined by register IDLE.
IC2	6		
IC3	5		
IC4	4		
IC5	3		
IC6	2		
IC7	1		
IC8	0		

Similar Registers

Registers ICB2 and ICB3 have the same description.

The Offset Addresses are listed in **ICBn Overview**, for layout and bit names refer to **Idle Channel Registers**

Table 116 ICBn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
ICB2	Idle Channel Register 2	33_H	
ICB3	Idle Channel Register 3	34_H	

Table 117 Idle Channel Registers

	7	6	5	4	3	2	1	0
ICB1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8
ICB2	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16
ICB3	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24

Line Interface Mode 0

LIM0_T	Offset	Reset Value
Line Interface Mode 0	$xx36_H$	00_H

7	6	5	4	3	2	1	0
XFB	XDOS	RTRS	DCIM	EQON	RLM	LL	MAS
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XFB	7	rw	**Transmit Full Bauded Mode** Only applicable for dual-rail mode (bit LIM1.DRS = ´1´). *Note: If CMI coding is selected (FMR0.XC(1:0) = ´01_b´) this bit has to be cleared.* 0_B , Output signals XDOP/XDON are half bauded (normal operation). 1_B , Output signals XDOP/XDON are full bauded.
XDOS	6	rw	**Transmit Data Out Sense** *Note: If CMI coding is selected (FMR0.XC(1:0) = ´01_b´) this bit has to be cleared.The transmit frame marker XFM is independent of this bit.* 0_B , Output signals XDOP/XDON are active low. Output XOID is active high (normal operation). 1_B , Output signals XDOP/XDON are active high. Output XOID is active low.
RTRS	5	rw	**Receive Termination Resistance Selection** This bit controls the analog switch of the receive line interface, see Chapter 3.6.6. *Note: If the RLT functionality is selected at one of the multi function ports, a logical equivalence is build out of RTRS and RLT for controlling the analog switch. If RLT functionality is not configured at one of the multi function ports, the analog switch is controlled only by RTRS.* 0_B , analog switch is switched off. 1_B , analog switch is switched on.
DCIM	4	rw	**Digital Clock Interface Mode** *Note: DCO-X must be used in DCIM mode (CMR1.DXJA = ´0´).* 0_B , normal operation. 1_B , enables the digital Clock Interface Mode (synchronization interface mode) according to ITU-T G.703, Section 13. A 2048/1544 kHz clock is expected on RL1/2. On XL1/2 a 2048/1544 kHz output clock is driven. The transmit clock signal on XL1/2 is derived from the clock supplied on SCLKX (CMR1.DXSS = ´0´).

Field	Bits	Type	Description
EQON	3	rw	**Receive Equalizer On** *Note: This function is no longer used. The receive equalizer automatically adapts to the incoming signal level. This bit is ignored to assure software compatibility with QuadFALC®.*
RLM	2	rw	**Receive Line Monitoring** See **Chapter 3.6.7**. 0_B , Normal receiver mode 1_B , Receiver mode for receive line monitoring; the receiver sensitivity is increased to detect resistively attenuated signals of -20 dB (short-haul mode only)
LL	1	rw	**Local Loop** See **Chapter 5.7.4**. 0_B , Normal operation 1_B , Local loop active. The local loop-back mode disconnects the receive lines RL1/RL2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface is routed through the analog receiver back to the system interface. The unipolar bit stream is transmitted undisturbedly on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transferred through the complete analog receiver.
MAS	0	rw	**Master Mode** See **Chapter 3.6.5**. 0_B , Slave mode 1_B , Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (1.544, 2.048 MHz or 8 kHz, see IPC.SSYF, LIM1.DCOC) supplied by SYNC. If this pin is connected to VSS or VDD (or left open and pulled up to VDD internally) the DCO-R circuitry is centered and no receive jitter attenuation is performed (only if 1.544 or 2.048 MHz clock is selected by resetting bit IPC.SSYF). The generated clocks are stable.

Line Interface Mode 1

LIM1_T	Offset	Reset Value
Line Interface Mode 1	$xx37_H$	80_H

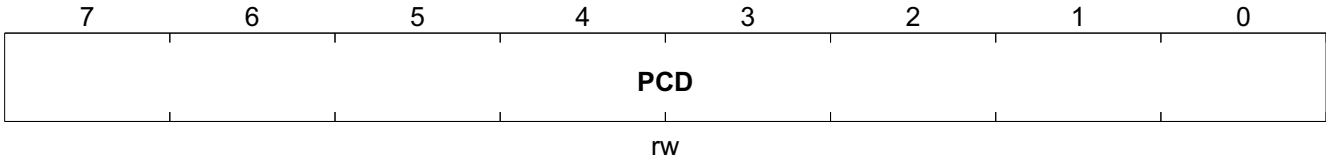
7	6	5	4	3	2	1	0
CLOS	RIL			DCOC	JATT	RL	DRS
rw	rw			rw	rw	rw	rw

Field	Bits	Type	Description
CLOS	7	rw	**Clear data in case of LOS** 0_B , Normal receiver mode, receive data stream is transferred normally in long-haul mode 1_B , In long-haul mode received data is cleared (driven low), as soon as LOS is detected
RIL	6:4	rw	**Receive Input Threshold** Only valid if analog line interface is selected (LIM1.DRS = 0). “No signal” is declared if the voltage between pins RL1 and RL2 drops below the limits programmed by bits RIL(2:0) and the received data stream has no transition for a period defined in the PCD register. See **Chapter 5.1.2** and the DC characteristics (**Table 139**) for detail.
DCOC	3	rw	**DCO-R Control** *Note: If IPC.SSYF = ´1´, external reference clock frequency is 8.0 kHz independent of DCOC.* 0_B , 1.544 MHz reference clock for the DCO-R circuitry provided on pin SYNC. 1_B , 2.048 MHz reference clock for the DCO-R circuitry provided on pin SYNC.
JATT	2	rw	**Transmit Jitter Attenuator** See **Chapter 3.7.4** and **Chapter 5.7.2**. *Note: JATT is only used to define the jitter attenuation during remote loop operation. Remote loop operation can be set by LIM1.RL or by automatic loop switching by BOM messages. Jitter attenuation during normal operation is not affected by JATT.* 0_B , Transmit jitter attenuator is disabled for remote Loop. Transmit data bypasses the remote loop jitter attenuator buffer. 1_B , Jitter attenuator is active for remote loop . Received data from pins RL1/2 or RDIP/N or ROID is sent "jitter-free" on ports XL1/2 or XDOP/N or XOID. The de-jittered clock is generated by the DCO-X circuitry.

Field	Bits	Type	Description
RL	1	rw	**Remote Loop** See **Chapter 5.7.2**. *Note: RL is logically ored with automatic loop switching by BOM messages.* 0_B , Normal operation. 1_B , Remote Loop active.
DRS	0	rw	**Dual-Rail Select** 0_B , The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs. 1_B , The digital dual-rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register

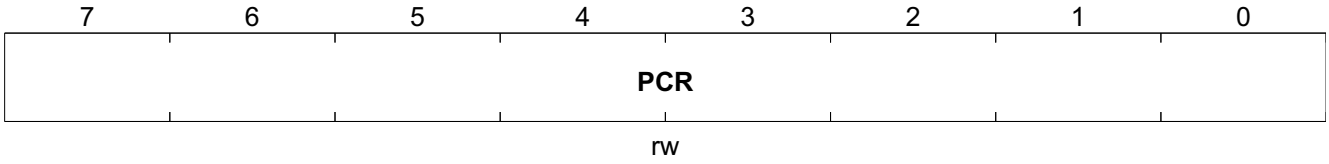
PCD_T	Offset	Reset Value
Pulse Count Detection Register	$xx38_H$	00_H



Field	Bits	Type	Description
PCD	7:0	rw	**Pulse Count Detection** A LOS alarm (red alarm) is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable by the PCD register and can be calculated as follows: T = 16 x (N+1); with 0 ≤ N ≤ 255. The maximum time is: 256 x 16 x 648 ns = 2.65 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery

PCR_T	Offset	Reset Value
Pulse Count Recovery	$xx39_H$	00_H



Field	Bits	Type	Description
PCR	7:0	rw	**Pulse Count Recovery** A LOS alarm (red alarm) is cleared if a pulse-density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable by the PCR register and can be calculated as follows: M = N+1; with $0 \leq N \leq 255$. The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared to the contents of PCR register. If the pulse number reaches or exceeds the PCR value the LOS alarm is reset otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval. An additional loss-of-signal recovery condition is selected by register LIM2.LOS1. See **Chapter 5.1.2**.

Line Interface Mode 2

LIM2_T	Offset	Reset Value
Line Interface Mode 2	$xx3A_H$	20_H

7	6	5	4	3	2	1	0
LBO2	LBO1	SLT		SCF	ELT	Res	LOS1
rw	rw	rw		rw	rw		rw

Field	Bits	Type	Description
LBO2	7	rw	**Line Build-Out** Selecting the transmitter attenuation is possible in steps of 7.5 dB at 772 kHz which is according to FCC68 and ANSI T1.403, see **Table 23**. To meet the line build-out defined by ANSI T1.403 registers XPM(2:0) should be programmed as follows: 00_B , 0 dB 01_B , 7.5 dB 10_B , -15 dB 11_B , -22.5 dB
LBO1	6		
SLT	5:4	rw	**Receive Slicer Threshold** 00_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 55% of the peak amplitude. 01_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 67% of the peak amplitude (may be used in some T1/J1 applications). 10_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 50% of the peak amplitude (default, recommended in T1/J1 mode). 11_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 45% of the peak amplitude.
SCF	3	rw	**Select Corner Frequency of DCO-R** Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.6 Hz, see **Chapter 3.6.5**. *Note: Reducing the corner frequency of the DCO-R circuitry increases the synchronization time of the DCO-R.*
ELT	2	rw	**Enable Loop-Timed** 0_B , Normal operation 1_B , Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register FMR5.XTM. For correct operation of loop timed the remote loop (bit LIM1.RL = 0) must be inactive and bit CMR1.DXSS must be cleared.

Field	Bits	Type	Description
LOS1	0	rw	**Loss-of-Signal Recovery condition** 0_B , The LOS alarm is cleared if the predefined pulse-density (register PCR) is detected during the time interval which is defined by register PCD. 1_B , Additionally to the recovery condition described above a LOS alarm is only cleared if the pulse-density is fulfilled and no more than 15 contiguous zeros are detected during the recovery interval (according to GR-499-CORE).

Loop Code Register 1

LCR1_T	Offset	Reset Value
Loop Code Register 1	$xx3B_H$	00_H

7	6	5	4	3	2	1	0
EPRM	XPRBS	LDC		LAC		FLLB	LLBP
rw	rw	rw		rw		rw	rw

Field	Bits	Type	Description
EPRM	7	rw	**Enable Pseudo-Random Binary Sequence** See **Chapter 5.7.1**. 0_B , Pseudo-random binary sequence (PRBS) monitor is disabled. 1_B , PRBS is enabled. Setting this bit enables incrementing the bit error counter BEC with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR3.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit FRS1.LLBAD.
XPRBS	6	rw	**Transmit Pseudo-Random Binary Sequence** A one in this bit position enables transmission of a pseudo-random binary sequence to the remote end. Depending on bit LLBP the PRBS is generated according to 2^{11} -1, 2^{15} -1, 2^{20} -1 or 2^{23} -1 (ITU-T O. 151). See **Chapter 5.7.1**.
LDC	5:4	rw	**Length Deactivate (Down) Code** These bits defines the length of the LLB deactivate code which is programmable in register LCR2. See **Chapter 5.5.7**. 00_B , Length: 5 bit 01_B , Length: 6 bit, 2 bit, 3 bit 10_B , Length: 7 bit 11_B , Length: 8 bit, 2 bit, 4bit
LAC	3:2	rw	**Length Activate (Up) Code** These bits defines the length of the LLB activate code which is programmable in register LCR3. See **Chapter 5.5.7**. 00_B , Length: 5 bit 01_B , Length: 6 bit, 2 bit, 3 bit 10_B , Length: 7 bit 11_B , Length: 8 bit, 2 bit, 4bit
FLLB	1	rw	**Framed Line Loop-Back/Invert PRBS** Depending on bit LCR1.XPRBS this bit enables different functions: LCR1.XPRBS =´ 0´: see table **FLLB Constant Values (Case 1)** LCR1.XPRBS =´ 1´: see table **FLLB Constant Values (Case 2)**
LLBP	0	rw	**Line Loop-Back Pattern** LCR1.XPRBS = ´0´: see table **LLBP Constant Values (Case 1)** LCR1.XPRBS = ´1´: see table **LLBP Constant Values (Case 2)**

Table 118 FLLB Constant Values (Case 1)

Name and Description	Value
Framed Line Loop-Back/Invert PRBS The line loop-back code is transmitted including framing bits. LLB code overwrites the FS/DL-bits.	0_B
Framed Line Loop-Back/Invert PRBS The line loop-back code is transmitted unframed. LLB code does not overwrite the FS/DL-bits.	1_B

Table 119 FLLB Constant Values (Case 2)

Name and Description	Value
Framed Line Loop-Back/Invert PRBS The generated PRBS is transmitted not inverted.	0_B
Framed Line Loop-Back/Invert PRBS The PRBS is transmitted inverted.	1_B

Table 120 LLBP Constant Values (Case 1)

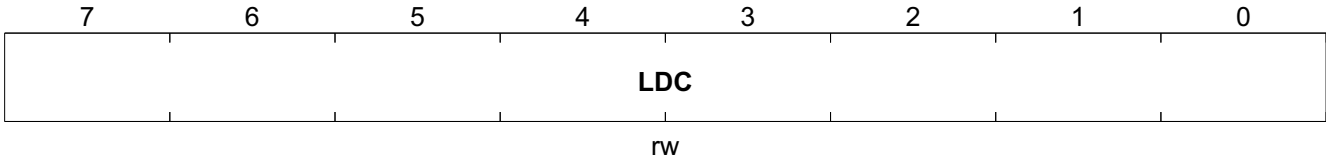
Name and Description	Value
Line Loop-Back Pattern Fixed line loop-back code according to ANSI T1. 403.	0_B
Line Loop-Back Pattern Enable user-programmable line loop-back code by register LCR2/3.	1_B

Table 121 LLBP Constant Values (Case 2)

Name and Description	Value
Line Loop-Back Pattern 2^{15} -1	0_B
Line Loop-Back Pattern 2^{20} -1	1_B

Loop Code Register 2

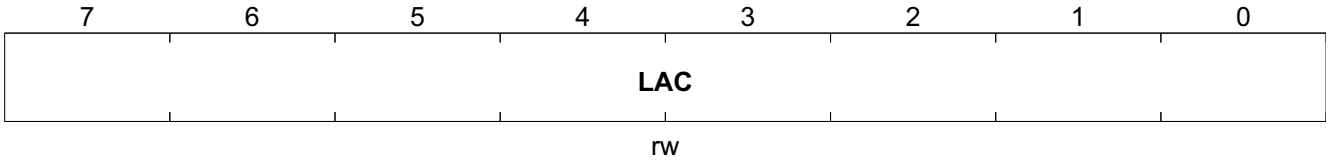
LCR2_T	Offset	Reset Value
Loop Code Register 2	$xx3C_H$	00_H



Field	Bits	Type	Description
LDC	7:0	rw	**Line Loop-Back Deactivate Code** If enabled by bit FMR5.XLD = ´1´ the LLB deactivate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared. If LCR2 is changed while the previous deactivate code has been detected and is still received, bit FRS1.LLBDD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´).

Loop Code Register 3

LCR3_T	Offset	Reset Value
Loop Code Register 3	$xx3D_H$	00_H



Field	Bits	Type	Description
LAC	7:0	rw	**Line Loop-Back Activate Code** If enabled by bit FMR5.XLU = ´1´ the LLB activate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.If LCR3 is changed while the previous activate code has been detected and is still received, bit FRS1.LLBAD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´).

System Interface Control 1

SIC1_T	Offset	Reset Value
System Interface Control 1	$xx3E_H$	00_H

7	6	5	4	3	2	1	0
SSC1	SSD1	RBS		SSC0	BIM	XBS	
rw	rw	rw		rw	rw	rw	

Field	Bits	Type	Description
SSC1	7	rw	**Select System Clock** SIC1.SSC(1:0) and SIC2.SSC2 define the clocking rate on the system highway, see **Chapter 5.6**. SIC2.SSC2 = ´0´: See table **SSC1 Constant Values (Case 1)** *Note: SIC2.SSC2 = ´1´: See table **SSC1 Constant Values (Case 2)***
SSD1	6	rw	**Select System Data Rate 1** SIC1.SSD1, FMR1.SSD0 and SIC2.SSC2 define the data rate on the system highway. SIC2.SSC2 = ´0´: See table **SSD1 Constant Values (Case 1)** *Note: SIC2.SSC2 = ´1´: See table **SSD1 Constant Values (Case 2)***
RBS	5:4	rw	**Receive Buffer Size** See **Chapter 5.1.7**, **Table 44**. 00_B , Buffer size: 2 frames 01_B , Buffer size: 1 frame 10_B , Buffer size: 96 bits 11_B , Bypass of receive elastic store
SSC0	3	rw	**Select System Clock** See bit SSC1.
BIM	2	rw	**Bit Interleaved Mode** Only applicable if bit SIC2.SSC2 is cleared. If SIC2.SSC2 is set high, the bit interleaved mode is automatically performed. 0_B , Byte interleaved mode 1_B , Bit interleaved mode
XBS	1:0	rw	**Transmit Buffer Size** See **Chapter 5.2.1**. 00_B , Bypass of transmit elastic store 01_B , Buffer size: 1 frame 10_B , Buffer size: 2 frames 11_B , Buffer size: 96 bits

Table 122 SSC1 Constant Values (Case 1)

Name and Description	Value
System Clock 2.048 MHz	00_B
System Clock 4.096 MHz	01_B
System Clock 8.192 MHz	10_B
System Clock 16.384 MHz	11_B

Table 123 SSC1 Constant Values (Case 2)

Name and Description	Value
System Clock 1.544 MHz	00_B
System Clock 3.088 MHz	01_B
System Clock 6.176 MHz	10_B
System Clock 12.352 MHz	11_B

Table 124 SSD1 Constant Values (Case 1)

Name and Description	Value
System Data Rate 1 2.048 Mbit/s	00_B
System Data Rate 1 4.096 Mbit/s	01_B
System Data Rate 1 8.192 Mbit/s	10_B
System Data Rate 1 16.384 Mbit/s	11_B

Table 125 SSD1 Constant Values (Case 2)

Name and Description	Value
System Data Rate 1 1.544 Mbit/s	00_B
System Data Rate 1 3.088 Mbit/s	01_B
System Data Rate 1 6.176 Mbit/s	10_B
System Data Rate 1 12.352 Mbit/s	11_B

System Interface Control 2

SIC2_T	Offset	Reset Value
System Interface Control 2	$xx3F_H$	00_H

7	6	5	4	3	2	1	0
FFS	SSF	CRB	SSC2	SICS			Res
rw	rw	rw	rw	rw			

Field	Bits	Type	Description
FFS	7	rw	**Force Freeze Signaling** Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is started again. The freeze signaling status can also be generated automatically by detection of a loss-of-signal alarm or a loss of frame alignment or a receive slip (only if external register access through RSIG is enabled). This automatic freeze signaling function is logically ored with this bit. The current internal freeze signaling status is output on pin RP(A to C) with selected pin function FREEZE (PC(3:1).RPC(3:0) = ´0110_b´). Additionally this status is also available in register SIS.SFS.
SSF	6	rw	**Serial Signaling Format** Only applicable if pin function RSIG/XSIG and SIC3.TTRF = ´0´ is selected. 0_B , Bits 1 to 4 in all time slots except time slot 0 are cleared. 1_B , Bits 1 to 4 in all time slots except time slot 0 are set high.
CRB	5	rw	**Center Receive Elastic Buffer** Only applicable if the time slot assigner is disabled (PC(3:1).RPC(3:0) = ´0001_b´), no external or internal synchronous pulse receive is generated. A transition from low to high forces a receive slip and the read pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 1.544 MHz periods before it is cleared.
SSC2	4	rw	**Select System Clock** This bit together with SIC1.SSC(1:0) enables the system interface to run with a clock of 1.544, 3.088, 6.176 or 12.352 MHz (SSC2 = ´1´) or 2.048, 4.096, 8.192 or 16.384 MHz (SSC2 = ´0´). See also register SIC1.SSC(1:0).

Field	Bits	Type	Description
SICS	3:1	rw	**System Interface Channel Select** Only applicable if the system clock rate is greater than 1.544/2.048 MHz. Received data is transmitted on pin RDO/RSIG or received on XDI/XSIG with the selected system data rate. If the data rate is greater than 1.544/2.048 Mbit/s the data is output or sampled in half, a quarter or one eighth of the time slot. Data is not repeated. The time while data is active during a 8 x 488/648 ns time slot is called a channel phase. RDO/RSIG are cleared (driven to low level) while XDI/XSIG are ignored for the remaining time of the 8 x 488/648 ns or for the remaining channel phases. The channel phases are selectable with these bits. 000_B , Data active in channel phase 1, valid if system data rate is 16/8/4 or 12/6/3 Mbit/s 001_B , Data active in channel phase 2, valid if data rate is 16/8/4 or 12/6/3 Mbit/s 010_B , Data active in channel phase 3, valid if data rate is 16/8 or 12/6 Mbit/s 011_B , Data active in channel phase 4, valid if data rate is 16/8 or 12/6 Mbit/s 100_B , Data active in channel phase 5, valid if data rate is 16 or 12 Mbit/s 101_B , Data active in channel phase 6, valid if data rate is 16 or 12 Mbit/s 110_B , Data active in channel phase 7, valid if data rate is 16 or 12 Mbit/s 111_B , Data active in channel phase 8, valid if data rate is 16 or 12 Mbit/s

System Interface Control 3

SIC3_T	Offset	Reset Value
System Interface Control 3	$xx40_H$	00_H

7	6	5	4	3	2	1	0
CMI	**RRTRI**	**RTRI**	**FSCT**	**RESX**	**RESR**	**TTRF**	**DAF**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CMI	7	rw	**Select CMI Precoding** Only valid if CMI code (FMR0.XC(1:0) = ´01_b´) is selected. This bit defines the CMI precoding and influences transmit and receive data. *Note: Before local loop is closed, B8ZS precoding has to be switched off.* 0_B , CMI with B8ZS precoding 1_B , CMI without B8ZS precoding
RRTRI	6	rw	**RSIG/RDO Tristate Mode** See **Table 19**. *Note: RRTRI is logically exored with RTDMT multi function port, if this function is selected. RTDMT exor RRTRI sets additionally RFM and SCLKR into tristate.* 00_B , normal operation (RSIG and RDO are switched to low level during inactive channel/bit phases). 01_B , RSIG and RDO are switched into tristate mode during inactive channel/bit phases. 10_B , RSIG and RDO are tristate constantly (and also RFM and SCLKR). 11_B , RSIG and RDO are tristate constantly (and also RFM and SCLKR).
RTRI	5		
FSCT	4	rw	**FSC Tristate Mode** *Note: If SEC/FSC is selected as SEC input, this bit is ignored.* 0_B , normal operation of SEC/FSC pin. 1_B , SEC/FSC is switched into tristate mode.

Field	Bits	Type	Description
RESX	3	rw	**Rising Edge Synchronous Pulse Transmit** Depending on this bit all transmit system interface data are clocked (outputs) or sampled (inputs) with the selected active edge. See **Chapter 5.6** and **SIC4_T**. Only valid if CMR2.IXSC = ´0´: *Note: CMR2.IXSC = ´1´: value of RESX bit has no impact on the selected edge of the system interface clock but value of RESR bit is used as RESX. Example: If RESR = ´0´, the rising edge of system interface clock is the selected one for sampling data on XDI and vice versa. Active edge of the transmit marker is also controlled by SIC4.SYPX.* 0_B , Clocked or sampled with the first falling edge of the selected system interface clock. 1_B , Clocked or sampled with the first rising edge of the selected system interface clock.
RESR	2	rw	**Rising Edge Synchronous Pulse Receive** Depending on this bit all receive system interface data are clocked (outputs) or sampled (inputs) with the selected active edge. See **Chapter 5.6** and **SIC4_T**. *Note: If bit CMR2.IRSP is set, the behavior of signal RFM (if used) is inverse (´1´ = falling edge, ´0´ = rising edge). Active edge of the receive marker is also controlled by SIC4.SYPR.* 0_B , Clocked or sampled with the first falling edge of the selected system interface clock. 1_B , Clocked or sampled with the first rising edge of the selected system interface clock.
TTRF	1	rw	**TTR Register Function (Fractional T1/J1 Access)** Setting this bit the function of the TTR(4:1) registers are changed. A one in each TTR register forces the XSIGM marker high for the corresponding time slot and controls sampling of the time slots provided on pin XSIG. XSIG is selected by PC(3:1).XPC(3:0).
DAF	0	rw	**Disable Automatic Freeze** 0_B , Signaling is automatically frozen if one of the following alarms occurred: Loss-Of-signal (FRS0.LOS), Loss-of-Frame- Alignment (FRS0.LFA), or receive slips (ISR3.RSP/N). 1_B , Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set. Significant only if the serial signaling access is enabled.

Clock Mode Register 4

CMR4_T	Offset	Reset Value
Clock Mode Register 4	$xx41_H$	00_H

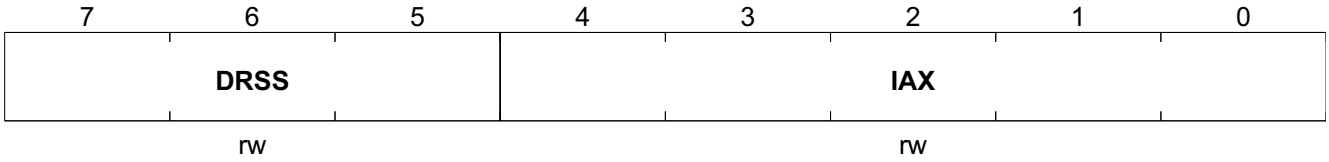
7	6	5	4	3	2	1	0
IAR					RS		
rw					rw		

Field	Bits	Type	Description
IAR	7:3	rw	**Integral parameter selection (Corner frequency and attenuation selection) for the DCO-R** Only valid if CMR6.DCOCOMPN = ´1´and CMR2.ECFAR = ´1´,See Chapter 3.6.5 and Table 15.
RS	2:0	rw	**Receive Clock (RCLK) Frequency Selection** See Chapter 3.6. *Note: Only valid for COMP = ´0´. In QuadFALC® compatibility mode (COMP = ´1´) these bits are ignored (see CMR1.RS). RS_2 to RS_5 are dejittered clocks sourced by DCO-R.* 000_B , clock recovered from the line through the DPLL drives RCLK. 001_B , clock recovered from the line through the DPLL drives RCLK. Ored with the incoming LOS signal. 010_B , 1.544 MHz, dejitered, sourced by DCO-R. 011_B , 3.088 MHz, dejitered, sourced by DCO-R. 100_B , 6.176 MHz, dejitered, sourced by DCO-R. 101_B , 12.352 MHz, dejitered, sourced by DCO-R. 110_B , 1.544 MHz ored with LOS. 111_B , 12.352 MHz ored with LOS.

Clock Mode Register 5

Note: The reset value depends on the channel, so that for the DCO-R the current channel is selected by the bits DRSS (for example for channel 3 the reset value is ´40´$_H$).

CMR5_T	Offset	Reset Value
Clock Mode Register 5	**xx42$_H$**	**00$_H$**



Field	Bits	Type	Description
DRSS	7:5	rw	**DCO-R Channel Selection** See **Chapter 3.6**. *Note: Only valid for COMP = ´0´. In QuadFALC® compatibility mode (COMP = ´1´) these bits are ignored and CMR1.DRSS are used.* 000_B , receive reference clock generated by the DPLL of channel 1. 001_B , receive reference clock generated by the DPLL of channel 2. 010_B , receive reference clock generated by the DPLL of channel 3. 011_B , receive reference clock generated by the DPLL of channel 4. 100_B , receive reference clock generated by the DPLL of channel 5. 101_B , receive reference clock generated by the DPLL of channel 6. 110_B , receive reference clock generated by the DPLL of channel 7. 111_B , receive reference clock generated by the DPLL of channel 8.
IAX	4:0	rw	**Integral parameter selection (Corner frequency and attenuation selection) for the DCO-X** Only valid if CMR6.DCOCOMPN = ´1´and CMR2.ECFAX = ´1´, see **Chapter 3.7.4** and **Table 15**.

Clock Mode Register 6

CMR6_T	Offset	Reset Value
Clock Mode Register 6	$xx43_H$	00_H

7	6	5	4	3	2	1	0
DCOCOMPN	SRESR	SRESX	STF			SCFX	ATCS
rw	rw	rw	rw			rw	rw

Field	Bits	Type	Description
DCOCOMPN	7	rw	**Compatibility programming of DCO-R/DCO-X disable** Only applicable if CMR2.ECFAR/ECFAX is set. See Chapter 3.6.5, Table 15. 0_B , programming of corner frequencies of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0) /CFAX(3:0), compatible to the QuadFALC56® v2.x. Register bits CMR5.IAX(4:0)/CMR4.IAR(4:0) are not valid. 1_B , programming of corner frequencies and attenuation factors of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0)/CFAX(3:0) and CMR4.IAR(4:0)/CMR5.IAX(4:0) in the range 0.2 ... 20 Hz.
SRESR	6	rw	**Soft Reset of DCO-R** By setting this bit a soft reset of the DCO-R will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-R lock functionality, this bit must be cleared subsequently. See Chapter 3.6.5. 0_B , DCO-R enabled (normal lock functionality). 1_B , soft reset of DCO-R, no lock functionality.
SRESX	5	rw	**Soft Reset of DCO-X** By setting this bit a soft reset of the DCO-X will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-X lock functionality, this bit must be cleared subsequently. See Chapter 3.7.4. 0_B , DCO-X enabled (normal lock functionality). 1_B , soft reset of DCO-X, no lock functionality.

Field	Bits	Type	Description
STF	4:2	rw	**Transmit Clock (TCLK) Frequency Selection** See **Chapter 3.7**. *Note: Only valid for COMP = 0. In QuadFALC® compatibility mode (COMP = 1) these bits are ignored and CMR1.STF is used. Note that frequencies are not in ascent ordering .* 000_B , 1.544 MHz. 001_B , 6.176 MHz. 010_B , 3.088 MHz. 011_B , 12.352 MHz. 100_B , 24.704 MHz. 101_B , reserved. 110_B , reserved. 111_B , reserved.
SCFX	1	rw	**Select Corner Frequency of DCO-X** See **Chapter 3.7.4** 0_B , corner frequency of DCO-X is 6Hz. 1_B , corner frequency of DCO-X is 0.6 Hz.
ATCS	0	rw	**Automatic Transmit Clock Switching** If TCLK is lost, SCLKX can be automatically selected to transmit data, see **Chapter 3.7.3**. *Note: Status bits ISR7.XCLKSS(1:0) (**ISR7_T**) show if automatic clock switching was performed. Status bits CLKSTAT.TCLKLOS and CLKSTAT.SCLKXLOS (**CLKSTAT_T**) show the current status of the input clocks TCLK and SCLKX respectively.* 0_B , automatic clock switching is disabled. 1_B , automatic clock switching is enabled.

Clock Mode Register 1

CMR1_T	Offset	Reset Value
Clock Mode Register 1	$xx44_H$	00_H

7	6	5	4	3	2	1	0
DRSS		RS		DCS	STF	DXJA	DXSS
rw		rw		rw	rw	rw	rw

Field	Bits	Type	Description
DRSS	7:6	rw	**Select RCLK Source Channel** These bits select the source channel of RCLK, see also **Chapter 3.6**. *Note: Only valid for COMP = ´1´. For COMP = ´0´) these bits are ignored and CMR5.DRSS are used.* 00_B , Receive reference clock generated by channel 1 01_B , Receive reference clock generated by channel 2. 10_B , Receive reference clock generated by channel 3. 11_B , Receive reference clock generated by channel 4.
RS	5:4	rw	**Select RCLK Source** These bits select the source of RCLK, see also **Chapter 3.6**. *Note: Only valid for COMP = ´1´. For COMP = ´0´) these bits are ignored and CMR4.RS are used.* 00_B , Clock recovered from the line through the DPLL drives RCLK 01_B , Clock recovered from the line through the DPLL drives RCLK and in case of an active LOS alarm RCLK pin is set high (ored with LOS). 10_B , Clock recovered from the line is de-jittered by DCO-R to drive a 1.544 MHz clock on RCLK. 11_B , Clock recovered from the line is de-jittered by DCO-R to drive a 6.176MHz clock on RCLK.
DCS	3	rw	**Disable Clock-Switching** In Slave mode (LIM0.MAS = ´0´) the DCO-R is synchronized on the recovered route clock. In case of loss-of-signal LOS the DCO-R switches automatically to the clock sourced by port SYNC, see also **Table 16**. 0_B , automatic switching from RCLK to SYNC is enabled 1_B , automatic switching from RCLK to SYNC is disabled

Field	Bits	Type	Description
STF	2	rw	**Select TCLK Frequency** Only applicable if the pin function TCLK on multi function port XP(A,B) is selected by PC(3:1).XPC(3:0) = ´0011$_b$´. Data on XL1/2 (XDOP/N / XOID) are clocked with TCLK. See **Chapter 3.7.2**. *Note: Only valid for COMP = ´1´. For COMP = ´0´) these bit is ignored and CMR5.STF are used.* 0_B , 1.544 MHz 1_B , 6.176 MHz
DXJA	1	rw	**Disable Internal Transmit Jitter Attenuation** Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N/XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from SCLKX, independent of this bit.
DXSS	0	rw	**DCO-X Synchronization Clock Source** See **Figure 29**. 0_B , The DCO-X circuitry synchronizes to the internal reference clock which is sourced by SCLKX/R or RCLK. Since there are many reference clock opportunities the following internal prioritizing in descending order from left to right is realized: LIM1.RL > CMR1.DXSS > LIM2.ELT > current working clock of transmit system interface. If one of these bits is set the corresponding reference clock is taken. 1_B , DCO-X synchronizes to an external reference clock provided on pin XPA or XPB pin function TCLK, if no remote loop is active. TCLK is selected by PC(2:1).XPC(3:0) = ´0011B´.

Clock Mode Register 2

CMR2_T	Offset	Reset Value
Clock Mode Register 2	$xx45_H$	00_H

7	6	5	4	3	2	1	0
ECFAX	ECFAR	DCOXC	DCF	IRSP	IRSC	IXSP	IXSC
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ECFAX	7	rw	**Enable Corner Frequency Adjustment for DCO-X** See **Chapter 3.7.4** and **Table 15**. *Note: DCO-X must be activated.* 0_B , adjustment is disabled (only 2Hz and 0.2Hz are possible). 1_B , adjustment is enabled as programmed in CMR3.CFAX(3:0) and CMR4.IAX(4:0)
ECFAR	6	rw	**Enable Corner Frequency Adjustment for DCO-R** See **Chapter 3.6.5** and **Table 15**. *Note: DCO-R must be activated.* 0_B , adjustment is disabled (only 2Hz and 0.2Hz are possible). 1_B , adjustment is enabled as programmed in CMR3.CFAR(3:0) and CMR5.IAR(4:0).
DCOXC	5	rw	**DCO-X Center-Frequency Enable** 0_B , The center function of the DCO-X circuitry is disabled. 1_B , The center function of the DCO-X circuitry is enabled. DCO-X centers to 1.544 MHz related to the master clock reference (MCLK), if reference clock (e.g. SCLKX) is missing.
DCF	4	rw	**DCO-R Center- Frequency Disabled** See **Table 16**. 0_B , The DCO-R circuitry is frequency centered in master mode if no 1.544 or 2.048 MHz reference clock on pin SYNC is provided or in slave mode if a loss-of-signal occurs in combination with no 1.544 or 2.048 MHz clock on pin SYNC or a gapped clock is provided on pin RCLKI and this clock is inactive or stopped. 1_B , The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available on pin SYNC or pin RCLKI. The DCO-R circuitry starts synchronization as soon as a clock on pins SYNC or RCLKI appears.

Field	Bits	Type	Description
IRSP	3	rw	**Internal Receive System Frame Sync Pulse** 0_B , The frame sync pulse for the receive system interface is sourced by $\overline{SYPR}$ (if $\overline{SYPR}$ is applied). If $\overline{SYPR}$ is not applied, the frame sync pulse is derived from RDO output signal internally free running). *Note: The use of IRSP = ´0´ is recommended.* 1_B , The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry. This internally generated frame sync signal can be output (active low) on multifunction ports RP(A to C) (RPC(3:0) = ´0001_B´). *Note: This is the only exception where the use of RFM and $\overline{SYPR}$ is allowed at the same time. Because only one set of offset registers (RC1/0) is available, programming is done by using the $\overline{SYPR}$ calculation formula in the same way as for the external $\overline{SYPR}$ pulse. Bit IRSC must be set for correct operation.*
IRSC	2	rw	**Internal Receive System Clock** See also **Figure 71**. 0_B , The working clock for the receive system interface is sourced by SCLKR of or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK. 1_B , The working clock for the receive system interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock. SCLKR is ignored.
IXSP	1	rw	**Internal Transmit System Frame Sync Pulse** 0_B , The frame sync pulse for the transmit system interface is sourced by $\overline{SYPX}$. 1_B , The frame sync pulse for the transmit system interface is internally sourced by the DCO-R circuitry. Additionally, the external XMFS signal defines the transmit multiframe begin. XMFS is enabled or disabled by the multifunction port configuration. For correct operation bits CMR2.IXSC/IRSC must be set. $\overline{SYPX}$ is ignored.
IXSC	0	rw	**Internal Transmit System Clock** See also **Figure 71**. 0_B , The working clock for the transmit system interface is sourced by SCLKX. 1_B , The working clock for the transmit system interface is sourced internally by the working clock of the receive system interface. SCLKX is ignored.

Global Configuration Register

GCR_T	Offset	Reset Value
Global Configuration Register	0046_H	00_H

7	6	5	4	3	2	1	0
VIS	**SCI**	**SES**	**ECMC**	Res			**PD**
rw	rw	rw	rw				rw

Field	Bits	Type	Description
VIS	7	rw	**Masked Interrupts Visible** See **Chapter 3.4.4**. 0_B , Masked interrupt status bits are not visible in registers ISR(7:0). 1_B , Masked interrupt status bits are visible in ISR(7:0), but they are not visible in registers GIS.
SCI	6	rw	**Status Change Interrupt** 0_B , Interrupts are generated either on activation or deactivation of the internal interrupt source. 1_B , The following interrupts are activated both on activation and deactivation of the internal interrupt source: ISR2.LOS, ISR2.AIS and ISR0.PDEN
SES	5	rw	**Select External Second Timer** 0_B , Internal second timer selected 1_B , External second timer selected
ECMC	4	rw	**Error Counter Mode COFA** 0_B , Not defined; reserved for future applications. 1_B , A Change of Frame or Multiframe Alignment COFA is detected since the last resynchronization. The events are accumulated in the COFA event counter COEC.(1:0). Multiframe periods received in the asynchronous state are accumulated in the COFA event counter COEC.(7:2). An overflow of each counter is disabled.
PD	0	rw	**Power Down** Switches between power-up and power-down mode. After switching from power down to power up a receiver reset should be made by setting of CMDR.RRES. 0_B , Power up 1_B , Power down: All outputs are driven inactive, except the multifunction ports, which are weakly driven high by the internal pullup devices.

Errored Second Mask

This register functions as an additional mask register for the interrupt status bit Errored Second (ISR3.ES). A "1" in a bit position of ESM deactivates the related second interrupt.

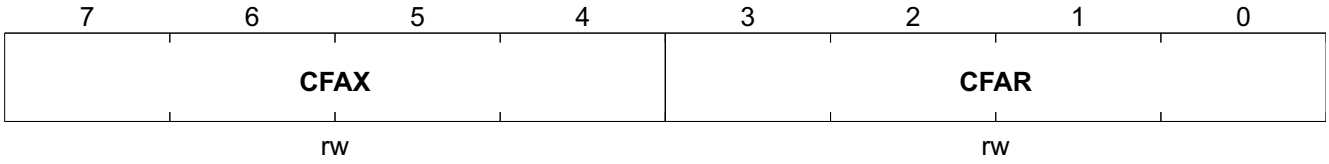
ESM_T	Offset	Reset Value
Errored Second Mask	$xx47_H$	FF_H

7	6	5	4	3	2	1	0
LFA	**FER**	**CER**	**AIS**	**LOS**	**CVE**	**SLIP**	Res
rw	rw	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
LFA	7	rw	**Errored Second Mask Bits**
FER	6		
CER	5		
AIS	4		
LOS	3		
CVE	2		
SLIP	1		

Clock Mode Register 3

CMR3_T	Offset	Reset Value
Clock Mode Register 3	$xx48_H$	00_H



Field	Bits	Type	Description
CFAX	7:4	rw	**Corner Frequency Adjustment for DCO-X** See **Chapter 3.7.4** and **Table 15**. *Note: DCO-X must be activated and CMR2.ECFAX must be set (adjustment must be enabled).*
CFAR	3:0	rw	**Corner Frequency Adjustment for DCO-R** See **Chapter 3.7.4** and **Table 15**. *Note: DCO-R must be activated and CMR2.ECFAR must be set (adjustment must be enabled).*

Disable Error Counter

See **Chapter 5.5.3**.

Note: Error counters and receive buffer delay can be read 1 µs after setting the according bit in bit DEC.

DEC_T	Offset	Reset Value
Disable Error Counter	**xx60$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
DRBD	**FECC**	**DCOEC**	**DBEC**	**DCEC**	**DEBC**	**DCVC**	**DFEC**
w	rw	w	w	w	w	w	w

Field	Bits	Type	Description
DRBD	7	w	**Disable Receive Buffer Delay** This bit has to be set before reading the register RBD. It is automatically reset if RBD has been read.
FECC	6	rw	**Frame Error Count Control** See **Chapter 5.5.3.1** 0_B , FEC count up will be done also if a severely error occurs as described in ANSI-T1-403 1995. 1_B , FEC count up is not done if a simultaneous severely error occurs as described in ANSI-T1-403 1999.
DCOEC	5	w	**Disable COFA Event Counter** 0_B , COFA event counter enabled. 1_B , COFA event counter disabled.
DBEC	4	w	**Disable PRBS Bit Error Counter** Only valid if LCR1.EPRM = ´1´ and FMR1.ECM are reset. 0_B , PRBS bit error counter enabled. 1_B , PRBS bit error counter disabled.
DCEC	3	w	**Disable CRC Error Counter** 0_B , CRC error counter enabled. 1_B , CRC error counter disabled.
DEBC	2	w	**Disable Errored Block Counter** 0_B , errored block counter enabled. 1_B , errored block counter disabled.
DCVC	1	w	**Disable Code Violation Counter** 0_B , Code violation counter enabled. 1_B , Code violation counter disabled.
DFEC	0	w	**Disable Framing Error Counter** These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They are reset automatically if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Transmit Signaling Register 1

The transmit signaling register access is enabled by setting bit FMR5.EIBR = ´1´. Each register contains the bit robbing information for 8 DS0 channels. With the transmit CAS empty interrupt ISR1.CASE the contents of these registers is copied into a shadow register. The contents is subsequently sent out in the corresponding bit positions of the next outgoing multiframe. XS1.7 is sent out first in channel 1 frame 1 and XS12.0 is sent out last. The transmit CAS empty interrupt ISR1.CASE requests that these registers should be serviced within the next 3 ms. If requests for new information are ignored, current contents is repeated. See also **Chapter 5.3.3**.

Note: If access to XS(12:1) registers is done without control of the interrupt ISR1.CASE and the write access to these registers is done exact in that moment when this interrupt is generated, data is lost.A software reset (CMDR.XRES) resets these registers.

XS1_T	Offset	Reset Value
Transmit Signaling Register 1	$xx70_H$	00_H

7	6	5	4	3	2	1	0
A1	B1	C1_A2	D1_B2	A2_A3	B2_B3	C2_A4	D2_B4
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
A1	7	w	**Transmit Signaling Bits**
B1	6		
C1_A2	5		
D1_B2	4		
A2_A3	3		
B2_B3	2		
C2_A4	1		
D2_B4	0		

Similar Registers

Registers XS2 and XS12 have the same description.

The Offset Addresses are listed in **XSn Overview**, for layout and bit names refer to **Transmit Signaling Registers (T1/J1)**

Table 126 XSn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
XS2	Transmit Signaling Register 2	71_H	
XS3	Transmit Signaling Register 3	72_H	
XS4	Transmit Signaling Register 4	73_H	
XS5	Transmit Signaling Register 5	74_H	
XS6	Transmit Signaling Register 6	75_H	
XS7	Transmit Signaling Register 7	76_H	
XS8	Transmit Signaling Register 8	77_H	
XS9	Transmit Signaling Register 9	78_H	

Table 126 XSn Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
XS10	Transmit Signaling Register 10	79_H	
XS11	Transmit Signaling Register 11	$7A_H$	
XS12	Transmit Signaling Register 12	$7B_H$	

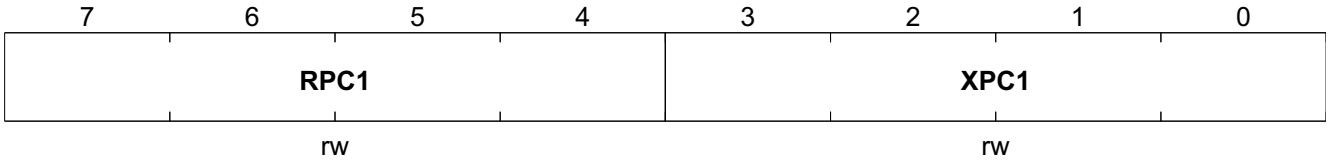
Table 127 Transmit Signaling Registers (T1/J1)

	7							0
XS1	A1	B1	C1_A2	D1_B2	A2_A3	B2_B3	C2_A4	D2_B4
XS2	A3_A5	B3_B5	C3_A6	D3_B6	A4_A7	B4_B7	C4_A8	D4_B8
XS3	A5_A9	B5_B9	C5_A10	D5_B10	A6_A11	B6_B11	C6_A12	D6_B12
XS4	A7_A13	B7_B13	C7_A14	D7_B14	A8_A15	B8_B15	C8_A16	D8_B16
XS5	A9_A17	B9_B17	C9_A18	D9_B18	A10_A19	B10_B19	C10_A20	D10_B20
XS6	A11_A21	B11_B21	C11_A22	D11_B22	A12_A23	B12_B23	C12_A24	D12_B24
XS7	A13_A1	B13_B1	C13_A2	D13_B2	A14_A3	B14_B3	C14_A4	D14_B4
XS8	A15_A5	B15_B5	C15_A6	D15_B6	A16_A7	B16_B7	C16_A8	D16_B8
XS9	A17_A9	B17_B9	C17_A10	D17_B10	A18_A11	B18_B11	C18_A12	D18_B12
XS10	A19_A13	B19_B13	C19_A14	D19_B14	A20_A15	B20_B15	C20_A16	D20_B16
XS11	A21_A17	B21_B17	C21_A18	D21_B18	A22_A19	B22_B19	C22_A20	D22_B20
XS12	A23_A21	B23_B21	C23_A22	D23_B22	A24_A23	B24_B23	C24_A24	D24_B24

Port Configuration 1

See **Chapter 3.8**. The unvailable multi function ports must be configured to an allowed value. It is suggested to configure them to an uncritical output signal, for example PC3 = ´x5$_H$´, PC4 = ´35$_H$´.

PC1_T	Offset	Reset Value
Port Configuration 1	xx80$_H$	00$_H$



Field	Bits	Type	Description
RPC1	7:4	rw	**Receive multifunction port configuration** The multifunction ports RP(A to C) are bidirectional. After Reset the ports RPA and RPB are configured as SYPR., the port RPC is configured as RCLK output. With the selection of the pin function the In/Output configuration is also achieved. The input function $\overline{\text{SYPR}}$ may only be selected once, it must not be selected twice or more. Register PC1 configures port RPA, while PC2 configures port RPB and PC3 port RPC. See **RPC1 Constant Values**
XPC1	3:0	rw	**Transmit multifunction Port Configuration** The multifunction ports XP(A to B) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the four different input functions ($\overline{\text{SYPX}}$, XMFS, XSIG, TCLK, XLT and $\overline{\text{XLT}}$) may only be selected once. No input function must be selected twice or more. $\overline{\text{SYPX}}$ and XMFS should not be selected in parallel. Register PC1 configures port XPA and PC2 the port XPB. See XPC1 Constant Values.

Table 128 RPC1 Constant Values

Name and Description	Value
SYPR Synchronous Pulse Receive (Input, low active) Together with register RC(1:0) $\overline{\text{SYPR}}$ defines the frame begin on the receive system interface. Because of the offset programming the $\overline{\text{SYPR}}$ and the RFM pin function cannot be selected in parallel.	0000$_B$
RFM: Receive Frame Marker (Output) CMR2.IRSP = 0: The receive frame marker is active high for one 2.048 MHz period during any bit position of the current frame. Programming of the bit position is done by using registers RC(1:0). The internal time slot assigner is disabled. The RFM offset calculation formula has to be used. CMR2.IRSP = 1: Internally generated frame synchronization pulse sourced by the DCO-R circuitry. The pulse is active low for one 2.048 MHz period.	0001$_B$

Table 128 RPC1 Constant Values (cont'd)

Name and Description	Value
RMFB: Receive Multiframe Begin (Output) Marks the beginning of every received multiframe or optionally the begin of every CAS multiframe begin (active high).	0010_B
RSIGM: Receive Signaling Marker (Output) Marks the time slots which are defined by register RTR(4:1) of every frame on port RDO.	0011_B
RSIG: Receive Signaling Data (Output) The received CAS multiframe is transmitted on this pin. Time slot on RSIG correlates directly to the time slot assignment on RDO.	0100_B
DLR: Data Link Bit Receive (Output) Marks the Sa-bits within the data stream on RDO.	0101_B
FREEZE: Freeze Signaling (Output) The freeze signaling status is active high by detecting a loss-of-signal alarm, or a loss of CAS frame alignment or a receive slip (positive or negative). It stays high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.	0110_B
RFSP: Receive Frame Synchronous Pulse (Output, low active) Marks the frame begin in the receivers synchronous state. This marker is active low for 488 ns with a frequency of 8 kHz.	0111_B
RLT: Receive line termination (input) "Hardware" switching of receive line termination, see **Chapter 3.6.6**.	1000_B
GPI: general purpose input Value of this input is stored in register MFPI.	1001_B
GPOH: General purpose output, high level Pin is set fixed to high level	1010_B
GPOL: General purpose output, low level Pin is set fixed to low level	1011_B
LOS: Loss of signal (output) Loss of signal indication output	1100_B
RTDMT: Receive TDM tristate (input) receive TDM i/f tristate (RDO, RSIG, SCLKR, RFM), see **Chapter 3.6.7**.	1101_B
reserved	1110_B
RCLK: RCLK output	1111_B

Table 129 XPC1 Constant Values

Name and Description	Value
SYPX: Synchronous Pulse Transmit (Input, low active) Together with register XC(1:0) $\overline{\text{SYPX}}$ defines the frame begin on the transmit system interface ports XDI and XSIG.	0000_B
XMFS: Transmit Multiframe Synchronization (Input) Together with register XC(1:0) XMFS defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low.	0001_B
XSIG: Transmit Signaling Data (Input) Input for transmit signaling data received from the signaling highway. Optionally sampling of XSIG data is controlled by the active high XSIGM marker.	0010_B

Table 129 XPC1 Constant Values (cont'd)

Name and Description	Value
TCLK: Transmit Clock (Input) A 1.544/6.176 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) is not used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 1.544 MHz.	0011_B
XMFB: Transmit Multiframe Begin (Output) Marks the beginning of every transmit multiframe.	0100_B
XSIGM: Transmit Signaling Marker (Output) Marks the time slots which are defined by register TTR(4:1) of every frame on port XDI.	0101_B
DLX: Data Link Bit Transmit (Output) Marks the Sa-bits within the data stream on XDI.	0110_B
XCLK: Transmit Line Clock (Output) Frequency: 1.544 MHz	0111_B
XLT: Transmit Line Tristate control input, high active With a high level on this port the transmit lines XL1/2 or XDOP/N are set directly into tristate. This pin function is logically ored with register XPM2.XLT, see **Chapter 3.6.7**.	1000_B
GPI: General Purpose Input, low level Value of this input is stored in register MFPI.	1001_B
GPOH: General Purpose Output, high level Pin is set fixed to high level	1010_B
GPOL: General Purpose Output, low level Pin is set fixed to low level	1011_B
reserved	1100_B
reserved	1101_B
XLT: Transmit Line Tristate control input, low active see XLT	1110_B
reserved	1111_B

Registers PC2 to PC3 have the same layout and description, but the 4 LSBs of PC3 are not used because only 2 MFPs in transmit direction exists.

The register PC4 and the bits (3:0) of the register PC3 can be written and read, but are not valid (dummy register bits for software compatibility to the QuadFALC).

Only one of the ports RPA, RPB or RPC must be configured as RTDMT.

Only one of the ports XPA or XPB must be configured as XLT or $\overline{\text{XLT}}$.

The registers PC1, PC2 and PC4 have the reset values ´00_H´, PC3 has the reset value ´$F0_H$´.

The Offset Addresses are listed in **PCn Overview**, for bit names refer to **Port Configuration Registers**.

Table 130 PCn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
PC2	Port Configuration Register 2	81_H	
PC3	Port Configuration Register 3	82_H	
PC4	Port Configuration Register 4	83_H	

Table 131 Port Configuration Registers

	7	6	5	4	3	2	1	0
PC1	RPC13	RPC12	RPC11	RPC10	XPC13	XPC12	XPC11	XPC10
PC2	RPC23	RPC22	RPC21	RPC20	XPC23	XPC22	XPC21	XPC20
PC3	RPC33	RPC32	RPC31	RPC30	XPC33	XPC32	XPC31	XPC30
PC4		RPC42	RPC41	RPC40	XPC43	XPC42	XPC41	XPC40

Port Configuration 5

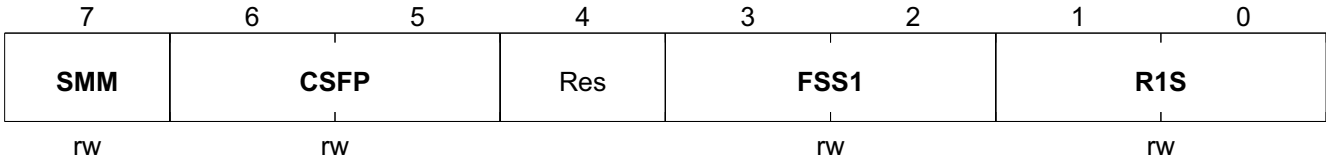
PC5_T	Offset	Reset Value
Port Configuration 5	$xx84_H$	00_H

7	6	5	4	3	2	1	0
PHDSX	**PHDSR**	Res		**CXMFS**	**0**	**CSRP**	**CRP**
rw	rw			rw	rw	rw	rw

Field	Bits	Type	Description
PHDSX	7	rw	**Phase Decoder Switch for DCO-X** See **Chapter 3.7.4** and formulas in **GCM6_T**. 0_B , switch phase decoder by 1/3 1_B , switch phase decoder by 1/6
PHDSR	6	rw	**Phase Decoder Switch for DCO-R** See **Chapter 3.7.4** and formulas in **GCM6_T**. 0_B , switch phase decoder by 1/3 1_B , switch phase decoder by 1/6
CXMFS	3	rw	**Configure XMFS Port** 0_B , Port XMFS is active low. 1_B , Port XMFS is active high.
0	2	rw	**Reserved** Must be cleared.
CSRP	1	rw	**Configure SCLKR Port** 0_B , SCLKR: Input 1_B , SCLKR: Output
CRP	0	rw	**Configure RCLK Port** 0_B , RCLK: Input 1_B , RCLK: Output

Global Port Configuration 1

GPC1_T	Offset	Reset Value
Global Port Configuration 1	0085_H	00_H



Field	Bits	Type	Description
SMM	7	rw	**System Interface Multiplex Mode** Setting of these bit enables 4:1 or 8:1 multiplexing of E1 frames into one or two data streams, dependent on GPC6.SSI16. See **Chapter 5.6.1**. 0_B , System multiplex mode disabled 1_B , System multiplex mode enabled
CSFP	6:5	rw	**Configure SEC/FSC Port** The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = ´1´ or CMR1.RS(1:0) = ´10_b´ or ´11_b´), see **Chapter 5.5.5**. 00_B , SEC: Input, active high 01_B , SEC: Output, active high 10_B , FSC: Output, active high 11_B , FSC: Output, active low
FSS1	3:2	rw	**SEC/FSC Source** One of four internally generated dejittered 8 kHz clocks FSC or second timers SEC (switching between FSC and SEC depends on GPC1.CSFP) are output on pin SEC/FSC. Switching between FSC and SEC is done by GPC1.CSFP, see **Chapter 5.5.5**. *Note: Only valid for COMP = ´1´. For COMP = ´0´ these bits are ignored and GPC2.FSS are used.* 00_B , FSC or SEC respectively, sourced by channel 1 01_B , FSC or SEC respectively, sourced by channel 2 10_B , FSC or SEC respectively, sourced by channel 3 11_B , FSC or SEC respectively, sourced by channel 4
R1S	1:0	rw	**RCLK1 Source** One of the four internally generated receive route clocks is output on pin RCLK1. Ouputs RCLK(4:2) are valid independent of these bits, see **Chapter 3.6**. *Note: Only valid for COMP = ´1´. For COMP = ´0´ these bits are ignored and GPC2.R1S are used.* 00_B , RCLK1 sourced by channel 1 01_B , RCLK1 sourced by channel 2 10_B , RCLK1 sourced by channel 3 11_B , RCLK1 sourced by channel 4

Port Configuration 6

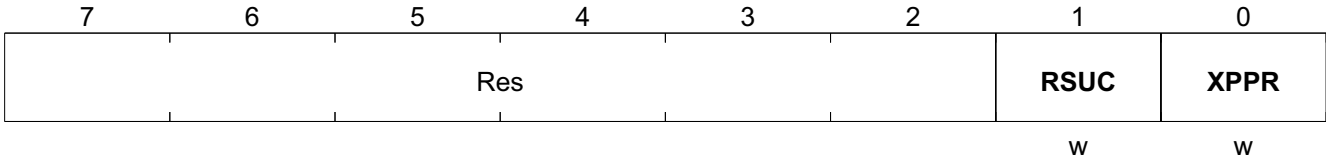
PC6_T	Offset	Reset Value
Port Configuration 6	$xx86_H$	00_H

7	6	5	4	3	2	1	0
Res	**TSRE**	Res					
	rw						

Field	Bits	Type	Description
TSRE	6	rw	**Transmit serial resistor enable** See **Chapter 3.7.1**. 0_B , Internal serial resistors are disabled. 1_B , Internal serial resistors are enabled.

Command Register 2

CMDR2_T	Offset	Reset Value
Command Register 2	$xx87_H$	00_H



Field	Bits	Type	Description
RSUC	1	w	**Reset Signaling Unit Counter - HDLC Channel 1** See **Chapter 5.3.2**. *Note: The maximum time between writing to the CMDR2 register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the external micro controller operates with a very high clock rate in comparison with the OctalFALCTM's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.* 0_B , no reset of the SS7 signaling unit counter and error counter is done (no action is done) 1_B , After setting this bit the SS7 signaling unit counter and error counter are reset.The bit is cleared automatically after execution
XPPR	0	w	**Transmit Periodical Performance Report (PPR)** See **Chapter 5.3.7**. 0_B , no sending of PPR 1_B , After setting this bit the last PPR is sent once. The bit is cleared automatically after completion. Applies to HDLC channel 1 only

Command Register 3

See **Chapter 5.3**.

CMDR3_T	Offset	Reset Value
Command Register 3	**xx88$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
RMC2	Res	**XREP2**	Res	**XHF2**	**XTF2**	**XME2**	**SRES2**
w		w		w	w	w	w

Field	Bits	Type	Description
RMC2	7	w	**Receive Message Complete - HDLC Channel 2** Confirmation from external micro controller to OctalFALCTM that the current frame or data block has been fetched following an RPF2 or RME2 interrupt, thus the occupied space in the RFIFO2 can be released.
XREP2	5	w	**Transmission Repeat - HDLC Channel 2** If XREP2 is set together with XTF2 (write ´24$_H$´ to CMDR3), the OctalFALCTM repeatedly transmits the contents of the XFIFO2 (1 up to 64bytes) without HDLC framing fully transparently, i.e. without flag, CRC.The cyclic transmission is stopped with an SRES2 command or by resetting XREP2.
XHF2	3	w	**Transmit HDLC Frame - HDLC Channel 2** After having written up to 64 bytes to the XFIFO2, this command initiates the transmission of a HDLC frame.
XTF2	2	w	**Transmit Transparent Frame - HDLC Channel 2** Initiates the transmission of a transparent frame without HDLC framing.
XME2	1	w	**Transmit Message End - HDLC Channel 2** Indicates that the data block written last to the XFIFO2 completes the current frame. The OctalFALCTM can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.
SRES2	0	w	**Signaling Transmitter Reset - HDLC Channel 2** The transmitter of the signaling controller is reset. XFIFO2 is cleared of any data and an abort sequence (seven 1s) followed by interframe time fill is transmitted. In response to SRES2 an XPR2 interrupt is generated. This command can be used by the external micro controller to abort a frame currently in transmission.

Command Register 4

See **Chapter 5.3**.

CMDR4_T	Offset	Reset Value
Command Register 4	**xx89$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
RMC3	Res	**XREP3**	Res	**XHF3**	**XTF3**	**XME3**	**SRES3**
w		w		w	w	w	w

Field	Bits	Type	Description
RMC3	7	w	**Receive Message Complete - HDLC Channel 3** Confirmation from external micro controller to OctalFALCTM that the current frame or data block has been fetched following an RPF3 or RME3 interrupt, thus the occupied space in the RFIFO3 can be released.
XREP3	5	w	**Transmission Repeat - HDLC Channel 3** If XREP3 is set together with XTF3 (write ´24$_H$´ to CMDR4), the OctalFALCTM repeatedly transmits the contents of the XFIFO3 (1 up to 64 bytes) without HDLC framing fully transparently, i.e. without flag, CRC.The cyclic transmission is stopped with an SRES3 command or by resetting XREP3.
XHF3	3	w	**Transmit HDLC Frame - HDLC Channel 3** After having written up to 64 bytes to the XFIFO3, this command initiates the transmission of a HDLC frame.
XTF3	2	w	**Transmit Transparent Frame - HDLC Channel 3** Initiates the transmission of a transparent frame without HDLC framing.
XME3	1	w	**Transmit Message End - HDLC Channel 3** Indicates that the data block written last to the XFIFO3 completes the current frame. The OctalFALCTM can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.
SRES3	0	w	**Signaling Transmitter Reset - HDLC Channel 3** The transmitter of the signaling controller is reset. XFIFO3 is cleared of any data and an abort sequence (seven ´1´s) followed by interframe time fill is transmitted. In response to SRES3 an XPR3 interrupt is generated.This command can be used by the external micro controller to abort a frame currently in transmission.

Global Port Configuration Register 2

GPC2_T	Offset	Reset Value
Global Port Configuration Register 2	$008A_H$	00_H

7	6	5	4	3	2	1	0
Res	FSS			Res	R1S		
	rw				rw		

Field	Bits	Type	Description
FSS	6:4	rw	**SEC/FSC Source Selection** See **Chapter 4.5.5**. *Note: Only valid for COMP = ´0´. For COMP = ´1´ these bits are ignored and GPC1.FSS are used.* 000_B , SEC/FSC sourced by channel 1. 001_B , SEC/FSC sourced by channel 2. 010_B , SEC/FSC sourced by channel 3. 011_B , SEC/FSC sourced by channel 4. 100_B , SEC/FSC sourced by channel 5. 101_B , SEC/FSC sourced by channel 6. 110_B , SEC/FSC sourced by channel 7. 111_B , SEC/FSC sourced by channel 8.
R1S	2:0	rw	**RCLK1 Source Selection** See **Chapter 3.6**. *Note: Only valid for COMP = ´0´. For COMP = ´1´ these bits are ignored and GPC1.R1S are used.* 000_B , RCLK1 sourced by channel 1. 001_B , RCLK1 sourced by channel 2. 010_B , RCLK1 sourced by channel 3. 011_B , RCLK1 sourced by channel 4. 100_B , RCLK1 sourced by channel 5. 101_B , RCLK1 sourced by channel 6. 110_B , RCLK1 sourced by channel 7. 111_B , RCLK1 sourced by channel 8.

Common Configuration Register 3

CCR3_T	Offset	Reset Value
Common Configuration Register 3	$xx8B_H$	00_H

7	6	5	4	3	2	1	0
RFT22	RADD2	RCRC2	XCRC2	ITF2	XMFA2	RFT12	RFT02
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RFT22	7	rw	**RFIFO2 Threshold Level - HDLC Channel 2** Highest bit to set the RFIFO2 size. See RFT12, RFT02.
RADD2	6	rw	**Receive Address Pushed to RFIFO2** If this bit is set, the received HDLC channel 2 address information (1 or 2 bytes, depending on the address mode selected via MODE2.MDS02) is pushed to RFIFO2. This function is applicable in non-auto mode and transparent mode 1.
RCRC2	5	rw	**Receive CRC ON/OFF - HDLC Channel 2** Only applicable in non-auto mode.If this bit is set, the received CRC checksum is written to RFIFO2 (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO2 by the status information byte (contents of register RSIS2). The received CRC checksum will additionally be checked for correctness. If non-auto mode is selected, the limits for “valid frame” check are modified.
XCRC2	4	rw	**Transmit CRC ON/OFF - HDLC Channel 2** If this bit is set, the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO2). The transmitted frame is closed automatically with a closing flag.
ITF2	3	rw	**Interframe Time Fill - HDLC Channel 2** Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller. 0_B , Continuous logical "1" is output 1_B , Continuous flag sequences are output ("01111110" bit patterns)
XMFA2	2	rw	**Transmit Multiframe Aligned - HDLC Channel 2** Determines the synchronization between the framer and the corresponding signaling controller. 0_B , The contents of the XFIFO2 is transmitted without multiframe alignment. 1_B , The contents of the XFIFO2 is transmitted multiframe aligned.

Field	Bits	Type	Description
RFT12	1	rw	**RFIFO2 Threshold Level - HDLC Channel 2** The size of the accessible part of RFIFO2 can be determined by programming these bits together with the bit RFT22. The number of valid bytes after an RPF interrupt is given in the following overview. The value of RFT(2:0)2 can be changed dynamically if reception is not running or after the current data block has been read, but before the command CMDR3.RMC2 is issued (interrupt controlled data transfer). See **Chapter 3.4.3**. 000_B , 32 bytes (default value) 001_B , 16 bytes 010_B , 4 bytes 011_B , 2 bytes $1xx_B$, 64 bytes
RFT02	0		

Common Configuration Register 4

CCR4_T	Offset	Reset Value
Common Configuration Register 4	$xx8C_H$	00_H

7	6	5	4	3	2	1	0
RFT23	**RADD3**	**RCRC3**	**XCRC3**	**ITF3**	**XMFA3**	**RFT13**	**RFT03**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RFT23	7	rw	**RFIFO3 Threshold Level - HDLC Channel 3** Highest bit to set the RFIFO3 size. See RFT13, RFT03.
RADD3	6	rw	**Receive Address Pushed to RFIFO3** If this bit is set, the received HDLC channel 3 address information (1 or 2 bytes, depending on the address mode selected via MODE3.MDS03) is pushed to RFIFO3. This function is applicable in non-auto mode and transparent mode 1.
RCRC3	5	rw	**Receive CRC ON/OFF - HDLC Channel 3** Only applicable in non-auto mode.If this bit is set, the received CRC checksum is written to RFIFO3 (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO3 by the status information byte (contents of register RSIS3). The received CRC checksum will additionally be checked for correctness. If non-auto mode is selected, the limits for “Valid Frame” check are modified.
XCRC3	4	rw	**Transmit CRC ON/OFF - HDLC Channel 3** If this bit is set, the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO3). The transmitted frame is closed automatically with a closing flag.
ITF3	3	rw	**Interframe Time Fill - HDLC Channel 3** Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller. 0_B , Continuous logical "1" is output 1_B , Continuous flag sequences are output ("01111110" bit patterns)
XMFA3	2	rw	**Transmit Multiframe Aligned - HDLC Channel 3** Determines the synchronization between the framer and the corresponding signaling controller. 0_B , The contents of the XFIFO3 is transmitted without multiframe alignment. 1_B , The contents of the XFIFO3 is transmitted multiframe aligned.

Field	Bits	Type	Description
RFT13	1	rw	**RFIFO3 Threshold Level - HDLC Channel 3** The size of the accessible part of RFIFO3 can be determined by programming these bits together with the bit RFT23. The number of valid bytes after an RPF interrupt is given in the following overview. The value of RFT(2:0)3 can be changed dynamically if reception is not running or after the current data block has been read, but before the command CMDR3.RMC3 is issued (interrupt controlled data transfer). See **Chapter 3.4.3**. 000_B , 32 bytes (default value) 001_B , 16 bytes 010_B , 4 bytes 011_B , 2 bytes $1xx_B$, 64 bytes
RFT03	0		

Common Configuration Register 5

Note: SUET, CSF and AFX are only valid, if SS7 mode is selected.CR and EPR are only valid, if PPR mode is selected.

CCR5_T	Offset	Reset Value
Common Configuration Register 5	$xx8D_H$	00_H

7	6	5	4	3	2	1	0
FECCC	**CSF2**	**SUET**	**CSF**	**AFX**	Res	**CR**	**EPR**
rw	rw	rw	rw	rw		rw	rw

Field	Bits	Type	Description
FECCC	7	rw	**FEC Count Control** See **Chapter 5.5.3.1**. 0_B , FEC count up will be done also if a severely error occurs as described in ANSI-T1-403 1995. 1_B , FEC count up is not done if a simultaneous severely error occurs as described in ANSI-T1-403 1999.
CSF2	6	rw	**Compare Status Field-Mode 2** 0_B , Compare disabled 1_B , Compare enabled
SUET	5	rw	**Signaling Unit Error Threshold - HDLC Channel 1** Defines the number of signaling units received in error that will cause an error rate high indication (ISR1.SUEX). 0_B , Threshold 64 errored signaling units 1_B , Threshold 32 errored signaling units
CSF	4	rw	**Compare Status Field - HDLC Channel 1** If the status fields of consecutive LSSUs are equal, only the first is stored and every following is ignored. 0_B , Compare disabled. 1_B , Compare enabled.
AFX	3	rw	**Automatic FISU Transmission - HDLC Channel 1** After the contents of the transmit FIFO (XFIFO) has been transmitted completely, FISUs are transmitted automatically. These FISUs contain the FSN and BSO of the last transmitted signaling unit (provided in XFIFO). 0_B , Automatic FISU transmission disabled. 1_B , Automatic FISU transmission enabled.
CR	1	rw	**Command Response - HDLC Channel 1** Reflects the status of the CR bit in the SAPI octet transmitted during Periodical Performance Report (PPR), if CCR5.EPR = ´1´. 0_B , CR bit = ´0´ 1_B , CR bit = ´1´

Field	Bits	Type	Description
EPR	0	rw	**Enable Periodical Performance Report (PPR) - HDLC Channel 1** See **Chapter 5.3.7**. 0_B , PPR disabled. 1_B , PPR enabled.

Mode Register 2

MODE2_T	Offset	Reset Value
Mode Register 2	$xx8E_H$	00_H

7	6	5	4	3	2	1	0
MDS2			Res	HRAC2	DIV2	HDLCI2	TSFL2
rw				rw	rw	rw	rw

Field	Bits	Type	Description
MDS2	7:5	rw	**Mode Select - HDLC Channel 2** The operating mode of the HDLC controller is selected, see **Chapter 5.3**. 000_B , Reserved 001_B , Reserved 010_B , One-byte address comparison mode (RAL1, 2) 011_B , Two-byte address comparison mode (RAH1, 2 and RAL1, 2) 100_B , No address comparison 101_B , One-byte address comparison mode (RAH1, 2) 110_B , Reserved 111_B , No HDLC framing mode 1
HRAC2	3	rw	**Receiver Active - HDLC Channel 2** Switches the HDLC receiver to operational or inoperational state. 0_B , Receiver inactive 1_B , Receiver active
DIV2	2	rw	**Data Inversion - HDLC Channel 2** Setting this bit will invert the internal generated HDLC data stream. 0_B , Normal operation, HDLC data stream not inverted 0_B , HDLC data stream inverted
HDLCI2	1	rw	**Inverse HDLC Operation Selection for HDLC Channel 2** Setting this bit will switch the HDLC controller to the system side, see **Chapter 5.3.1**. 0_B , HDLC protocol is sent and received on line side. 1_B , HDLC protocol is sent and received on system side.
TSFL2	0	rw	**Enable Shared Flags in Transmit Direction for HDLC Channel 2** *Note: In receive direction shared flag is detected automatically.* 0_B , Both, an opening and a closing flag (7EH) are transmitted for each HDLC frame (normal operation). 1_B , The closing flag (7EH) of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one to be transmitted.

Mode Register 3

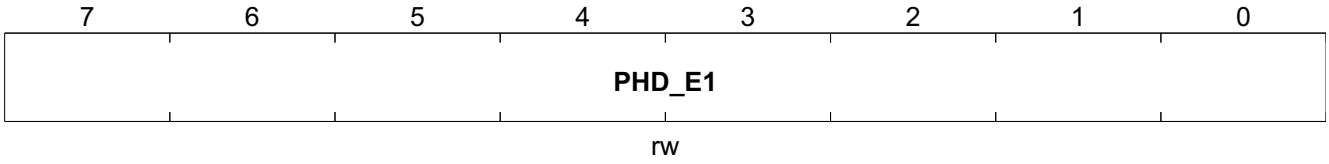
MODE3_T	Offset	Reset Value
Mode Register 3	xx8F$_H$	00$_H$

7	6	5	4	3	2	1	0
MDS3			Res	HRAC3	DIV3	HDLCI3	TSFL3
rw				rw	rw	rw	rw

Field	Bits	Type	Description
MDS3	7:5	rw	**Mode Select - HDLC Channel 3** The operating mode of the HDLC controller is selected, see **Chapter 5.3**. 000_B , Reserved 001_B , Reserved 010_B , One-byte address comparison mode (RAL1, 2) 011_B , Two-byte address comparison mode (RAH1, 2 and RAL1, 2) 100_B , No address comparison 101_B , One-byte address comparison mode (RAH1, 2) 110_B , Reserved 111_B , No HDLC framing mode 1
HRAC3	3	rw	**Receiver Active - HDLC Channel 3** Switches the HDLC receiver to operational or inoperational state. 0_B , Receiver inactive 1_B , Receiver active
DIV3	2	rw	**Data Inversion - HDLC Channel 3** Setting this bit will invert the internal generated HDLC data stream. 0_B , Normal operation, HDLC data stream not inverted 1_B , HDLC data stream inverted
HDLCI3	1	rw	**Inverse HDLC Operation Selection for HDLC Channel 3** Setting this bit will switch the HDLC controller to the system side. 0_B , HDLC protocol is sent and received on line side. 1_B , HDLC protocol is sent and received on system side.
TSFL3	0	rw	**Enable Shared Flags in Transmit Direction for HDLC Channel 3** *Note: In receive direction shared flag is detected automatically.* 0_B , Both, an opening and a closing flag (7EH) are transmitted for each HDLC frame (normal operation). 1_B , The closing flag (7EH) of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one to be transmitted.

Global Clock Mode Register 1

GCM1_T	Offset	Reset Value
Global Clock Mode Register 1	0092_H	00_H



Field	Bits	Type	Description
PHD_E1	7:0	rw	**Frequency Adjust for E1 (lower 8 bits, for highest 4 bits see GCM2)** For details see calculation formulas in register **GCM6_T** and **Table 132**.

Global Clock Mode Register 2

GCM2_T	Offset	Reset Value
Global Clock Mode Register 2	0093_H	10_H

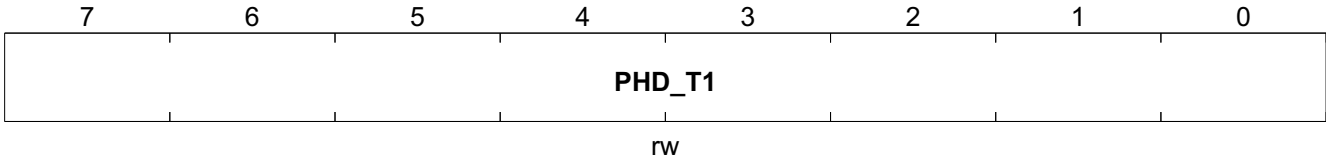
7	6	5	4	3	2	1	0
PHSDEM	PHSDIR	PHSDS	VFREQ_EN	PHD_E111	PHD_E110	PHD_E19	PHD_E18
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PHSDEM	7	rw	**RX Phase Decoder Demand** .... 0_B , default operation 1_B , see formulas in register **GCM6_T**.
PHSDIR	6	rw	**RX Phase Decoder Direction** .... 0_B , default operation 1_B , see formulas in register **GCM6_T**.
PHSDS	5	rw	**RX Phase Decoder Switch** .... 0_B , default operation 1_B , see formulas in register **GCM6_T**.
VFREQ_EN	4	rw	**Variable Frequency Enable** If “fixed mode” mode is selected the clock frequency at the pin MCLK must be 2.048 for E1 or 1.544 MHz for T1/J1 respectively. The setting of the whole clock mode is done automatically and register bits of GCM1, GCM2.PHSDEM, PHDIR, PHSDS, PHD_E1 and GCM3 to GCM8 are unused. If “fixed mode” mode is selected and the SPI- or SCI-interface is used as controller interface, the pinstrapping values at D(15:5) are also not used. *Note: If “fixed mode “ is enabled all of the eight ports must work in the same mode, either in T1 or in E1 mode. A switching between E1 and T1 modes causes a reset of the whole clock system. If “fixed mode“ is disabled a switching between E1 and T1 mode (which can be done in this case individually for every port) does not cause a reset of the whole clock system.* 0_B , Fixed clock frequency of 2.048 (E1) or 1.544 MHz (T1/J1) 1_B , Variable master clock frequency (normal operation, operation after reset)

Field	Bits	Type	Description
PHD_E111	3	rw	**Frequency Adjust for E1 (highest 4 bits, for lower 8 bits see GCM1)** The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6_T** and **Table 132**. 100000000000_B, -2048 .....B, 000000000000_B, 0 .....B, 011111111111_B, +2047
PHD_E110	2	rw	
PHD_E19	1	rw	
PHD_E18	0	rw	

Global Clock Mode Register 3

GCM3_T	Offset	Reset Value
Global Clock Mode Register 3	0094_H	00_H



Field	Bits	Type	Description
PHD_T1	7:0	rw	**Frequency Adjust for T1 (lower 8 bits, for 4 highest bits see GCM4)** For details see calculation formulas in register GCM6_T and Table 132.

Global Clock Mode Register 4

GCM4_T	Offset	Reset Value
Global Clock Mode Register 4	0095_H	00_H

7	6	5	4	3	2	1	0
DVM_T1			Res	PHD_T111	PHD_T110	PHD_T19	PHD_T18
rw				rw	rw	rw	rw

Field	Bits	Type	Description
DVM_T1	7:5	rw	**Divider Mode for T1** This bits can be write and read to be software compatible to QuadFALC®, but has no influence on the clock system.
PHD_T111	3	rw	**Frequency Adjust for T1 (highest 4 bits, for lower 8 bits see GCM3)** The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6_T** and **Table 132**. 100000000000_B, -2048 .....$_B$, 000000000000_B, 0 .....$_B$, 011111111111_B, +2047
PHD_T110	2		
PHD_T19	1		
PHD_T18	0		

Global Clock Mode Register 5

Note: Write operations to GCM5 and GCM6 initiate a PLL reset if the asynchronous interface is selected (IM(1:0) = ´0x´) and if the "flexible master clocking mode" is selected (GCM2.VFREQ_EN = ´1´), see ***Chapter 3.4.6.1****.*

GCM5_T	Offset	Reset Value
Global Clock Mode Register 5	**0096_H**	**00_H**

7	6	5	4	3	2	1	0
MCLK_LOW	Res		**PLL_M**				
rw			rw				

Field	Bits	Type	Description
MCLK_LOW	7	rw	**Master Clock Range Low** This bit can be write and read to be software compatible to QuadFALC®, but has no influence on the clock system.
PLL_M	4:0	rw	**PLL Dividing Factor M** For details see calculation formulas in register **GCM6_T** and **Table 132**. 00001_B, 1 .....B, 11111_B, 31

Global Clock Mode Register 6

Note: Write operations to GCM5 and GCM6 initiate a PLL reset if the asynchronous interface is selected (IM(1:0) = ´0x´) and if the "flexible master clocking mode" is selected (GCM2.VFREQ_EN = ´1´), see ***Chapter 3.4.6.1****.*

GCM6_T	Offset	Reset Value
Global Clock Mode Register 6	**0097_H**	**00_H**

7	6	5	4	3	2	1	0
Res		**PLL_N**					
		rw					

Field	Bits	Type	Description
PLL_N	5:0	rw	**PLL Dividing Factor N** For details see calculation formulas below. 000001_B, 1 .....B, , 111111_B, 63

Flexible Clock Mode Settings

If "flexible master clock mode" is used (VFREQ_EN = ´1´), the according register settings can be calculated as follows (a windows-based program for automatic calculation is available, see **Chapter 13.3**. For some of the standard frequencies see the table below.

1. The master clock MCLK must be in the following frequency range:

1.02 MHz ≤ f_{MCLK} ≤ 20 MHz

2. Generally the PLL of the master clocking unit includes an input divider with a dividing factor PLL_M +1 and a feedback divider with a dividing factor 4 x (PLL_N +1). So it generates a clock f_{PLL} of about

$f_{PLL} = f_{MCLK}$ x 4 x (PLL_N +1) / (PLL_M +1) ,.

3. The selection of PLL_N and PLL_M must be done in the following way:

The PLL frequency f_{PLL} must be in the following range:

200 MHz ≤ f_{PLL} ≤ 300 MHz

The combinations of the values PLL_M and PLL_M must fulfill the equations:

2 MHz ≤ f_{MCLK} / (PLL_M +1) ≤ 6 MHz if PLL_N is in the range 25 to 63.

5 MHz ≤ f_{MCLK} / (PLL_M +1) ≤ 15 MHz if PLL_N is in the range 1 to 24.

4. The selection of PHSN_T1 and PHSX_T1 must be done in such a manner that the frequency for the receiver f_{RX_T1} has nearly the value 16 x f_{DATA_T1} x (1 + 100ppm) = 24.7064 MHz:

$f_{RX\_T1} = f_{PLL}$ / {PHSN_T1 + (PHSX_T1 / 6)} .

GCM2.PHSDEM, GCM2.PHSDIR, GCM2.PHSDS, PC5.PHDSX and PC5.PHDSR must be left to ´0´.

5. To bring the "characteristic T1 frequency" f_{outT1} exact to 16 x f_{DATA_T1} = 24.70400 MHz a correction value PHD_T1 is necessary:

PHD_T1 = round **(**12288 x { [PHSN_T1 + (PHSX_T1 / 6)] - [f_{PLL} /16 x f_{DATA_T1}] }**)** .

Table 132 Clock Mode Register Settings for E1 or T1/J1

fMCLK [MHz]	GCM1	GCM2	GCM3	GCM4	GCM5	GCM6	GCM7	GCM8
1.5440	$F0_H$	19_H	00_H	08_H	00_H	$2B_H$	98_H	DA_H
2.0480	00_H	18_H	$D2_H$	$0A_H$	00_H	21_H	$A8_H$	$9B_H$
8.1920	00_H	18_H	$D2_H$	$0A_H$	03_H	21_H	$A8_H$	$9B_H$
12.3520	$F0_H$	19_H	00_H	08_H	07_H	$2B_H$	98_H	DA_H
16.3840	00_H	18_H	$D2_H$	$0A_H$	07_H	21_H	$A8_H$	$9B_H$

Global Clock Mode Register 7

GCM7_T	Offset	Reset Value
Global Clock Mode Register 7	0098_H	80_H

7	6	5	4	3	2	1	0
1	PHSX_E1			PHSN_E1			
r	rw			rw			

Field	Bits	Type	Description
1	7	r	**Fixed ´1´**
PHSX_E1	6:4	rw	**Frequency Adjustment value E1** For details see calculation formulas in register **GCM6_T** and **Table 132**. 000_B , 0 .....$_B$, 101_B , 5
PHSN_E1	3:0	rw	**Frequency Adjustment value for E1** For details see calculation formulas in register **GCM6_T** and **Table 132**. 0001_B, 1 .....$_B$, 1111_B, 15

Global Clock Mode Register 7

GCM8_T	Offset	Reset Value
Global Clock Mode Register 7	0099_H	80_H

7	6	5	4	3	2	1	0
1	PHSX_T1			PHSN_T1			
r	rw			rw			

Field	Bits	Type	Description
1	7	r	**Fixed ´1´**
PHSX_T1	6:4	rw	**Frequency Adjustment value T1** For details see calculation formulas in register **GCM6_T** and **Table 132**. 000_B , 0 .....B , 101_B , 5
PHSN_T1	3:0	rw	**Frequency Adjustment value for T1** For details see calculation formulas in register **GCM6_T** and **Table 132**. 0001_B, 1 .....B , 1111_B, 15

Transmit FIFO 2 Lower Byte

Writing data to XFIFO of HDLC channel 2 can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first. Up to 64bytes/32 words of transmit data can be written to the XFIFO following a XPR interrupt, see Chapter 3.4.3.

XFIFO2L_T	Offset	Reset Value
Transmit FIFO 2 Lower Byte	$xx9C_H$	xx_H

7	6	5	4	3	2	1	0
XF7	**XF6**	**XF5**	**XF4**	**XF3**	**XF2**	**XF1**	**XF0**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF7	7	w	**Transmit FIFO HDLC Channel 2**
XF6	6	w	
XF5	5	w	
XF4	4	w	
XF3	3	w	
XF2	2	w	
XF1	1	w	
XF0	0	w	

Transmit FIFO 2 Higher Byte

XFIFO2H_T	Offset	Reset Value
Transmit FIFO 2 Higher Byte	$xx9D_H$	00_H

7	6	5	4	3	2	1	0
XF15	**XF14**	**XF13**	**XF12**	**XF11**	**XF10**	**XF9**	**XF8**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF15	7	w	**Transmit FIFO for HDLC Channel 2** The function is equivalent to XFIFO2L.
XF14	6	w	
XF13	5	w	
XF12	4	w	
XF11	3	w	
XF10	2	w	
XF9	1	w	
XF8	0	w	

Transmit FIFO 3 Lower Byte

XFIFO3L_T	Offset	Reset Value
Transmit FIFO 3 Lower Byte	$xx9E_H$	00_H

7	6	5	4	3	2	1	0
XF7	XF6	XF5	XF4	XF3	XF2	XF1	XF0
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF7	7	w	**Transmit FIFO for HDLC Channel 3** The function is equivalent to XFIFO2L.
XF6	6	w	
XF5	5	w	
XF4	4	w	
XF3	3	w	
XF2	2	w	
XF1	1	w	
XF0	0	w	

Transmit FIFO 3 Higher Byte

XFIFO3H_T	Offset	Reset Value
Transmit FIFO 3 Higher Byte	$xx9F_H$	00_H

7	6	5	4	3	2	1	0
XF15	XF14	XF13	XF12	XF11	XF10	XF9	XF8
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
XF15	7	w	**Transmit FIFO for HDLC Channel 3** The function is equivalent to XFIFO2H.
XF14	6	w	
XF13	5	w	
XF12	4	w	
XF11	3	w	
XF10	2	w	
XF9	1	w	
XF8	0	w	

Time Slot Even/Odd Select

HDLC protocol data can be sent in even, odd or both frames of a multiframe. Even frames are frame number 2, 4, and so on, odd frames are frame number 1, 3, and so on. The selection refers to receive and transmit direction as well. Each multiframe starts with an odd frame and ends with an even frame. By default all frames are used for HDLC reception and transmission.

Note: The different HDLC channels have to be configured to use different time slots, bit positions or frames.

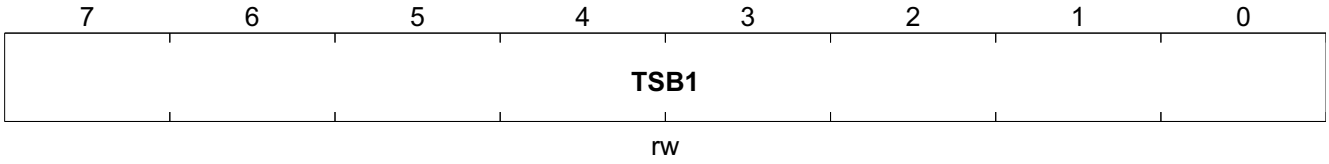
TSEO_T	Offset	Reset Value
Time Slot Even/Odd Select	**xxA0$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res		**EO3**		**EO2**		**EO1**	
		rw		rw		rw	

Field	Bits	Type	Description
EO3	5:4	rw	**Even/Odd frame selection - HDLC Channel 3** Channel 3 HDLC protocol data can be sent in even, odd or both frames of a multiframe. 00_B , Even and odd frames 01_B , Odd frames only 10_B , Even frames only 11_B , Undefined
EO2	3:2	rw	**Even/Odd frame selection - HDLC Channel 2** Channel 2 HDLC protocol data can be sent in even, odd or both frames of a multiframe. 00_B , Even and odd frames 01_B , Odd frames only 10_B , Even frames only 11_B , Undefined
EO1	1:0	rw	**Even/Odd frame selection - HDLC Channel 1** Channel 1 HDLC protocol data can be sent in even, odd or both frames of a multiframe. 00_B , Even and odd frames 01_B , Odd frames only 10_B , Even frames only 11_B , Undefined

Time Slot Bit Select 1

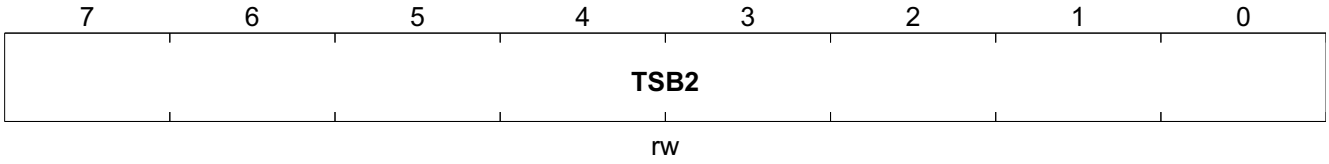
TSBS1_T	Offset	Reset Value
Time Slot Bit Select 1	$xxA1_H$	FF_H



Field	Bits	Type	Description
TSB1	7:0	rw	**Time Slot Bit Selection - HDLC Channel 1** Only bits selected by this register are used for HDLC channel 1 in selected time slots. Time slot selection is done by setting the appropriate bits in registers TTR(4:1) and RTR(4:1) independently for receive and transmit direction. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot(s) are enabled. TSB1x = ´0´ to bit position x in selected time slot(s) is not used for HDLC channel 1 reception and transmission. TSB1x = ´1´ to bit position x in selected time slot(s) is used for HDLC channel 1 reception and transmission.

Time Slot Bit Select 2

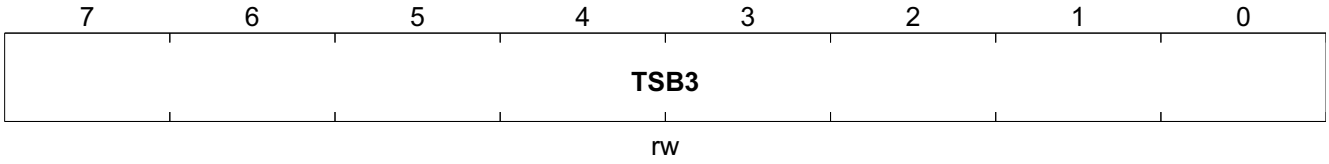
TSBS2_T	Offset	Reset Value
Time Slot Bit Select 2	$xxA2_H$	FF_H



Field	Bits	Type	Description
TSB2	7:0	rw	**Time Slot Bit Selection - HDLC Channel 2** Only bits selected by this register are used for HDLC channel 2 in selected time slots. Time slot selection is done by setting the appropriate bits in register TSS2. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot are enabled. TSB2x=0 to bit position x in selected time slot(s) is not used for HDLC channel 2 reception and transmission. TSB2x=1 to bit position x in selected time slot(s) is used for HDLC channel 2 reception and transmission.

Time Slot Bit Select 3

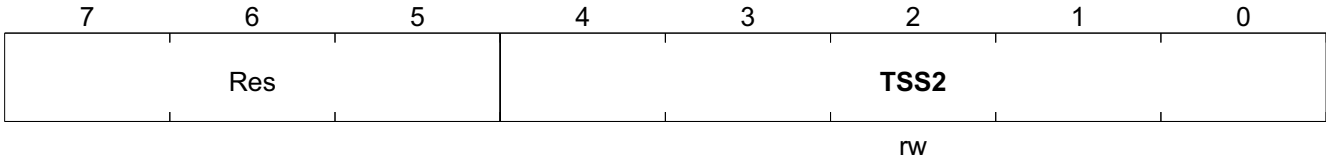
TSBS3_T	Offset	Reset Value
Time Slot Bit Select 3	$xxA3_H$	FF_H



Field	Bits	Type	Description
TSB3	7:0	rw	**Time Slot Bit Selection - HDLC Channel 3** Only bits selected by this register are used for HDLC channel 3 in selected time slots. Time slot selection is done by setting the appropriate bits in register TSS3. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot are enabled. TSB3x=0 to bit position x in selected time slot(s) is not used for HDLC channel 3 reception and transmission. TSB3x=1 to bit position x in selected time slot(s) is used for HDLC channel 3 reception and transmission.

Time Slot Select 2

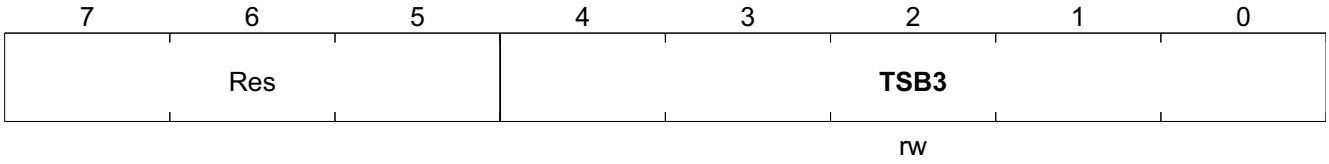
TSS2_T	Offset	Reset Value
Time Slot Select 2	$xxA4_H$	00_H



Field	Bits	Type	Description
TSS2	4:0	rw	**Time Slot Selection Code - HDLC Channel 2** Defines the time slot used by HDLC channel 2. *Note: Different HDLC channels must use different time slots.* 00000_B , No time slot selected 00001_B , Time slot 1 $_B$, ... 11111_B , Time slot 31

Time Slot Select 3

TSS3_T	Offset	Reset Value
Time Slot Select 3	**xxA5$_H$**	**00$_H$**



Field	Bits	Type	Description
TSB3	4:0	rw	**Time Slot Selection Code - HDLC Channel 3** Defines the time slot used by HDLC channel 3. *Note: Different HDLC channels must use different time slots.* 00000_B , No time slot selected 00001_B , Time slot 1 $_B$, ... 11111_B , Time slot 31

Global Interrupt Mask Register

GIMR_T	Offset	Reset Value
Global Interrupt Mask Register	$00A7_H$	00_H

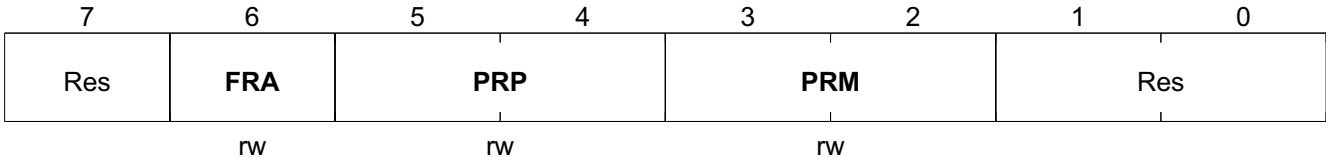
7	6	5	4	3	2	1	0
Res					**PLIL**	Res	**PLLL**
					rw		rw

Field	Bits	Type	Description
PLLL	0	rw	**PLL Locked Interrupt Mask** 0_B , GIS2.PLLLC is enabled. 1_B , GIS2.PLLLC is disabled.

Test Pattern Control Register 0

See **Chapter 5.7.1**.

TPC0_T	Offset	Reset Value
Test Pattern Control Register 0	**xxA8$_H$**	**00$_H$**

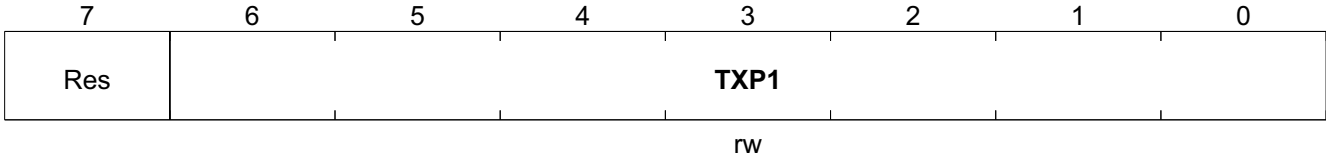


Field	Bits	Type	Description
FRA	6	rw	**Framed/Unframed Selection** 0_B , PRBS is generated/monitored unframed. Framing information is overwritten by the generator. 1_B , PRBS is generated/monitored framed. Time slot 0 is not overwritten by the generator and not observed by the monitor.
PRP	5:4	rw	**PRBS Pattern Selection** See **Chapter 5.7.1**. 00_B , PRBS11 pattern. 01_B , PRBS15 pattern. 10_B , PRBS20 pattern. 11_B , PRBS23 pattern.
PRM	3:2	rw	**PRBS Mode Selection** See **Chapter 5.7.1**. 00_B , PRBS controlled by LCR1 and TPC0.FRA. 01_B , n x 64 kbit/s PRBS. 10_B , reserved. 11_B , n x 56 kbit/s PRBS.

TX Pulse Template Register 1

See Chapter 3.7.5 and Chapter 3.7.5.2. This register contains the transmit amplitude of the 1st 1/16 of the transmit pulse. The contents of this register is ignored unless bit XPM2.XPDIS is set. By default, the values programmed in XPM0 to XPM2 are used to control the transmit pulse template.

TXP1_T	Offset	Reset Value
TX Pulse Template Register 1	$xxC1_H$	38_H



Field	Bits	Type	Description
TXP1	6:0	rw	**Transmit Pulse Amplitude** Two´s Complement number of pulse amplitude, see Table 25

Similar Registers

Registers TXP1to TXP16 have the same description and layout. Every register TXPn defines the amplitude of the part n of 16 of the transmit pulse. An overview is given is the next table.

Note that the reset values of the registers TXP1 to TXP8 are ´38_H´, that of the registers TXP9 to TXP16 are ´00_H´.

Table 133 TXP Overview

Register Short Name	Register Long Name	Offset Address	Page Number
TXP1	TX Pulse Template Register 1	$C1_H$	
TXP2	TX Pulse Template Register 2	$C2_H$	
TXP3	TX Pulse Template Register 3	$C3_H$	
TXP4	TX Pulse Template Register 4	$C4_H$	
TXP5	TX Pulse Template Register 5	$C5_H$	
TXP6	TX Pulse Template Register 6	$C6_H$	
TXP7	TX Pulse Template Register 7	$C7_H$	
TXP8	TX Pulse Template Register 8	$C8_H$	
TXP9	TX Pulse Template Register 9	$C9_H$	
TXP10	TX Pulse Template Register 10	CA_H	
TXP11	TX Pulse Template Register 11	CB_H	
TXP12	TX Pulse Template Register 12	CC_H	
TXP13	TX Pulse Template Register 13	CD_H	
TXP14	TX Pulse Template Register 14	CE_H	
TXP15	TX Pulse Template Register 15	CF_H	
TXP16	TX Pulse Template Register 16	$D0_H$	

Global Port Configuration Register 3

This register is only valid if COMP = ´0´. For COMP = ´1´ selection of source is not possible, always sourced by same channel. See **Chapter 3.6**.

GPC3_T	Offset	Reset Value
Global Port Configuration Register 3	**$00D3_H$**	**21_H**

7	6	5	4	3	2	1	0
Res	**R3S**			Res	**R2S**		
	rw				rw		

Field	Bits	Type	Description
R3S	6:4	rw	**RCLK3 Source Selection** 000_B , RCLK3 sourced by channel 1. 001_B , RCLK3 sourced by channel 2. 010_B , RCLK3 sourced by channel 3. 011_B , RCLK3 sourced by channel 4. 100_B , RCLK3 sourced by channel 5. 101_B , RCLK3 sourced by channel 6. 110_B , RCLK3 sourced by channel 7. 111_B , RCLK3 sourced by channel 8.
R2S	2:0	rw	**RCLK2 Source Selection** 000_B , RCLK2 sourced by channel 1. 001_B , RCLK2 sourced by channel 2. 010_B , RCLK2 sourced by channel 3. 011_B , RCLK2 sourced by channel 4. 100_B , RCLK2 sourced by channel 5. 101_B , RCLK2 sourced by channel 6. 110_B , RCLK2 sourced by channel 7. 111_B , RCLK2 sourced by channel 8.

Global Port Configuration Register 4

This register is only valid if COMP = ´0´. For COMP = ´1´ selection of source is not possible, always sourced by same channel. See **Chapter 3.6**.

GPC4_T	Offset	Reset Value
Global Port Configuration Register 4	**$00D4_H$**	**43_H**

7	6	5	4	3	2	1	0
Res	**R5S**			Res	**R4S**		
	rw				rw		

Field	Bits	Type	Description
R5S	6:4	rw	**RCLK5 Source Selection** 000_B , RCLK5 sourced by channel 1. 001_B , RCLK5 sourced by channel 2. 010_B , RCLK5 sourced by channel 3. 011_B , RCLK5 sourced by channel 4. 100_B , RCLK5 sourced by channel 5. 101_B , RCLK5 sourced by channel 6. 110_B , RCLK5 sourced by channel 7. 111_B , RCLK5 sourced by channel 8.
R4S	2:0	rw	**RCLK4 Source Selection** 000_B , RCLK4 sourced by channel 1. 001_B , RCLK4 sourced by channel 2. 010_B , RCLK4 sourced by channel 3. 011_B , RCLK4 sourced by channel 4. 100_B , RCLK4 sourced by channel 5. 101_B , RCLK4 sourced by channel 6. 110_B , RCLK4 sourced by channel 7. 111_B , RCLK4 sourced by channel 8.

Global Port Configuration Register 5

This register is only valid if COMP = ´0´. For COMP = ´1´ selection of source is not possible, always sourced by same channel. See **Chapter 3.6**.

GPC5_T	Offset	Reset Value
Global Port Configuration Register 5	**$00D5_H$**	**65_H**

7	6	5	4	3	2	1	0
Res	**R7S**			Res	**R6S**		
	rw				rw		

Field	Bits	Type	Description
R7S	6:4	rw	**RCLK7 Source Selection** 000_B , RCLK7 sourced by channel 1. 001_B , RCLK7 sourced by channel 2. 010_B , RCLK7 sourced by channel 3. 011_B , RCLK7 sourced by channel 4. 100_B , RCLK7 sourced by channel 5. 101_B , RCLK7 sourced by channel 6. 110_B , RCLK7 sourced by channel 7. 111_B , RCLK7 sourced by channel 8.
R6S	2:0	rw	**RCLK6 Source Selection** 000_B , RCLK6 sourced by channel 1. 001_B , RCLK6 sourced by channel 2. 010_B , RCLK6 sourced by channel 3. 011_B , RCLK6 sourced by channel 4. 100_B , RCLK6 sourced by channel 5. 101_B , RCLK6 sourced by channel 6. 110_B , RCLK6 sourced by channel 7. 111_B , RCLK6 sourced by channel 8.

Global Port Configuration Register 6

This register is only valid if COMP = ´0´. For COMP = ´1´ selection of RCLK source is not possible, always sourced by same channel. See **Chapter 3.6**.

GPC6_T	Offset	Reset Value
Global Port Configuration Register 6	**$00D6_H$**	**07_H**

7	6	5	4	3	2	1	0
Res	**SSI16**			Res	**R8S**		
	rw				rw		

Field	Bits	Type	Description
SSI16	6:4	rw	**System Interface Multiplex Mode 16 Mbit/s** See **Chapter 5.6.1**, **Table 58**. *Note: System data rate must be set to 16Mbit/s by SIC1.SSD(1:0) = ´11B´.* 000_B , QuadFALC® compatible multiplexed modes selected. 001_B , 16 Mbit/s, 8-to-1 multiplex system mode selected.
R8S	2:0	rw	**RCLK8 Source Selection** See **Chapter 3.6**. 000_B , RCLK8 sourced by channel 1. 001_B , RCLK8 sourced by channel 2. 010_B , RCLK8 sourced by channel 3. 011_B , RCLK8 sourced by channel 4. 100_B , RCLK8 sourced by channel 5. 101_B , RCLK8 sourced by channel 6. 110_B , RCLK8 sourced by channel 7. 111_B , RCLK8 sourced by channel 8.

In-Band Loop Detection Time Register

See **Chapter 5.5.7**.

INBLDTR_T	Offset	Reset Value
In-Band Loop Detection Time Register	**$00D7_H$**	**00_H**

7	6	5	4	3	2	1	0
Res		**INBLDR**		Res		**INBLDT**	
		rw				rw	

Field	Bits	Type	Description
INBLDR	5:4	rw	**In-Band Loop Detection Time for Line Side** 00_B , at least 16 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 01_B , at least 32 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 10_B , “In-band loop sequences” must be valid for at least 4 seconds to perform automatic loop switching. 11_B , “In-band loop sequences” must be valid for at least 5 seconds to perform automatic loop switching.
INBLDT	1:0	rw	**In-Band Loop Detection Time for System Side** 00_B , at least 16 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 01_B , at least 32 consecutive “In-band loop sequences” must be valid to perform automatic loop switching. 10_B , “In-band loop sequences” must be valid for at least 4 seconds to perform automatic loop switching. 11_B , “In-band loop sequences” must be valid for at least 5 seconds to perform automatic loop switching.

Automatic Loop Switching Register

Enabling of automatic loop switching by In-band loop codes, see **Chapter 5.5.7**, and enabling of automatic loop switching by Out-band loop codes, see **Chapter 5.5.8**, is performed by this register.

ALS_T	Offset	Reset Value
Automatic Loop Switching Register	$xxD9_H$	00_H

7	6	5	4	3	2	1	0
Res				SOLS	LOLS	SILS	LILS
				rw	rw	rw	rw

Field	Bits	Type	Description
SOLS	3	rw	**System Out-Band Loop Switching (Payload Loop)** This bit controls if automatic switching of payload loop will be done by Out-Band loop codes from the line or the system side, see **Chapter 5.5.8**. *Note: Detection of BOM messages from the system side is only possible in "inverse configuration" of the HDLC/BOM controllers (MODE.HDLCI = ´1´). Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6).* 0_B , automatic out-band loop switching of payload is disabled (default). 1_B , automatic switching of remote or payload loop by Out-Band loop codes (BOM messages) coming from the line side or system side is enabled if local loop is not active (LIM0.LL = ´0´). Enabling is not recommended for "inverse configuration" of the HDLC/BOM controller.
LOLS	2	rw	**Line Out-Band Loop Switching (Remote Loop)** This bit controls if automatic switching of remote loop will be done by Out-Band loop codes from the line or the system side, see **Chapter 5.5.8**. *Note: Detection of BOM messages from the system side is only possible in "inverse configuration" of the HDLC/BOM controllers (MODE.HDLCI = ´1´). Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6).* 0_B , automatic out-band loop switching of remote loop is disabled (default). 1_B , automatic switching of remote loop by Out-Band loop codes (BOM messages) coming from the line side or the system side is enabled if local loop is not active (LIM0.LL = ´0´).

Field	Bits	Type	Description
SILS	1	rw	**System In-Band Loop Switching (Local Loop)** This bit controls if automatic switching of the local loop will be done by In-Band loop codes from the system side, see **Chapter 5.5.7**. The necessary receiption time of In-band loop codes until an automatic loop switching is performed is configured by INBLDTR.INBLDT(1:0). *Note: This feature is not described in E1/T1/J1 standards. Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6). Setting both, SILS and LILS to ´1´ is forbidden.* 0_B , automatic switching of local loop (“on system side”) is disabled (default). 1_B , automatic switching of local loop (“on system side”) by In-band loop codes detected from the system side is enabled.
LILS	0	rw	**Line In-Band Loop Switching (Remote Loop)** This bit controls if automatic switching of the remote loop will be done by In-Band loop codes from the line side, see **Chapter 5.5.7**. The necessary receiption time of In-band loop codes until an automatic loop switching is performed is configured by INBLDTR.INBLDR(1:0). *Note: Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6). Setting both, SILS and LILS to ´1´ is forbidden.* 0_B , automatic switching of remote loop (“on line side”) is disabled (default). 1_B , automatic switching of remote loop (“on line side”) by In-band loop codes detected from the line side is enabled if local loop is not activated by LIM0.LL = ´1´.

PRBS Time Slot Register 1

Selects the used time slots for PRBS if TPC0.PRM is not ´00b´.See **Chapter 5.7.1**.

PRBSTS1_T	Offset	Reset Value
PRBS Time Slot Register 1	$00DB_H$	00_H

7	6	5	4	3	2	1	0
TS0	**TS1**	**TS2**	**TS3**	**TS4**	**TS5**	**TS6**	**TS7**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS0	7	rw	**PRBS Time Slot 0 Selection** *Note: If "N x 56 kbit/s" mode is selected by TPC0.PRM(1:0) = ´11_b´ this bit is not valid: In this case time slot 0 - which is the frame bit - will not be used for PRBS, independent on bit TSO.* 0_B , no PRBS pattern in time slot 0. 1_B , pattern transmitted/received in time slot 0.
TS1	6	rw	**PRBS Time Slot 1Selection** 0_B , no PRBS pattern in time slot 1. 1_B , pattern transmitted/received in time slot 1.
TS2	5	rw	**PRBS Time Slot 2Selection** 0_B , no PRBS pattern in time slot 2. 1_B , pattern transmitted/received in time slot 2.
TS3	4	rw	**PRBS Time Slot 3 Selection** 0_B , no PRBS pattern in time slot 3. 1_B , pattern transmitted/received in time slot 3.
TS4	3	rw	**PRBS Time Slot 4 Selection** 0_B , no PRBS pattern in time slot 4. 1_B , pattern transmitted/received in time slot 4.
TS5	2	rw	**PRBS Time Slot 5 Selection** 0_B , no PRBS pattern in time slot 5. 1_B , pattern transmitted/received in time slot 5.
TS6	1	rw	**PRBS Time Slot 6 Selection** 0_B , no PRBS pattern in time slot 6. 1_B , pattern transmitted/received in time slot 6.

Field	Bits	Type	Description
TS7	0	rw	**PRBS Time Slot 7 Selection** 0_B , no PRBS pattern in time slot 7. 1_B , pattern transmitted/received in time slot 7.

PRBS Time Slot Register 2

Selects the used time slots for PRBS.

PRBSTS2_T	Offset	Reset Value
PRBS Time Slot Register 2	$00DC_H$	00_H

7	6	5	4	3	2	1	0
TS8	**TS9**	**TS10**	**TS11**	**TS12**	**TS13**	**TS14**	**TS15**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS8	7	rw	**PRBS Time Slot 8 Selection** 0_B , no PRBS pattern in time slot 8. 1_B , pattern transmitted/received in time slot 8.
TS9	6	rw	**PRBS Time Slot 9 Selection** 0_B , no PRBS pattern in time slot 9. 1_B , pattern transmitted/received in time slot 9.
TS10	5	rw	**PRBS Time Slot 10 Selection** 0_B , no PRBS pattern in time slot 10. 1_B , pattern transmitted/received in time slot 10.
TS11	4	rw	**PRBS Time Slot 11 Selection** 0_B , no PRBS pattern in time slot 11. 1_B , pattern transmitted/received in time slot 11.
TS12	3	rw	**PRBS Time Slot 12 Selection** 0_B , no PRBS pattern in time slot 12. 1_B , pattern transmitted/received in time slot 12.
TS13	2	rw	**PRBS Time Slot 13 Selection** 0_B , no PRBS pattern in time slot 13. 1_B , pattern transmitted/received in time slot 13.
TS14	1	rw	**PRBS Time Slot 14 Selection** 0_B , no PRBS pattern in time slot 14. 1_B , pattern transmitted/received in time slot 14.
TS15	0	rw	**PRBS Time Slot 15 Selection** 0_B , no PRBS pattern in time slot 15. 1_B , pattern transmitted/received in time slot 15.

PRBS Time Slot Register 3

Selects the used time slots for PRBS.

PRBSTS3_T	Offset	Reset Value
PRBS Time Slot Register 3	$00DD_H$	00_H

7	6	5	4	3	2	1	0
TS16	**TS17**	**TS18**	**TS19**	**TS20**	**TS21**	**TS22**	**TS23**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS16	7	rw	**PRBS Time Slot 16 Selection** 0_B , no PRBS pattern in time slot 16. 1_B , pattern transmitted/received in time slot 16.
TS17	6	rw	**PRBS Time Slot 17 Selection** 0_B , no PRBS pattern in time slot 17. 1_B , pattern transmitted/received in time slot 17.
TS18	5	rw	**PRBS Time Slot 18 Selection** 0_B , no PRBS pattern in time slot 18. 1_B , pattern transmitted/received in time slot 18.
TS19	4	rw	**PRBS Time Slot 19 Selection** 0_B , no PRBS pattern in time slot 19. 1_B , pattern transmitted/received in time slot 19.
TS20	3	rw	**PRBS Time Slot 20 Selection** 0_B , no PRBS pattern in time slot 20. 1_B , pattern transmitted/received in time slot 20.
TS21	2	rw	**PRBS Time Slot 21 Selection** 0_B , no PRBS pattern in time slot 21. 1_B , pattern transmitted/received in time slot 21.
TS22	1	rw	**PRBS Time Slot 22 Selection** 0_B , no PRBS pattern in time slot 22. 1_B , pattern transmitted/received in time slot 22.
TS23	0	rw	**PRBS Time Slot 23 Selection** 0_B , no PRBS pattern in time slot 23. 1_B , pattern transmitted/received in time slot 23.

PRBS Time Slot Register 4

Selects the used time slots for PRBS.

PRBSTS4_T	Offset	Reset Value
PRBS Time Slot Register 4	$00DE_H$	00_H

7	6	5	4	3	2	1	0
TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS24	7	rw	**PRBS Time Slot 24 Selection** 0_B , no PRBS pattern in time slot 24. 1_B , pattern transmitted/received in time slot 24.
TS25	6	rw	**PRBS Time Slot 25 Selection** 0_B , no PRBS pattern in time slot 25. 1_B , pattern transmitted/received in time slot 25.
TS26	5	rw	**PRBS Time Slot 26 Selection** 0_B , no PRBS pattern in time slot 26. 1_B , pattern transmitted/received in time slot 26.
TS27	4	rw	**PRBS Time Slot 27 Selection** 0_B , no PRBS pattern in time slot 27. 1_B , pattern transmitted/received in time slot 27.
TS28	3	rw	**PRBS Time Slot 28 Selection** 0_B , no PRBS pattern in time slot 28. 1_B , pattern transmitted/received in time slot 29.
TS29	2	rw	**PRBS Time Slot 29 Selection** 0_B , no PRBS pattern in time slot 29. 1_B , pattern transmitted/received in time slot 29.
TS30	1	rw	**PRBS Time Slot 30 Selection** 0_B , no PRBS pattern in time slot 30. 1_B , pattern transmitted/received in time slot 30.
TS31	0	rw	**PRBS Time Slot 31 Selection** 0_B , no PRBS pattern in time slot 31. 1_B , pattern transmitted/received in time slot 31.

Interrupt Mask Register 7

Masks interrupt bits of register ISR7.

IMR7_T	Offset	Reset Value
Interrupt Mask Register 7	$xxDF_H$	FF_H

7	6	5	4	3	2	1	0
Res			XCLKSS1	XCLKSS0	Res		
			rw	rw			

Field	Bits	Type	Description
XCLKSS1	4	rw	**XCLKSS1 Interrupt Masking** 0_B , ISR7.XCLKSS1 is enabled. 1_B , ISR7.XCLKSS1 is disabled
XCLKSS0	3	rw	**XCLKSS0 Interrupt Masking** 0_B , ISR7.XCLKSS0 is enabled. 1_B , ISR7.XCLKSS0 is disabled

8.2 Detailed Description of T1/J1 Status Registers

Receive FIFO - HDLC Channel 1 - Lower Byte

RFIFO1L_T	Offset	Reset Value
Receive FIFO - HDLC Channel 1 - Lower Byte	$xx00_H$	xx_H

7	6	5	4	3	2	1	0
RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF7	7	r	**RFIFO Data** Reading data from RFIFO of HDLC channel 1 can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface. The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT(1:0) and MODE.RFT2 (RFIFO threshold level), see Chapter 3.4.3. Data Transfer: Up to 64bytes/32 words of received data can be read from the RFIFO following an RPF or an RME interrupt. RPF Interrupt: A fixed number of bytes/words to be read (64, 32, 16, 4, 2 bytes). The message is not yet complete. RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers. RFIFO is released by issuing the RMC (Receive Message Complete) command.
RF6	6	r	
RF5	5	r	
RF4	4	r	
RF3	3	r	
RF2	2	r	
RF1	1	r	
RF0	0	r	

Receive FIFO - HDLC Channel 1 - Higher Byte

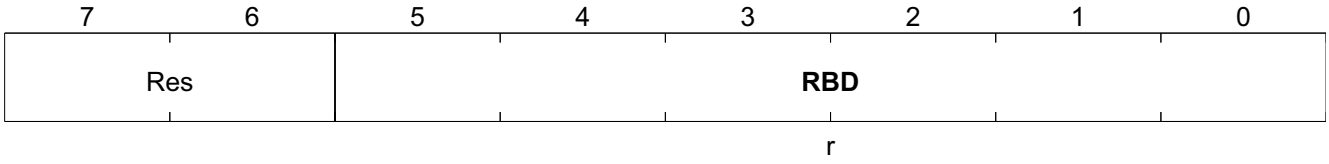
RFIFO1H_T	Offset	Reset Value
Receive FIFO - HDLC Channel 1 - Higher Byte	$xx01_H$	xx_H

7	6	5	4	3	2	1	0
RF15	**RF14**	**RF13**	**RF12**	**RF11**	**RF10**	**RF9**	**RF8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF15	7	r	**RFIFO Data** Reading data from RFIFO of HDLC channel 1 can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface. The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT(1:0) and MODE.RFT2 (RFIFO threshold level), see **Chapter 3.4.3**. Data Transfer: Up to 64bytes/32 words of received data can be read from the RFIFO following an RPF or an RME interrupt. RPF Interrupt: A fixed number of bytes/words to be read (64, 32, 16, 4, 2 bytes). The message is not yet complete. RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers. RFIFO is released by issuing the RMC (Receive Message Complete) command.
RF14	6	r	
RF13	5	r	
RF12	4	r	
RF11	3	r	
RF10	2	r	
RF9	1	r	
RF8	0	r	

Receive Buffer Delay

RBD_T	Offset	Reset Value
Receive Buffer Delay	$xx49_H$	xx_H



Field	Bits	Type	Description
RBD	5:0	r	**Receive Elastic Buffer Delay** These bits informs the user about the current delay (in time slots) through the receive elastic buffer. The delay is updated every 386 or 193 bits (SIC1.RBS(1:0)). Before reading this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed. 000000_B , Delay < 1 time slot $_B$, ... 111111_B , Delay > 63 time slots

Version Status Register

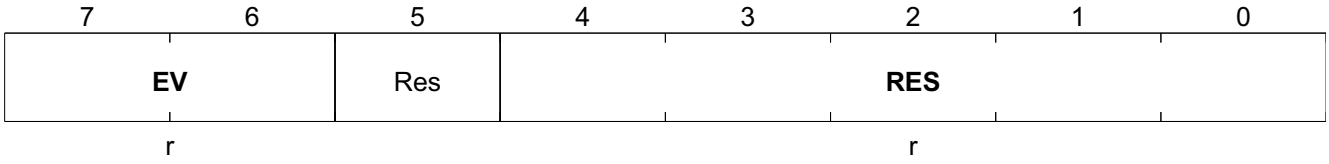
VSTR_T	Offset	Reset Value
Version Status Register	$xx4A_H$	H

7	6	5	4	3	2	1	0
VSTR							
r							

Field	Bits	Type	Description
VSTR	7:0	r	**Version Number of Chip** Status information depends on the setting of input signal COMP. See **Figure 96** for more detail.

Receive Equalizer Status

RES_T	Offset	Reset Value
Receive Equalizer Status	$xx4B_H$	00_H



Field	Bits	Type	Description
EV	7:6	r	**Equalizer Status Valid** These bits informs the user about the current state of the receive equalization network. 00_B , Equalizer status not valid, still adapting 01_B , Equalizer status valid 10_B , Equalizer status not valid 11_B , Equalizer status valid but high noise floor
RES	4:0	r	**Receive Equalizer Status** The current line attenuation status in steps of about 1.4 dB are displayed in these bits. Only valid if bits EV(1:0) = ´01_b´. Accuracy: ± 2 digits, based on temperature influence and noise amplitude variations. 00000_B , Minimum attenuation: 0 dB $_B$, ... 11001_B , Maximum attenuation: -36 dB

Framer Receive Status Register 0

FRS0_T	Offset	Reset Value
Framer Receive Status Register 0	$xx4C_H$	xx_H

7	6	5	4	3	2	1	0
LOS	AIS	LFA	RRA	Res		LMFA	FSRF
r	r	r	r			r	r

Field	Bits	Type	Description
LOS	7	r	**Loss-of-Signal (Red Alarm)** Detection: This bit is set when the incoming signal has “no transitions“ (analog interface) or logical zeros (digital interface) in a time interval of T consecutive pulses, where T is programmable by PCD register: Total account of consecutive pulses: 16 < T < 4096. Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL(2:0). Recovery: • Analog interface: The bit is reset in short-haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL(2:0)) for at least M pulse periods defined by register PCR in the PCD time interval. In long-haul mode additionally bit RES.6 must be set for at least 250 µs. • Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval. With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. For additionally recovery conditions refer also to register LIM2.LOS1. The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 6,7 and no alarm condition exists.
AIS	6	r	**Alarm Indication Signal (Blue Alarm)** This bit is set when the conditions defined by bit FMR4.AIS3 are detected. The flag stays active for at least one multiframe. With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set. It is reset with the beginning of the next following multiframe if no alarm condition is detected.The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 7 and no alarm condition exists.
LFA	5	r	**Loss of Frame Alignment** The flag is set if pulseframe synchronization has been lost. The conditions are specified by bit FMR4.SSC(1:0). Setting this bit causes an interrupt (ISR2.LFA). The flag is cleared when synchronization has been regained. Additionally interrupt status ISR2.FAR is set with clearing this bit.

Field	Bits	Type	Description
RRA	4	r	**Receive Remote Alarm (Yellow Alarm)** The flag is set after detecting remote alarm (yellow alarm). Conditions for setting/resetting are defined by bit RC0.RRAM. With the rising edge of this bit an interrupt status bit ISR2.RA is set. With the falling edge of this bit an interrupt status bit ISR2.RAR is set. The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4,5,7 and no alarm condition exists.
LMFA	1	r	**Loss Of Multiframe Alignment** Set in F12 or F72 format when 2 out of 4 (or 5 or 6) multiframe alignment patterns are incorrect. Additionally the interrupt status bit ISR2.LMFA is set. Cleared after multiframe synchronization has been regained. With the falling edge of this bit an interrupt status bit ISR2.MFAR is generated.
FSRF	0	r	**Frame Search Restart Flag** Toggles when no framing candidate (pulse framing or multiframing) is found and a new frame search is started.

Framer Receive Status Register 1

FRS1_T	Offset	Reset Value
Framer Receive Status Register 1	$xx4D_H$	xx_H

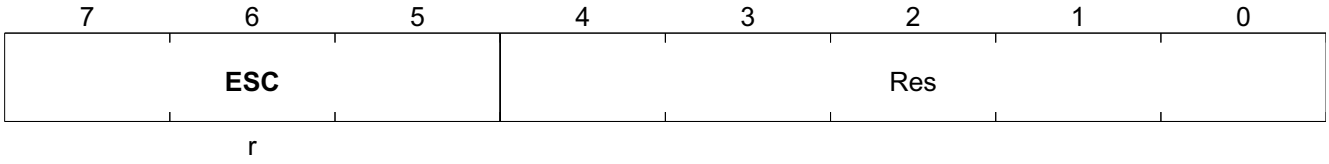
7	6	5	4	3	2	1	0
EXZD	**PDEN**	Res	**LLBDD**	**LLBAD**	Res	**XLS**	**XLO**
r	r		r	r		r	r

Field	Bits	Type	Description
EXZD	7	r	**Excessive Zeros Detected** Significant only if excessive zeros detection is enabled (FMR2.EXZE = ´1´). Set after detecting of more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros in the received bit stream. This bit is cleared on read.
PDEN	6	r	**Pulse-Density Violation Detected** The pulse-density of the received data stream is below the requirement defined by ANSI T1. 403 or more than 14 consecutive zeros are detected. With the violation of the pulse-density this bit is set and remains active until the pulse-density requirement is fulfilled for 23 consecutive "1"-pulses. Additionally an interrupt status ISR0.PDEN is generated with the rising edge of PDEN.
LLBDD	4	r	**Line Loop-Back Deactivation Signal Detected** This bit is set in case of the LLB deactivate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.Any change of this bit causes an LLBSC interrupt.
LLBAD	3	r	**Line Loop-Back Activation Signal Detected PRBS Status** Depending on bit LCR1.EPRM the source of this status bit changed. • LCR1.EPRM = ´0´: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation. Any change of this bit causes an LLBSC interrupt. • LCR1.EPRM = ´1´: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of up to 10^{-3}. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo-random binary sequence.

Field	Bits	Type	Description
XLS	1	r	**Transmit Line Short** Significant only if the ternary line interface is selected by LIM1.DRS = ´0´. Note that shorts in generic transmit line interface mode are not detected and will not ham the device 0_B , Normal operation. No short is detected. 1_B , The XL1 and XL2 are shortened for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high-impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high-impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen.
XLO	0	r	**Transmit Line Open** 0_B , Normal operation 1_B , This bit is set if at least 32 consecutive zeros were sent on pins XL1/XL2 or XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen.

Framer Receive Status Register 2

FRS2_T	Offset	Reset Value
Framer Receive Status Register 2	$xx4E_H$	xx_H



Field	Bits	Type	Description
ESC	7:5	r	**Error Simulation Counter** This three-bit counter is incremented by setting bit FMR0.SIM. The state of the counter determines the function to be tested. For complete checking of the alarm indications, eight simulation steps are necessary (FRS2.ESC = ´0´ after a complete simulation).

Table 134 Alarm Simulation States

Tested Alarms ESC(2:0) =	0	1	2	3	4	5	6	7
LFA			x				x	
LMFA			x				x	
RRA (bit2 = 0)		x						
RRA (S-bit frame 12)			x					
RRA (DL-pattern)							x	
LOS[1)]		x	x			x		
EBC[2)] (F12,F72)			x				(x)	
EBC[2)] (only ESF)		x	x			x	(x)	
AIS[1)]		x	x			x	x	
FEC[2)]			x				(x)	
CVC		x	x			x		
CEC (only ESF)		x	x			x	x	
RSP		x						
RSN						x		
XSP		x						
XSN						x		
BEC[1)]		x	x			x		
COEC			x				x	

1) Only active during FMR0.SIM = 1

2) FEC is counting +2 while EBC is counting +1 if the framer is in synchronous state; if asynchronous in state 2 but synchronous in state 6, counters are incremented during state 6

Some of these alarm indications are simulated only if the OctalFALCTM is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7 pending status flags are reset automatically and clearing of the error counters and interrupt status registers ISR(7:0) should be done. Incrementing the simulation counter should not be done at time intervals shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations might occur at later steps. Control bit FMR0.SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

Framing Error Counter Lower Byte

FECL_T	Offset	Reset Value
Framing Error Counter Lower Byte	$xx50_H$	00_H

7	6	5	4	3	2	1	0
FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FE7	7	r	**Framing Errors** This 16-bit counter is incremented when a FAS word has been received with an error.Framing errors are counted during basic frame synchronous state only (but even if multiframe synchronous state is not reached yet). During alarm simulation, the counter is incremented every 250 ms up to its saturation. The error counter does not roll over.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
FE6	6	r	
FE5	5	r	
FE4	4	r	
FE3	3	r	
FE2	2	r	
FE1	1	r	
FE0	0	r	

Framing Error Counter Higher Byte

FECH_T	Offset	Reset Value
Framing Error Counter Higher Byte	$xx51_H$	00_H

7	6	5	4	3	2	1	0
FE15	**FE14**	**FE13**	**FE12**	**FE11**	**FE10**	**FE9**	**FE8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FE15	7	r	**Framing Errors** This 16-bit counter is incremented when a FAS word has been received with an error.Framing errors are counted during basic frame synchronous state only (but even if multiframe synchronous state is not reached yet). During alarm simulation, the counter is incremented every 250 ms up to its saturation. The error counter does not roll over.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
FE14	6	r	
FE13	5	r	
FE12	4	r	
FE11	3	r	
FE10	2	r	
FE9	1	r	
FE8	0	r	

Code Violation Counter Lower Byte

CVCL_T	Offset	Reset Value
Code Violation Counter Lower Byte	$xx52_H$	00_H

7	6	5	4	3	2	1	0
CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CV7	7	r	**Code Violations** No function if NRZ code has been enabled.If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit FMR0.EXTD. If simple AMI coding is enabled (FMR0.RC(1:0) = ´01_b´) all bipolar violations are counted. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CV6	6	r	
CV5	5	r	
CV4	4	r	
CV3	3	r	
CV2	2	r	
CV1	1	r	
CV0	0	r	

Code Violation Counter Higher Byte

CVCH_T	Offset	Reset Value
Code Violation Counter Higher Byte	$xx53_H$	00_H

7	6	5	4	3	2	1	0
CV15	CV14	CV13	CV12	CV11	CV10	CV9	CV8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CV15	7	r	**Code Violations** No function if NRZ code has been enabled.If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit FMR0.EXTD. If simple AMI coding is enabled (FMR0.RC(1:0) = ´01_b´) all bipolar violations are counted. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CV14	6	r	
CV13	5	r	
CV12	4	r	
CV11	3	r	
CV10	2	r	
CV9	1	r	
CV8	0	r	

CRC Error Counter 1 Lower Byte

CEC1L_T	Offset	Reset Value
CRC Error Counter 1 Lower Byte	$xx54_H$	00_H

7	6	5	4	3	2	1	0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CR7	7	r	**CRC Errors** No function if doubleframe format is selected.In CRC-multiframe mode, the 16-bit counter is incremented when a CRC-submultiframe has been received with a CRC error. CRC errors are not counted during asynchronous state. The error counter does not roll over.During alarm simulation, the counter is incremented once per submultiframe up to its saturation.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC1 is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CR6	6	r	
CR5	5	r	
CR4	4	r	
CR3	3	r	
CR2	2	r	
CR1	1	r	
CR0	0	r	

CRC Error Counter 1 Higher Byte

CEC1H_T	Offset	Reset Value
CRC Error Counter 1 Higher Byte	$xx55_H$	00_H

7	6	5	4	3	2	1	0
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CR15	7	r	**CRC Errors** No function if doubleframe format is selected.In CRC-multiframe mode, the 16-bit counter is incremented when a CRC-submultiframe has been received with a CRC error. CRC errors are not counted during asynchronous state. The error counter does not roll over.During alarm simulation, the counter is incremented once per submultiframe up to its saturation.Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC1 is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CR14	6	r	
CR13	5	r	
CR12	4	r	
CR11	3	r	
CR10	2	r	
CR9	1	r	
CR8	0	r	

E-Bit Error Counter Lower Byte

EBCL_T	Offset	Reset Value
E-Bit Error Counter Lower Byte	$xx56_H$	00_H

7	6	5	4	3	2	1	0
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
EB7	7	r	**E-Bit Errors** If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. The error counter does not roll over. During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
EB6	6	r	
EB5	5	r	
EB4	4	r	
EB3	3	r	
EB2	2	r	
EB1	1	r	
EB0	0	r	

E-Bit Error Counter Higher Byte

EBCH_T	Offset	Reset Value
E-Bit Error Counter Higher Byte	$xx57_H$	00_H

7	6	5	4	3	2	1	0
EB15	**EB14**	**EB13**	**EB12**	**EB11**	**EB10**	**EB9**	**EB8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
EB15	7	r	**E-Bit Errors** If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. The error counter does not roll over. During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is reset automatically with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
EB14	6	r	
EB13	5	r	
EB12	4	r	
EB11	3	r	
EB10	2	r	
EB9	1	r	
EB8	0	r	

Bit Error Counter Lower Bytes

BECL_T	Offset	Reset Value
Bit Error Counter Lower Bytes	$xx58_H$	00_H

7	6	5	4	3	2	1	0
BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
BEC7	7	r	**Bit Error Counter** If the PRBS monitor is enabled by LCR1.EPRM = ´1´ this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state FRS1.LLBAD = ´1´. The error counter does not roll over.During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit FMR1.ECM.If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DBEC is automatically reset with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
BEC6	6	r	
BEC5	5	r	
BEC4	4	r	
BEC3	3	r	
BEC2	2	r	
BEC1	1	r	
BEC0	0	r	

Bit Error Counter Higher Bytes

BECH_T	Offset	Reset Value
Bit Error Counter Higher Bytes	$xx59_H$	00_H

7	6	5	4	3	2	1	0
BEC15	**BEC14**	**BEC13**	**BEC12**	**BEC11**	**BEC10**	**BEC9**	**BEC8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
BEC15	7	r	**Bit Error Counter** If the PRBS monitor is enabled by LCR1.EPRM = ´1´ this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state FRS1.LLBAD = ´1´. The error counter does not roll over.During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit FMR1.ECM.If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DBEC is automatically reset with reading the error counter high byte. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
BEC14	6	r	
BEC13	5	r	
BEC12	4	r	
BEC11	3	r	
BEC10	2	r	
BEC9	1	r	
BEC8	0	r	

COFA Event Counter

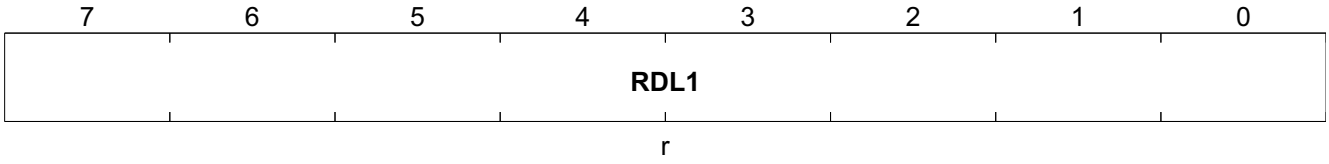
COEC_T	Offset	Reset Value
COFA Event Counter	$xx5A_H$	00_H

7	6	5	4	3	2	1	0
COE7	COE6	COE5	COE4	COE3	COE2	COE1	COE0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
COE7	7	r	**Multiframe Counter** If GCR.ECMC = ´1´ this 6-bit counter increments with each multiframe period in the asynchronous state FRS0.LFA/LMFA = ´1´. The error counter does not roll over.
COE6	6		
COE5	5		
COE4	4		
COE3	3		
COE2	2		
COE1	1	r	**Change of Frame Alignment Counter** If GCR.ECMC = ´1´ this 2-bit counter increments with each detected change of frame/multiframe alignment. The error counter does not roll over. During alarm simulation, the counter is incremented once per multiframe. Clearing and updating the counter is done according to bit FMR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the event counter bit DEC.DCOEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCOEC is automatically reset with reading the error counter high byte on address ´$5B_H$´. Data read on ´$5B_H$´ is not defined. If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
COE0	0		

Receive DL-Bit Register 1

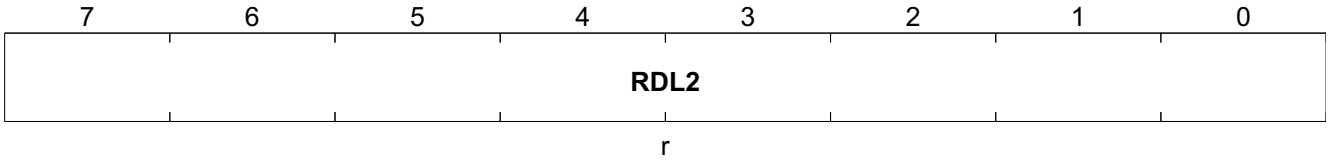
RDL1_T	Offset	Reset Value
Receive DL-Bit Register 1	$xx5C_H$	xx_H



Field	Bits	Type	Description
RDL1	7:0	r	**Receive DL-Bit** Only valid if F12, F24 or F72 format is enabled.The received FS/DL-Bits are shifted into this register. RDL10 is received in frame 1 and RDL17 in frame 15, if F24 format is enabled. RDL10 is received in frame 26 and RDL17 in frame 40, if F72 format is enabled. In F12 format the FS-Bits of a complete multiframe is stored in this register. RDL10 is received in frame 2 and RDL15 in frame 12. This register is updated with every receive multiframe begin interrupt ISR0.RMB. Two kinds of DL- bit accesses are selectable in ESF mode by register bit FMR5.DLM, see **Chapter 5.3.6.1**.

Receive DL-Bit Register 2

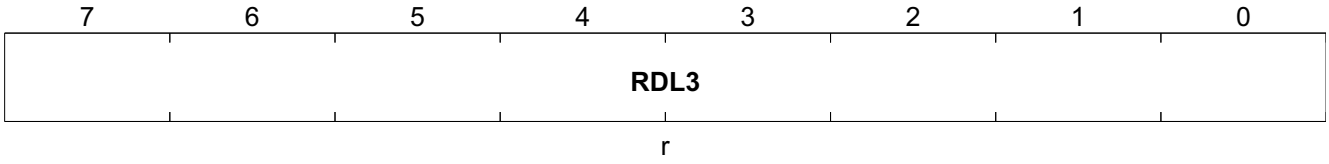
RDL2_T	Offset	Reset Value
Receive DL-Bit Register 2	$xx5D_H$	xx_H



Field	Bits	Type	Description
RDL2	7:0	r	**Receive DL-Bit** Only valid if F24 or F72 format is enabled.The received DL-Bits are shifted into this register. RDL20 is received in frame 17 and RDL23 in frame 23, if F24 format is enabled. RDL20 is received in frame 42 and RDL27 in frame 56, if F72 format is enabled. This register is updated with every receive multiframe begin interrupt ISR0.RMB. Two kinds of DL- bit accesses are selectable in ESF mode by register bit FMR5.DLM, see **Chapter 5.3.6.1**.

Receive DL-Bit Register 3

RDL3_T	Offset	Reset Value
Receive DL-Bit Register 3	$xx5E_H$	xx_H



Field	Bits	Type	Description
RDL3	7:0	r	**Receive DL-Bit** Only valid if F72 format is enabled.The received DL-Bits are shifted into this register. RDL30 is received in frame 58 and RDL37 in frame 72, if F72 format is enabled. This register is updated with every receive multiframe begin interrupt ISR0.RMB. Two kinds of DL- bit accesses are selectable in ESF mode by register bit FMR5.DLM, see **Chapter 5.3.6.1**.

Receive Signaling Pointer 1

RSP1_T	Offset	Reset Value
Receive Signaling Pointer 1	$xx62_H$	00_H

7	6	5	4	3	2	1	0
RS8C	RS7C	RS6C	RS5C	RS4C	RS3C	RS2C	RS1C
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RS8C	7	r	**Receive Signaling Register RS(8:1) Changed** A one in each bit position indicates that the received signaling data in the corresponding RS(8:1) registers are updated. Bit RS1C is the pointer for register RS1, while RS8C points to RS8.
RS7C	6		
RS6C	5		
RS5C	4		
RS4C	3		
RS3C	2		
RS2C	1		
RS1C	0		

Receive Signaling Pointer 2

RSP2_T	Offset	Reset Value
Receive Signaling Pointer 2	$xx63_H$	00_H

7	6	5	4	3	2	1	0
Res				RS12C	RS11C	RS10C	RS9C
				r	r	r	r

Field	Bits	Type	Description
RS12C	3	r	**Receive Signaling Register RS(12:9) Changed** A one in each bit position indicates that the received signaling data in the corresponding RS(12:9) registers are updated. Bit RS9C is the pointer for register RS9, while RS12C points to RS12
RS11C	2		
RS10C	1		
RS9C	0		

Signaling Status Register

SIS_T	Offset	Reset Value
Signaling Status Register	$xx64_H$	xx_H

7	6	5	4	3	2	1	0
XDOV	XFW	XREP	IVB	RLI	CEC	SFS	BOM
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
XDOV	7	r	**Transmit Data Overflow - HDLC Channel 1** More than 64 bytes have been written to the XFIFO.This bit is cleared either • By a transmitter reset command XRES or • When all bytes in the accessible half of the XFIFO have been moved in the inaccessible half (shadow register). 0_B , normal FIFO operation. 1_B , number of bytes written to the FIFO exceeds the FIFO size.
XFW	6	r	**Transmit FIFO Write Enable - HDLC Channel 1** Data can be written to the XFIFO.
XREP	5	r	**Transmission Repeat - HDLC Channel 1** Status indication of CMDR.XREP.
IVB	4	r	**Invalid BOM Frame Received - HDLC Channel 1** 0_B , Valid BOM frame (11111111, 0xxxxxx0) received. 1_B , Invalid BOM frame received.
RLI	3	r	**Receive Line Inactive - HDLC Channel 1** Neither flags as interframe time fill nor frames are received in the signaling time slot.
CEC	2	r	**Command Executing** *Note: CEC is active at most 2.5 periods of the current system data rate.* 0_B , No command is currently executed, the CMDR register can be written to. 1_B , A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.
SFS	1	r	**Status Freeze Signaling** 0_B , Freeze signaling status inactive. 1_B , Freeze signaling status active.

Field	Bits	Type	Description
BOM	0	r	**Bit Oriented Message - HDLC Channel 1** Significant only in ESF frame format and auto switching mode is enabled. See **Chapter 5.3.4**. 0_B , HDLC/BOM controller 1 in HDLC mode 1_B , HDLC/BOM controller 1 in BOM mode

Receive Signaling Status Register

SIS relates to the last received HDLC or BOM frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

RSIS_T	Offset	Reset Value
Receive Signaling Status Register	$xx65_H$	xx_H

7	6	5	4	3	2	1	0
VFR	RDO	CRC16	RAB	HA		HFR	LA
r	r	r	r	r		r	r

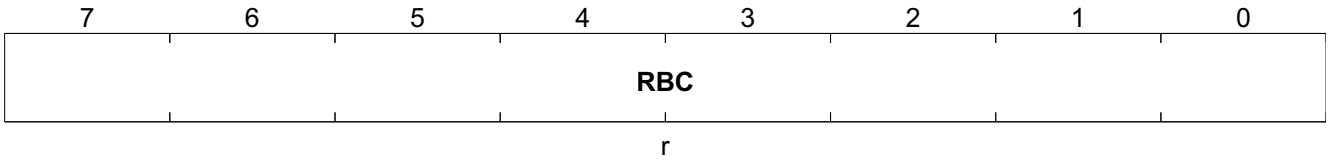
Field	Bits	Type	Description
VFR	7	r	**Valid Frame - HDLC Channel 1** Determines whether a valid frame has been received. An invalid frame is either a frame which is not an integer number of 8 bits (nx8 bits) in length (e.g. 25 bits), or a frame which is too short taking into account the operation mode selected by MODE (MDS(2:0)) and the selection of receive CRC on/off (CCR2.RCRC) as follows: • MDS(2:0) = ´011_b´ (16 bit Address), RCRC = ´0´: 4 bytes; RCRC = 1: 3 or 4 bytes • MDS(2:0) = 010_b´ (8 bit Address), RCRC = ´0´: 3 bytes; RCRC = 1: 2 or 3 bytes *Note: Shorter frames are not reported.* 1_B , Valid 0_B , Invalid
RDO	6	r	**Receive Data Overflow - HDLC Channel 1** A data overflow has occurred during reception of the frame.Additionally, an interrupt can be generated (refer to ISR1.RDO/IMR1.RDO).
CRC16	5	r	**CRC16 Compare/Check - HDLC Channel 1** 0_B , CRC check failed; received frame contains errors. 1_B , CRC check o.k.; received frame is error-free.
RAB	4	r	**Receive Message Aborted - HDLC Channel 1** The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.This bit is set in SS7 mode, if the maximum number of octets (272+7) is exceeded.

Field	Bits	Type	Description
HA	3:2	r	**High Byte Address Compare - HDLC Channel 1** Significant only if 2-byte address mode or SS7 mode has been selected.In operating modes which provide high byte address recognition, the OctalFALCTM compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values ´FE_H´ and ´FC_H´ (broadcast address). CASE A Depending on the result of this comparison, the following bit combinations are possible (SS7 support not active): *Note: If RAH1, RAH2 contain identical values, a match is indicated by "10" or "11".* 00_B , RAH2 has been recognized 01_B , Broadcast address has been recognized 10_B , RAH1 has been recognized C/R = ´0´ (bit 1) 11_B , RAH1 has been recognized C/R = ´1´ (bit 1) **High Byte Address Compare - HDLC Channel 1** If Signaling System 7 support is activated (see MODE register), the bit functions are defined as follows: 00_B , not valid 01_B , Fill In signaling unit (FISU) detected 10_B , Link status signaling unit (LSSU) detected 11_B , Message signaling unit (MSU) detected
HFR	1	r	**HDLC Frame Format - HDLC Channel 1** *Note: Bits RSIS.(7:2) and RSIS.0 are not valid with a BOM frame. This means, if HFR = 0, all other bits of RSIS have to be ignored. Not valid in SS7 mode. Bit HFR has to be ignored, if SS7 mode is selected.* 0_B , A BOM frame was received. 1_B , A HDLC frame was received.
LA	0	r	**Low Byte Address Compare - HDLC Channel 1** Significant in HDLC modes only.The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared to two registers. (RAL1, RAL2). *Note: Not valid in SS7 mode. Bit LA has to be ignored, if SS7 mode is selected.* 0_B , RAL2 has been recognized 1_B , RAL1 has been recognized

Receive Byte Count Low - HDLC Channel 1

Together with RBCH, bits RBC(11:8), indicates the length of a received frame (1 to 4095 bytes). Bits RBC(4:0) indicate the number of valid bytes currently in RFIFO. These registers must be read by the external micro controller following a RME interrupt.

RBCL_T	Offset	Reset Value
Receive Byte Count Low - HDLC Channel 1	$xx66_H$	xx_H



Field	Bits	Type	Description
RBC	7:0	r	**Receive Frame Length Lower Bytes**

Received Byte Count High - HDLC Channel 1

RBCH_T	Offset	Reset Value
Received Byte Count High - HDLC Channel 1	$xx67_H$	$000xxxxx_H$

7	6	5	4	3	2	1	0
Res			**OV**	**RBC11**	**RBC10**	**RBC9**	**RBC8**
			r	r	r	r	r

Field	Bits	Type	Description
OV	4	r	**Counter Overflow - HDLC Channel 1** More than 4095 bytes received.
RBC11	3	r	**Receive Byte Count - HDLC Channel 1 (most significant bits)** Together with RBCL (bits RBC7...0) indicates the length of the received frame.
RBC10	2		
RBC9	1		
RBC8	0		

Interrupt Status Register 0

All bits are reset when ISR0 is read. If bit GCR.VIS is set, interrupt statuses in ISR0 are flagged although they are masked by register IMR0. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS. See Chapter 3.4.4.

ISR0_T	Offset	Reset Value
Interrupt Status Register 0	$xx68_H$	00_H

7	6	5	4	3	2	1	0
RME	RFS_BIV	ISF	RMB	RSC	CRC6	PDEN	RPF
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RME	7	r	**Receive Message End - HDLC Channel 1** One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC(4:0). Additional information is available in the RSIS register.
RFS_BIV	6	r	**Receive Frame Start - HDLC Channel 1** This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After a RFS interrupt, the contents of RAL1and RSIS.3-1 are valid and can be read by the external micro controller. BOM Frame Invalid - HDLC Channel 1 Only valid if CCR2.RBFE is set.When the BOM receiver left the valid BOM status (detecting 7 out of 10 equal BOM frames) this interrupt is generated.
ISF	5	r	**Incorrect Sync Format - HDLC Channel 1** The OctalFALCTM did not detect eight consecutive ones within 32 bits in BOM mode. Only valid if BOM receiver has been activated.
RMB	4	r	**Receive Multiframe Begin** This bit is set with the beginning of a received multiframe of the receive line timing.
RSC	3	r	**Received Signaling Information Changed** This interrupt bit is set during each multiframe in which signaling information on at least one channel changes its value from the previous multiframe. This interrupt only occurs in the synchronous state. The registers RS(12:1) should be read within the next 3 ms otherwise the contents is lost.

Field	Bits	Type	Description
CRC6	2	r	**Receive CRC6 Error** 0_B , No CRC6 error occurs. 1_B , The CRC6 check of the last received multiframe failed.
PDEN	1	r	**Pulse-Density Violation** The pulse-density violation of the received data stream defined by ANSI T1. 403 is violated. More than 14 consecutive zeros or less than N ones in each and every time window of 8x(N+1) data bits (N = 23) are detected. If GCR.SCI is set high this interrupt status bit is activated with every change of state of FRS1.PDEN.
RPF	0	r	**Receive Pool Full - HDLC Channel 1** 32 bytes of a frame have arrived in the receive FIFO. The frame is not yet received completely.

Interrupt Status Register 1

All bits are reset when ISR1 is read. If bit GCR.VIS is set, interrupt statuses in ISR1 are flagged although they are masked by register IMR1. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS. See **Chapter 3.4.4**.

ISR1_T	Offset	Reset Value
Interrupt Status Register 1	$xx69_H$	00_H

7	6	5	4	3	2	1	0
CASE	**RDO**	**ALLS**	**XDU**	**XMB**	**SUEX**	**XLSC**	**XPR**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CASE	7	r	**Transmit CAS Register Empty** In ESF format this bit is set with the beginning of a transmitted multiframe related to the internal transmitter timing. In F12 and F72 format this interrupt occurs every 24 frames to inform the user that new bit robbing data may be written to the XS(12:1) registers. This interrupt is generated only if the serial signaling access on the system highway is not enabled.
RDO	6	r	**Receive Data Overflow - HDLC Channel 1** This interrupt status indicates that the external micro controller did not respond fast enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again. *Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.*
ALLS	5	r	**All Sent - HDLC Channel 1** This bit is set if the last bit of the current frame has been sent completely and XFIFO is empty. This bit is valid in HDLC mode only.
XDU	4	r	**Transmit Data Underrun - HDLC Channel 1** Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued. *Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU should not be masked by register IMR1. Additionally, CMDR.SRES must be set after XDU occurs to reset the transmit signaling controller.*
XMB	3	r	**Transmit Multiframe Begin** This bit is set with the beginning of a transmitted multiframe related to the internal transmit line interface timing.

Field	Bits	Type	Description
SUEX	2	r	**Signaling Unit Error Threshold Exceeded - HDLC Channel 1** Masks the indication by interrupt that the selected error threshold for SS7 signaling units has been exceeded. *Note: SUEX is only valid, if SS7 mode is selected. If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).* 0_B , Signaling unit error count below selected threshold 1_B , Signaling unit error count exceeded selected threshold
XLSC	1	r	**Transmit Line Status Change** XLSC is set with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS. The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.
XPR	0	r	**Transmit Pool Ready - HDLC Channel 1** A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2

All bits are reset when ISR2 is read. If bit GCR.VIS is set, interrupt statuses in ISR2 are flagged although they are masked by register IMR2. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS. See **Chapter 3.4.4**.

ISR2_T	Offset	Reset Value
Interrupt Status Register 2	$xx6A_H$	00_H

7	6	5	4	3	2	1	0
FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FAR	7	r	**Frame Alignment Recovery** The framer has reached synchronization. Set with the falling edge of bit FRS0.LFA. It is set also after alarm simulation is finished and the receiver is still synchronous.
LFA	6	r	**Loss of Frame Alignment** The framer has lost synchronization and bit FRS0.LFA is set. It is set during alarm simulation.
MFAR	5	r	**Multiframe Alignment Recovery** Set when the framer has reached multiframe alignment in F12 or F72 format. With the negative transition of bit FRS0.LMFA this bit is set. It is set during alarm simulation.
LMFA	4	r	**Loss of Multiframe Alignment** Set when the framer has lost the multiframe alignment in F12 or F72 format. With the positive transition of bit FRS0.LMFA this bit is set. It is set during alarm simulation.
AIS	3	r	**Alarm Indication Signal (Blue Alarm)** This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of FRS0.AIS.It is set during alarm simulation.
LOS	2	r	**Loss-of-Signal (Red Alarm)** This bit is set when a loss-of-signal alarm is detected in the received data stream and FRS0.LOS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of FRS0.LOS. It is set during alarm simulation.
RAR	1	r	**Remote Alarm Recovery** Set if a remote alarm (yellow alarm) is cleared and bit FRS0.RRA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.
RA	0	r	**Remote Alarm** A remote alarm (yellow alarm) is detected. Set with the rising edge of bit FRS0.RRA. It is set during alarm simulation.

Interrupt Status Register 3

All bits are reset when ISR3 is read. If bit GCR.VIS is set, interrupt status bits in ISR3 are flagged although they are masked by register IMR3. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS. See **Chapter 3.4.4**.

ISR3_T	Offset	Reset Value
Interrupt Status Register 3	$xx6B_H$	00_H

7	6	5	4	3	2	1	0
ES	**SEC**	Res		**LLBSC**	**LTC**	**RSN**	**RSP**
r	r			r	rsc	r	r

Field	Bits	Type	Description
ES	7	r	**Errored Second** This bit is set if at least one enabled interrupt source by ESM is set during the time interval of one second. Interrupt sources of ESM register: • LFA = Loss of frame alignment detected • FER = Framing error received • CER = CRC error received • AIS = Alarm indication signal (blue alarm) • LOS = Loss-of-signal (red alarm) • CVE = Code violation detected • SLIP = Transmit slip or receive slip positive/negative detected
SEC	6	r	**Second Timer** The internal one-second timer has expired. The timer is derived from clock RCLK.
LLBSC	3	r	**Line Loop-Back Status Change/PRBS Status Change** Depending on bit LCR1.EPRM the source of this interrupt status changed:LCR1.EPRM = ´0´: This bit is set, if the LLB activate signal or the LLB deactivate signal is detected over a period of 33,16 ms with a bit error rate less than 10^{-2}. The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 10^{-2}.The actual detection status can be read from the FRS1.LLBAD and FRS1.LLBDD, respectively. PRBS Status ChangeLCR1.EPRM = ´1´: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in FRS1.LLBAD.
LTC	2	rsc	**Loss of Transmit Clock** Transmit clock TCLK has been lost. Transmit clock switching is performed if CMR6.ATCS = ´1´, see **Chapter 3.7.3**. *Note: The actual status of TCLK is shown in the status bit CLKSTAT.TCLKLOS, see **CLKSTAT_T**.*
RSN	1	r	**Receive Slip Negative** The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 1.544 MHz. A frame is skipped. It is set during alarm simulation. See **Chapter 5.1.7**

Field	Bits	Type	Description
RSP	0	r	**Receive Slip Positive** The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 1.544 MHz. A frame is repeated. It is set during alarm simulation. See **Chapter 5.1.7**.

Interrupt Status Register 4

All bits are reset when ISR4 is read. If bit GCR.VIS is set, interrupt status bits in ISR4 are flagged although they are masked by register IMR4. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS. See **Chapter 3.4.4**.

ISR4_T	Offset	Reset Value
Interrupt Status Register 4	$xx6C_H$	00_H

7	6	5	4	3	2	1	0
XSP	**XSN**	**RME2**	**RFS2**	**RDO2**	**ALLS2**	**XDU2**	**RPF2**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
XSP	7	r	**Transmit Slip Positive** The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 1.544 MHz. A frame is repeated. After a slip has performed writing of register XC1 is not necessary.
XSN	6	r	**Transmit Slip Negative** The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 1.544 MHz. A frame is skipped. After a slip has performed writing of register XC1 is not necessary.
RME2	5	r	**Receive Message End - HDLC Channel 2** One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO2, including the status byte.The complete message length can be determined reading register RBC2, the number of bytes currently stored in RFIFO2 is given by RBC2(6:0). Additional information is available in register RSIS2.
RFS2	4	r	**Receive Frame Start - HDLC Channel 2** This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS2 interrupt, the contents of • RAL1 • RSIS2 bits 3 to 1 Are valid and can be read by the external micro controller.

Field	Bits	Type	Description
RDO2	3	r	**Receive Data Overflow - HDLC Channel 2** This interrupt status indicates that the external micro controller did not respond fast enough to an RPF2 or RME2 interrupt and that data in RFIFO2 has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO2 is available again. *Note: Whereas the bit RSIS2.RDO2 in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO2, the ISR4.RDO2 interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.*
ALLS2	2	r	**All Sent - HDLC Channel 2** This bit is set if the last bit of the current frame has been sent completely and XFIFO2 is empty. This bit is valid in HDLC mode only.
XDU2	1	r	**Transmit Data Underrun - HDLC Channel 2** Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO2 and no XME2 was issued. *Note: Transmitter and XFIFO2 are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU2 should not be masked via register IMR4. Additionally, CMDR3.SRES2 must be set after XDU occurs to reset the transmit signaling controller.*
RPF2	0	r	**Receive Pool Full - HDLC Channel 2** 32 bytes of a frame have arrived in the receive FIFO2. The frame is not yet completely received.

Interrupt Status Register 5

All bits are reset when ISR5 is read. If bit GCR.VIS is set, interrupt status bits in ISR5 are flagged although they are masked via register IMR5. However, these masked interrupt statuses neither generate a signal on INT (or INT1, INT2), nor are visible in register GIS. See Chapter 3.4.4.

ISR5_T	Offset	Reset Value
Interrupt Status Register 5	$xx6D_H$	00_H

7	6	5	4	3	2	1	0
XPR2	XPR3	RME3	RFS3	RDO3	ALLS3	XDU3	RPF3
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
XPR2	7	r	**Transmit Pool Ready - HDLC Channel 2** A data block of up to 32 bytes can be written to the transmit FIFO2. XPR2 enables the fastest access to XFIFO2. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.
XPR3	6	r	**Transmit Pool Ready - HDLC Channel 3** A data block of up to 32 bytes can be written to the transmit FIFO3. XPR3 enables the fastest access to XFIFO3. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.
RME3	5	r	**Receive Message End - HDLC Channel 3** One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO3, including the status byte.The complete message length can be determined reading register RBC3, the number of bytes currently stored in RFIFO3 is given by RBC3(6:0). Additional information is available in register RSIS3.
RFS3	4	r	**Receive Frame Start - HDLC Channel 3** This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS2 interrupt, the contents of • RAL1 • RSIS3 bits 3 to 1 Are valid and can be read by the external micro controller.

Field	Bits	Type	Description
RDO3	3	r	**Receive Data Overflow - HDLC Channel 3** This interrupt status indicates that the external micro controller did not respond fast enough to an RPF3 or RME3 interrupt and that data in RFIFO3 has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO3 is available again. *Note: Whereas the bit RSIS3.RDO3 in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO3, the ISR5.RDO3 interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.*
ALLS3	2	r	**All Sent - HDLC Channel 3** This bit is set if the last bit of the current frame has been sent completely and XFIFO3 is empty. This bit is valid in HDLC mode only.
XDU3	1	r	**Transmit Data Underrun - HDLC Channel 3** Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO3 and no XME3 was issued. *Note: Transmitter and XFIFO3 are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU3 should not be masked via register IMR5. Additionally, CMDR4.SRES3 must be set after XDU occurs to reset the transmit signaling controller.*
RPF3	0	r	**Receive Pool Full - HDLC Channel 3** 32 bytes of a frame have arrived in the receive FIFO3. The frame is not yet completely received.

Global Interrupt Status Register

This status register points to pending interrupts sourced by ISR(7:0). See **Chapter 3.4.4**.

GIS_T	Offset	Reset Value
Global Interrupt Status Register	**xx6E$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
ISR7	**ISR6**	**ISR5**	**ISR4**	**ISR3**	**ISR2**	**ISR1**	**ISR0**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
ISR7	7	rsc	**Interrupt Status Register 7Pointer** 0_B , no interrupt is pending in ISR7. 1_B , at least one interrupt is pending in ISR7.
ISR6	6	rsc	**Interrupt Status Register 6 Pointer** 0_B , no interrupt is pending in ISR6. 1_B , at least one interrupt is pending in ISR6.
ISR5	5	rsc	**Interrupt Status Register 5 Pointer** 0_B , no interrupt is pending in ISR5. 1_B , at least one interrupt is pending in ISR5.
ISR4	4	rsc	**Interrupt Status Register 4 Pointer** 0_B , no interrupt is pending in ISR4. 1_B , at least one interrupt is pending in ISR4.
ISR3	3	rsc	**Interrupt Status Register 3 Pointer** 0_B , no interrupt is pending in ISR3. 1_B , at least one interrupt is pending in ISR3.
ISR2	2	rsc	**Interrupt Status Register 2 Pointer** 0_B , no interrupt is pending in ISR2. 1_B , at least one interrupt is pending in ISR2.
ISR1	1	rsc	**Interrupt Status Register 1 Pointer** 0_B , no interrupt is pending in ISR1. 1_B , at least one interrupt is pending in ISR1.
ISR0	0	rsc	**Interrupt Status Register 0 Pointer** 0_B , no interrupt is pending in ISR0. 1_B , at least one interrupt is pending in ISR0.

Channel Interrupt Status Register

This status register points to pending interrupts sourced by channels 1 to 8. See **Chapter 3.4.4**

CIS_T	Offset	Reset Value
Channel Interrupt Status Register	$006F_H$	00_H

7	6	5	4	3	2	1	0
GIS8_PLLLS	GIS7	GIS6	GIS5	GIS4	GIS3	GIS2	GIS1
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
GIS8_PLLLS	7	rsc	**GIS 8: Global Interrupt Status of Channel 8** *Note: Different function of this bit: PLLLS if COMP = ´1´; GIS 8 if COMP = ´0´ , see **Figure 17** and **Figure 18**.* 0_B , no interrupt is pending on channel 8. 1_B , at least one interrupt is pending on channel 8, read GIS of channel 8 for more information. **PLLLS: PLL Lock Status** This bit shows the lock status of the internal PLL. *Note: PLLLS only if COMP = ´1´. PLLLS (for COMP = ´1´) has the same value as PLLLS in register GIS2 (which is used for COMP = ´0´). For both pseudo QuadFALCs (if COMP = ´1´) PLLLS has the same value.* 0_B , PLL is unlocked. 1_B , PLL is locked.
GIS7	6	rsc	**Global Interrupt Status of Channel 7** *Note: Only if COMP = ´0´, see **Figure 18**.* 0_B , no interrupt is pending on channel 7. 1_B , at least one interrupt is pending on channel 7, read GIS of channel 7 for more information.
GIS6	5	rsc	**Global Interrupt Status of Channel 6** *Note: Only if COMP = ´0´, see **Figure 18**.* 0_B , no interrupt is pending on channel 6. 1_B , at least one interrupt is pending on channel 6, read GIS of channel 6 for more information.

Field	Bits	Type	Description
GIS5	4	rsc	**Global Interrupt Status of Channel 5** *Note: Only if COMP = ´0´, see Figure 18.* 0_B , no interrupt is pending on channel 5. 1_B , at least one interrupt is pending on channel 5, read GIS of channel 5 for more information.
GIS4	3	rsc	**Global Interrupt Status of Channel 4** 0_B , no interrupt is pending on channel 4. 1_B , at least one interrupt is pending on channel 4, read GIS of channel 4 for more information.
GIS3	2	rsc	**Global Interrupt Status of Channel 3** 0_B , no interrupt is pending on channel 3. 1_B , at least one interrupt is pending on channel 3, read GIS of channel 3 for more information.
GIS2	1	rsc	**Global Interrupt Status of Channel 2** 0_B , no interrupt is pending on channel 2. 1_B , at least one interrupt is pending on channel 2, read GIS of channel 2 for more information.
GIS1	0	rsc	**Global Interrupt Status of Channel 1** 0_B , no interrupt is pending on channel 1. 1_B , at least one interrupt is pending on channel 1, read GIS of channel 1 for more information.

Receive Signaling Register 1

Each register contains the received bit robbing information for 8 DS0 channels. The received robbed bit signaling information of a complete ESF multiframe is compared to the previously received one. In F12/72 frame format the received signaling information of every 24 frames is compared to the previously received 24 frames. If the contents changed a Receive Signaling Changed interrupt ISR0.RSC is generated and informs the user that a new multiframe has to be read within the next 3 ms. Received data is stored in RS(12:1) registers. The RS1.7 is received in channel 1 frame 1 and RS12.0 in channel 24 frame 24 (ESF). See also **Chapter 5.3.3**.

If requests for reading the RS(12:1) registers are ignored, received data might get lost.

Additionally a receive signaling data change pointer indicates an update of register RS(12:1). Refer also to register RSP(2:1).

Access to RS(12:1) registers is only valid if the serial receive signaling access on the system highway is disabled, see **Chapter 5.3.3.1**.

RS1_T	Offset	Reset Value
Receive Signaling Register 1	$xx70_H$	xx_H

7	6	5	4	3	2	1	0
A1	B1	C1_A2	D1_B2	A2_A3	B2_B3	C2_A4	D2_B4
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
A1	7	r	**CAS Bits**
B1	6		
C1_A2	5		
D1_B2	4		
A2_A3	3		
B2_B3	2		
C2_A4	1		
D2_B4	0		

Similar Registers

Registers RS2 to RS12 have the same description.

The Offset Addresses are listed in **RSn Overview**, for bit names refer to **Receive Signaling Registers (T1/J1)**

Table 135 RSn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
RS2	Receive Signaling Register 2	71_H	
RS3	Receive Signaling Register 3	72_H	
RS4	Receive Signaling Register 4	73_H	
RS5	Receive Signaling Register 5	74_H	
RS6	Receive Signaling Register 6	75_H	
RS7	Receive Signaling Register 7	76_H	
RS8	Receive Signaling Register 8	77_H	

Table 135 RSn Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
RS9	Receive Signaling Register 9	78_H	
RS10	Receive Signaling Register 10	79_H	
RS11	Receive Signaling Register 11	$7A_H$	
RS12	Receive Signaling Register 12	$7B_H$	

Table 136 Receive Signaling Registers (T1/J1)

	7							0
RS1	A1	B1	C1/A2	D1/B2	A2/A3	B2/B3	C2/A4	D2/B4
RS2	A3/A5	B3/B5	C3/A6	D3/B6	A4/A7	B4/B7	C4/A8	D4/B8
RS3	A5/A9	B5/B9	C5/A10	D5/B10	A6/A11	B6/B11	C6/A12	D6/B12
RS4	A7/A13	B7/B13	C7/A14	D7/B14	A8/A15	B8/B15	C8/A16	D8/B16
RS5	A9/A17	B9/B17	C9/A18	D9/B18	A10/A19	B10/B19	C10/A20	D10/B20
RS6	A11/A21	B11/B21	C11/A22	D11/B22	A12/A23	B12/B23	C12/A24	D12/B24
RS7	A13/A1	B13/B1	C13/A2	D13/B2	A14/A3	B14/B3	C14/A4	D14/B4
RS8	A15/A5	B15/B5	C15/A6	D15/B6	A16/A7	B16/B7	C16/A8	D16/B8
RS9	A17/A9	B17/B9	C17/A10	D17/B10	A18/A11	B18/B11	C18/A12	D18/B12
RS10	A19/A13	B19/B13	C19/A14	D19/B14	A20/A15	B20/B15	C20/A16	D20/B16
RS11	A21/A17	B21/B17	C21/A18	D21/B18	A22/A19	B22/B19	C22/A20	D22/B20
RS12	A23/A21	B23/B21	C23/A22	D23/B22	A24/A23	B24/B23	C24/A24	D24/B24

Receive Byte Count Register 2

RBC2_T	Offset	Reset Value
Receive Byte Count Register 2	$xx90_H$	00_H

7	6	5	4	3	2	1	0
OV2	RBC2						
r	r						

Field	Bits	Type	Description
OV2	7	r	**Counter Overflow - HDLC Channel 2** 0_B , Less than or equal to 128 bytes received 1_B , More than 128 bytes received
RBC2	6:0	r	**Receive Byte Count - HDLC Channel 2** Indicates the length of a received frame.

Receive Byte Count Register 3

RBC3_T	Offset	Reset Value
Receive Byte Count Register 3	$xx91_H$	00_H

7	6	5	4	3	2	1	0
OV3	RBC3						
r	r						

Field	Bits	Type	Description
OV3	7	r	**Counter Overflow - HDLC Channel 3** 0_B , Less than or equal to 128 bytes received 1_B , More than 128 bytes received
RBC3	6:0	r	**Receive Byte Count - HDLC Channel 3** Indicates the length of a received frame.

Signaling Status Register 3

SIS3_T	Offset	Reset Value
Signaling Status Register 3	$xx9A_H$	00_H

7	6	5	4	3	2	1	0
XDOV3	**XFW3**	**XREP3**	Res	**RLI3**	**CEC3**	Res	
r	r	r		r	r		

Field	Bits	Type	Description
XDOV3	7	r	**Transmit Data Overflow - HDLC Channel 3** More than 32 bytes (if CCR4.RFT23 = ´0´) or 64 bytes (if CCR4.RFT23 = ´1´)have been written to the XFIFO3.This bit is cleared either • By a transmitter reset command XRES or • When all bytes in the accessible half of the XFIFO3 have been moved in the inaccessible half (shadow register). 0_B , normal FIFO operation. 1_B , number of bytes written to the FIFO exceeds the FIFO size.
XFW3	6	r	**Transmit FIFO Write Enable - HDLC Channel 3** Data can be written to the XFIFO3.
XREP3	5	r	**Transmission Repeat - HDLC Channel 3** Status indication of CMDR3.XREP3.
RLI3	3	r	**Receive Line Inactive - HDLC Channel 3** Neither flags as interframe time fill nor frames are received via the signaling time slot.
CEC3	2	r	**Command Executing - HDLC Channel 3** *Note: CEC3 will be active at most 2.5 periods of the current system data rate.* 0_B , No command is currently executed, the CMDR4 register can be written to. 1_B , A command (written previously to CMDR4) is currently executed, no further command can be temporarily written in CMDR4 register.

Receive Signaling Status Register 3

RSIS3 relates to the last received HDLC channel 3 frame; it is copied into RFIFO3 when end-of-frame is recognized (last byte of each stored frame).

RSIS3_T	Offset	Reset Value
Receive Signaling Status Register 3	$xx9B_H$	00_H

7	6	5	4	3	2	1	0
VFR3	**RDO3**	**CRC163**	**RAB3**	**HA13**	**HA03**	Res	**LA3**
rsc	rsc	rsc	rsc	rsc	rsc		rsc

Field	Bits	Type	Description
VFR3	7	rsc	**Valid Frame - HDLC Channel 3** Determines whether a valid frame has been received. An invalid frame is either • A frame which is not an integer number of 8 bits (nx8 bits) in length (e.g. 25 bits), or • A frame which is too short taking into account the operation mode selected via MODE3 (MDS3(2:0)) and the selection of receive CRC ON/OFF (CCR4.RCRC3) as follows: MDS3(2:0) = ´011_b´ (16-bit Address), RCRC3=´0´: 4 bytes; RCRC3 = ´1´: 3 or 4 bytes or MDS3(2:0) = ´010_b´ (8-bit Address), RCRC3 = ´0´: 3 bytes; RCRC3=1: 2 or 3 bytes *Note: Shorter frames are not reported.* 0_B , Received frame is invalid 1_B , Received frame is valid
RDO3	6	rsc	**Receive Data Overflow - HDLC Channel 3** A data overflow has occurred during reception of the frame.Additionally, an interrupt can be generated (refer to ISR5.RDO3/IMR5.RDO3). 0_B , normal receive operation. 1_B , data overflow has occurred during reception.
CRC163	5	rsc	**CRC16 Compare/Check - HDLC Channel 3** 0_B , CRC check failed; received frame contains errors. 1_B , CRC check o.k.; received frame is error-free.
RAB3	4	rsc	**Receive Message Aborted - HDLC Channel 3** This bit is set, if more than 5 contiguous ´1´-bits are detected. 0_B , data reception is in progress. 1_B , data reception has been aborted.

Field	Bits	Type	Description
HA13	3	rsc	**High Byte Address Compare - HDLC Channel 3** Significant only if 2-byte address mode is selected.In operating modes which provide high byte address recognition, the OctalFALCTM compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values ´FE_H´ and ´FC_H´ (broadcast address). Depending on the result of this comparison, the following bit combinations are possible: *Note: If RAH1, RAH2 contain identical values, a match is indicated by "10" or "11".* 00_B , RAH2 has been recognized 01_B , Broadcast address has been recognized 10_B , RAH1 has been recognized C/R = ´0´ (bit 1) 11_B , RAH1 has been recognized C/R = ´1´ (bit 1)
HA03	2		
LA3	0	rsc	**Low Byte Address Compare - HDLC Channel 3** Significant in HDLC modes only. The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2). 0_B , RAL2 has been recognized 1_B , RAL1 has been recognized

Receive FIFO 2 Lower Byte

RFIFO2L_T	Offset	Reset Value
Receive FIFO 2 Lower Byte	$xx9C_H$	xx_H

7	6	5	4	3	2	1	0
RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF7	7	r	**Receive FIFO - HDLC Channel 2** The function is equivalent to RFIFO1L of HDLC channel 1.
RF6	6	r	
RF5	5	r	
RF4	4	r	
RF3	3	r	
RF2	2	r	
RF1	1	r	
RF0	0	r	

Receive FIFO 2 Higher Byte

RFIFO2H_T	Offset	Reset Value
Receive FIFO 2 Higher Byte	$xx9D_H$	xx_H

7	6	5	4	3	2	1	0
RF15	**RF14**	**RF13**	**RF12**	**RF11**	**RF10**	**RF9**	**RF8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF15	7	r	**Receive FIFO - HDLC Channel 2** The function is equivalent to RFIFO1H of HDLC channel 1.
RF14	6	r	
RF13	5	r	
RF12	4	r	
RF11	3	r	
RF10	2	r	
RF9	1	r	
RF8	0	r	

Receive FIFO 3 Lower Byte

RFIFO3L_T	Offset	Reset Value
Receive FIFO 3 Lower Byte	$xx9E_H$	xx_H

7	6	5	4	3	2	1	0
RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF7	7	r	**Receive FIFO - HDLC Channel 3** The function is equivalent to RFIFO1L of HDLC channel 1.
RF6	6	r	
RF5	5	r	
RF4	4	r	
RF3	3	r	
RF2	2	r	
RF1	1	r	
RF0	0	r	

Receive FIFO 3 Higher Byte

RFIFO3H_T	Offset	Reset Value
Receive FIFO 3 Higher Byte	$xx9F_H$	xx_H

7	6	5	4	3	2	1	0
RF15	**RF14**	**RF13**	**RF12**	**RF11**	**RF10**	**RF9**	**RF8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RF15	7	r	**Receive FIFO - HDLC Channel 3** The function is equivalent to RFIFO1H of HDLC channel 1.
RF14	6	r	
RF13	5	r	
RF12	4	r	
RF11	3	r	
RF10	2	r	
RF9	1	r	
RF8	0	r	

Signaling Status Register 2

SIS2_T	Offset	Reset Value
Signaling Status Register 2	xxA9$_H$	00$_H$

7	6	5	4	3	2	1	0
XDOV2	**XFW2**	**XREP2**	Res	**RLI2**	**CEC2**	Res	
rsc	rsc	rsc		rsc	rsc		

Field	Bits	Type	Description
XDOV2	7	rsc	**Transmit Data Overflow - HDLC Channel 2** More than 32 bytes (if CCR3.RFT22 = ´0´) or 64 bytes (if CCR3.RFT22 = ´1´) have been written to the XFIFO, see **Chapter 3.4.3**.This bit is cleared either • By a transmitter reset command XRES or • When all bytes in the accessible half of the XFIFO have been moved in the inaccessible half (shadow register). 1_B , normal FIFO operation. 0_B , number of bytes written to the FIFO exceeds the FIFO size.
XFW2	6	rsc	**Transmit FIFO Write Enable - HDLC Channel 2** 0_B , FIFO is not ready, don’t write to FIFO. 1_B , FIFO is ready to accept data.
XREP2	5	rsc	**Transmission Repeat - HDLC Channel 2** 0_B , no repeated transmission in progress. 1_B , repeated transmission is in progress.
RLI2	3	rsc	**Receive Line Inactive - HDLC Channel 2** 0_B , HDLC data or interframe time fill are being received. 1_B , neither data nor flags as interframe time fill are received.
CEC2	2	rsc	**Command Executing - HDLC Channel 2** *Note: CEC2 will be high for about 2.5 periods of the system data rate after a command has been written to CMDR3.* 0_B , no command is currently executing, CMDR3 can be written. 1_B , a command is in progress, don’t write to CMDR3.

Receive Signaling Status Register 2

RSIS2_T	Offset	Reset Value
Receive Signaling Status Register 2	$xxAA_H$	00_H

7	6	5	4	3	2	1	0
VFR2	**RDO2**	**CRC162**	**RAB2**	**HA2**		Res	**LA2**
rsc	rsc	rsc	rsc	rsc			rsc

Field	Bits	Type	Description
VFR2	7	rsc	**Valid Frame - HDLC Channel 2** Indicates whether a valid frame has been received. An invalid frame is flagged if - the frame length is not an integer multiple of 8 bytes - the frame is too short (the lower limit depends on the selection of MODE2.MDS2 and CCR3.RCRC2). 1_B , received frame is invalid. 0_B , received frame is valid.
RDO2	6	rsc	**Receive Data Overflow - HDLC Channel 2** 0_B , normal receive operation. 1_B , data overflow has occurred during reception.
CRC162	5	rsc	**CRC16 Compare/Check - HDLC Channel 2** 0_B , CRC error check failed on the received frame. 1_B , received frame if free of CRC errors.
RAB2	4	rsc	**Receive Message Aborted- HDLC Channel 2** Message abortion is declared, if more than five contiguous “1” bits are received. 0_B , data reception is in progress. 1_B , data reception has been aborted.
HA2	3:2	rsc	**High Byte Address Compare - HDLC Channel 2** These bits are used in two-byte addressing mode only. In addressing modes using high byte recognition, the high byte of the received address is compared with two individually programmable registers (RAH1 and RAH2) as well as with the fixed values FEH and FCH (broadcast address). *Note: If RAH1 and RAH2 are set to identical values, a match is indicated by either “10” or “11”.* 00_B , RAH2 has been recognized. 01_B , broadcast address has been recognized. 10_B , RAH1 has been recognized, C/R = ´0´. 11_B , RAH1 has been recognized, C/R = ´1´.

Field	Bits	Type	Description
LA2	0	rsc	**Low Byte Address Compare - HDLC Channel 2** This bit is used in HDLC modes only. The low byte address of a two-byte address or a single-byte address are compared with two programmable values (RAL1 and RAL2). 1_B , received low address byte matches the value programmed to RAL2. 0_B , received low address byte matches the value programmed to RAL1.

Multi Function Port Input Register

This register always reflects the state of the multi function ports. If used as an input, the according port should be switched to general purpose input mode. If not, the programmed output signal can be monitored through this register. See registers **PC1_T** to PC4_T and **Chapter 3.8**.

MFPI_T	Offset	Reset Value
Multi Function Port Input Register	**$xxAB_H$**	**xx_H**

7	6	5	4	3	2	1	0
Res	**RPC**	**RPB**	**RPA**	Res		**XPB**	**XPA**
	r	r	r			r	r

Field	Bits	Type	Description
RPC	6	r	**RPC Input Level** 0_B , Low level on pin RPC. 1_B , High level on pin RPC.
RPB	5	r	**RPB Input Level** 0_B , Low level on pin RPB. 1_B , High level on pin RPB.
RPA	4	r	**RPA Input Level** 0_B , Low level on pin RPA. 1_B , High level on pin RPA.
XPB	1	r	**XPB Input Level** 0_B , Low level on pin XPB. 1_B , High level on pin XPB.
XPA	0	r	**XPA Input Level** 0_B , Low level on pin XPA. 1_B , High level on pin XPA.

Interrupt Status Register 6

Note that detection of Out-Band Loop messages (BOM codes) is only possible either on the line side or the system side, dependent on the configuration of the HDLC/BOM controller 1: If the HDLC/BOM controller 1 is attached to the line side (MODE.HDLCI = ´0´) only BOM messages on the line side can be detected. If the HDLC/BOM controller 1 is attached to the system side (MODE.HDLCI = ´1´) only BOM messages on the system side can be detected. See **Chapter 5.5.7** and **Chapter 5.5.8**.

A detection of an Out-Band loop message (BOM) “universal loopback deactivate” sets both bits SOLSD and LOLSD, independent if a loop is active (switched) or not.

ISR6_T	Offset	Reset Value
Interrupt Status Register 6	$xxAC_H$	00_H

7	6	5	4	3	2	1	0
SOLSU	SOLSD	LOLSU	LOLSD	SILSU	SILSD	LILSU	LILSD
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
SOLSU	7	rsc	**System Out-Band Loop Switching Up detected** See **Chapter 5.5.8**. System loop up code (payload loopback activate message) detected and payload loop is switched on if ALS.SOLS is set.
SOLSD	6	rsc	**System Out-Band Loop Switching Down detected** See **Chapter 5.5.8**. System loop down code (payload loopback deactivate message) detected and payload loop is switched off if ALS.SOLS is set.
LOLSU	5	rsc	**Line Out-Band Loop Switching Up detected** See **Chapter 5.5.8**. Line loop up code (line loopback activate message) detected and line loop is switched on if ALS.LOLS is set.
LOLSD	4	rsc	**Line Out-Band Loop Switching Down detected** See **Chapter 5.5.8**. Line loop down code (line loopback deactivate message) detected and line loop is switched off if ALS.LOLS is set.
SILSU	3	rsc	**System In-Band Loop Switching Up detected** See **Chapter 5.5.7**. System loop up code detected and payload loop is switched on if ALS.SILS is set.
SILSD	2	rsc	**System In-Band Loop Switching Down detected** See **Chapter 5.5.7**. System loop down code detected and payload loop is switched off if ALS.SILS is set.
LILSU	1	rsc	**Line In-Band Loop Switching Up Interrupt** See **Chapter 5.5.7**. Line loop up code detected and line loop is switched on if ALS.LILS is set.

Field	Bits	Type	Description
LILSD	0	rsc	**Line In-Band Loop Switching Down Interrupt** See **Chapter 5.5.7**. Line loop down code detected and line loop is switched off if ALS.LILS is set.

Global Interrupt Status 2

GIS2_T	Offset	Reset Value
Global Interrupt Status 2	$00AD_H$	00_H

7	6	5	4	3	2	1	0
Res					PLLIC	PLLLS	PLLLC
					rsc	r	rsc

Field	Bits	Type	Description
PLLLS	1	r	**PLL Locked Status Information** *Note: PLLLS is only a status bit, not an interrupt status bit, so type is r and not rsc. This bit is valid independent on value of COMP. For COMP = ´0´ this bit must be used instead of bit 7 of register CIS which has then the function GIS8.* 0_B , PLL is unlocked. 1_B , PLL is locked
PLLLC	0	rsc	**PLL Locked Status Change** 0_B , no change of PLL lock status since last read of this register. 1_B , PLL lock status has changed since last read. Status information is available in bit PLLLS.

PPR Data 0

This register contains the first PPR byte of time t0. For a detailed description see chapter “Periodical Performance Report in ESF Format (T1/J1)”. See **Chapter 5.3.7**.

PPR0_T	Offset	Reset Value
PPR Data 0	$xxD1_H$	$0x_H$

7	6	5	4	3	2	1	0
G3_T0	**LV_T0**	**G4_T0**	**U1_T0**	**U2_T0**	**G5_T0**	**SL_T0**	**G6_T0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
G3_T0	7	r	**G3_T0 bit**
LV_T0	6	r	**LV_T0 bit**
G4_T0	5	r	**G4_T0 bit**
U1_T0	4	r	**U1_T0 bit**
U2_T0	3	r	**U2_To bit**
G5_T0	2	r	**G5_T0 bit**
SL_T0	1	r	**SL_T0 bit**
G6_T0	0	r	**G6_T0 bit**

PPR Data 1

PPR1_T	Offset	Reset Value
PPR Data 1	$xxD2_H$	$0x_H$

7	6	5	4	3	2	1	0
FE_T0	**SE_T0**	**LB_T0**	**G1_T0**	**R_T0**	**G2_T0**	**NM_T0**	**N1_T0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FE_T0	7	r	**FE_T0 bit**
SE_T0	6	r	**SE_T0 bit**
LB_T0	5	r	**LB_T0-bit**
G1_T0	4	r	**G1_T0 bit**
R_T0	3	r	**R_T0 bit**
G2_T0	2	r	**G2_T0 bit**
NM_T0	1	r	**NM_To bit**
N1_T0	0	r	**N1_T0 bit**

Interrupt Status Register 7

Masked by register IMR7.

ISR7_T	Offset	Reset Value
Interrupt Status Register 7	**$xxD8_H$**	**00_H**

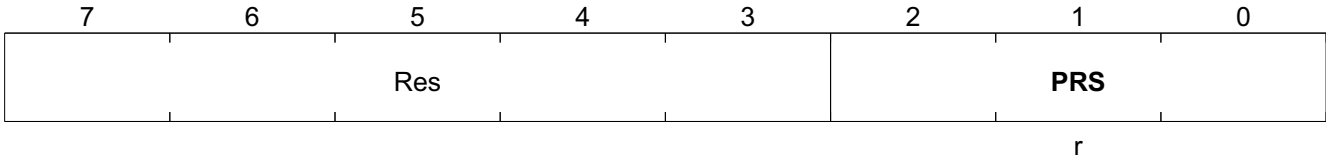
7	6	5	4	3	2	1	0
Res			**XCLKSS1**	**XCLKSS0**	Res		**SEFEI**
			rsc	rsc			rsc

Field	Bits	Type	Description
XCLKSS1	4	rsc	**XCLK Source Switched 1** See **Chapter 3.7.3**. Shows if an automatically switching of the DCO-X reference between TCLK and SCLK was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in register **CLKSTAT_T**.
XCLKSS0	3	rsc	**XCLK Source Switched 0** See **Chapter 3.7.3**. Shows if an automatically switching of the XCLK source between TCLK and DCO-X output was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in register **CLKSTAT_T**.
SEFEI	0	rsc	**SEF Error Interrupt** Shows if a SEF error was detected. See **Chapter 5.5.1.1**.

PRBS Status Register

See **Chapter 5.7.1**.

PRBSSTA_T	Offset	Reset Value
PRBS Status Register	$xxDA_H$	$0x_H$



Field	Bits	Type	Description
PRS	2:0	r	**PRBS Status Information** *Note: Every change of the bits PRS sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected in case alarm simulation is performed by the device. Detection of all_zero or all_ones is done over 12, 16, 21 or 24 consecutive bits, dependent on the choosed PRBS polynomial (11, 15, 20 or 23). Because every bit error in the PRBS increments the bit error counter BEC, no special status information like “PRBS detected with errors” is given here.* 000_B , no pattern detected. 001_B , reserved. 010_B , PRBS pattern detected. 011_B , inverted PRBS pattern detected. 100_B , reserved. 101_B , reserved. 110_B , all-zero pattern detected. 111_B , all-ones pattern detected.

Device Status Register

DSTR_T	Offset	Reset Value
Device Status Register	$00E7_H$	$0x_H$

7	6	5	4	3	2	1	0
Res						QFN	COMP
						r	r

Field	Bits	Type	Description
QFN	1	r	**QuadFALC® Number** *Note: See **Figure 96** for more detail. This bit is valid only if COMP = ´1´.* 0_B , A10/CS2 is low (QuadFALC® #0 has been selected). 1_B , QuadFALC® #1 has been selected.
COMP	0	r	**COMP Input Signal Status** *Note: See **Figure 96** for more detail.* 0_B , COMP input signal is low, OctalFALCTM mode is selected. 1_B , COMP input signal is high, QuadFALC® compatibility mode is selected.

Clock Status Register

The bits show the current status of the input clocks TCLK and SCLKX.

CLKSTAT_T	Offset	Reset Value
Clock Status Register	$xxFE_H$	xx_H

7	6	5	4	3	2	1	0
Res			TCLKLOS	SCLKXLOS	Res		
			r	r			

Field	Bits	Type	Description
TCLKLOS	4	r	**Loss of TCLK** Status of TCLK. *Note: See **Chapter 3.7.3** for more detail.* 0_B , TCLK is active. 1_B , TCLK is lost.
SCLKXLOS	3	r	**Loss of SCLKX** Status of SCLKX. *Note: See **Chapter 3.7.3** for more detail.* 0_B , SCLKX is active. 1_B , SCLKX is lost.

9 Package Outlines

Figure 97 shows the package outline for the RoHS compliant (PG-LBGA-256) and the non-RoHS compliant (P-LBGA-256) package.

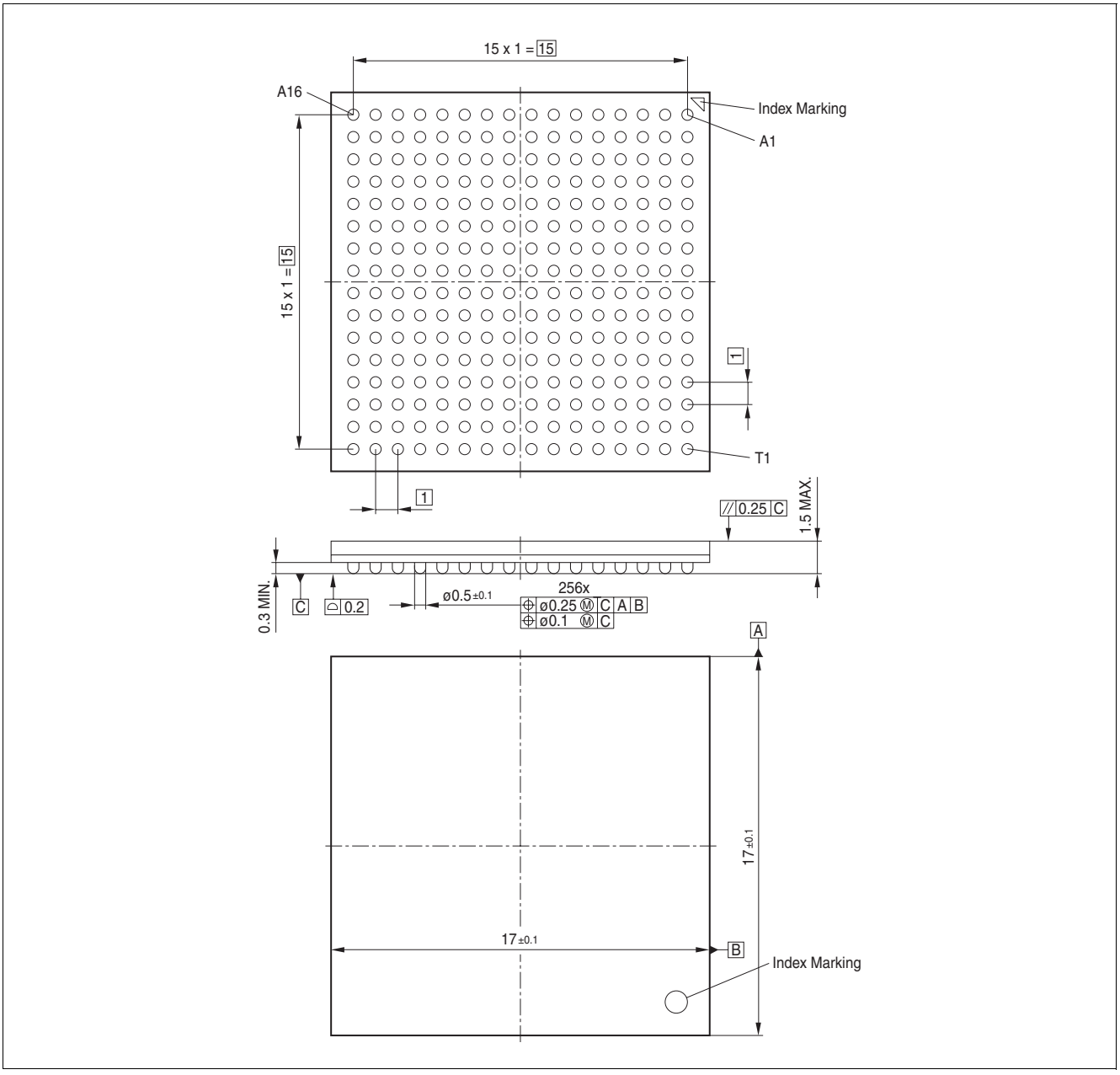


Figure 97 P-LBGA-256 (Plastic Low Profile Ball Grid Array Package), SMD

Note: The upper drawing shows the "Bottom View" of the package.

Dimensions in mm

10 Electrical Characteristics

In Table 137 the absolute maximum ratings of the OctalFALC™ are listed.

Table 137 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Ambient temperature under bias	T_A	-40	–	85	°C	–
Storage temperature	T_{stg}	-65	–	125	°C	–
Moisture Level 3 temperature	T_{ML3}	–	–	225	°C	According to IPS J-STD 020
				245	°C	According to Infineon internal standard
IC supply voltage (pads, digital)	V_{DD}	-0.5	3.3	4.5	V	–
IC supply voltage (core, digital)	V_{DDC}	-0.5	1.8	2.4	V	–
IC supply voltage receive (analog)	V_{DDR}	-0.4	–	4.5	V	–
IC supply voltage transmit (analog)	V_{DDX}	-0.4	–	4.5	V	–
Receiver input signal with respect to ground	V_{RLmax}	-0.8	–	4.5	V	RL1, RL2
Voltage on any pin with respect to ground	V_{max}	-0.4	–	4.5	V	Except RL1, RL2
ESD robustness[1] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	–	–	2000	V	[2]
ESD robustness[3] CDM	$V_{ESD,CDM}$	–	–	500		–

1) According to JEDEC standard JESD22-A114.

2) For RL1 and RL2 1500 V

3) According to ESD Association Standard DS5.3.1 - 1999

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 138 defines the maximum values of voltages and temperature which may be applied to guarantee proper operation of the OctalFALC™.

Table 138 Operating Range

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_A	-40	–	85	°C	–
Supply voltage digital pads	V_{DD}	3.13	3.30	3.46	V	3.3 V ±5 % [1]
Supply voltage digital core	V_{DDC}	1.62	1.80	1.98	V	1.8 V ±10 % [2]

Table 138 Operating Range (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Supply voltage analog receiver	V_{DDR}	3.13	3.30	3.46	V	3.3 V ±5 % 3)
Supply voltage analog transmitter	V_{DDX}	3.13	3.30	3.46	V	3.3 V ±5 % 4)
Analog input voltages	V_{RL}	0	–	V_{DDR} +0.3	V	RL1, RL2
Digital input voltages	V_{ID}	-0.4	–	3.46	V	V_{DD} = 3.3 V ±5 %
Ground	V_{SS} V_{SSR} V_{SSX}	0	–	0	V	–

1) Voltage ripple on analog supply less than 50 mV
2) Voltage ripple on analog supply less than 50 mV
3) Voltage ripple on analog supply less than 50 mV
4) Voltage ripple on analog supply less than 50 mV

Note: In the operating range, the functions given in the circuit description are fulfilled.
V_{DD}, V_{DDR} and V_{DDX} have to be connected to the same voltage level,
V_{SS}, V_{SSR} and V_{SSX} have to be connected to ground level.

Table 139 DC Characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input low voltage	V_{IL}	-0.4	–	0.8	V	1)
Input high voltage	V_{IH}	2.0	–	3.46	V	1)
Output low voltage	V_{OL}	V_{SS}	–	0.45	V	I_{OL} = +2 mA 2)
Output high voltage	V_{OH}	2.4	–	V_{DD}	V	I_{OH} = -2 mA 2)
Average power supply current at 1.8 V supply (analog line interface mode)	I_{DD18E1}	–	–	350	mA	E1 application 3) LIM1.DRS = ´0´, all-one´s pattern; 16 MHz at system interface
	I_{DD18E1}	–	–	300		E1 application 4) LIM1.DRS = ´0´, PRBS pattern; 2 MHz at system interface
	I_{DD18T1}	–	–	300		T1 application 5) LIM1.DRS = ´0´, all-one´s pattern; 12 MHz at system interface
	I_{DD18T1}	–	–	250		T1 application 6) LIM1.DRS = ´0´, PRBS pattern; 1.5 MHz at system interface

Table 139 DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Average power supply current at 3.3 V supply (analog line interface mode)	I_{DD33E1}	–	–	410	mA	E1 application [7] LIM1.DRS = ´0´, all-one´s pattern; 16 MHz at system interface
	I_{DD33E1}	–	–	370		E1 application [8] LIM1.DRS = ´0´, PRBS pattern; 2 MHz at system interface
	I_{DD33T1}	–	–	410		T1 application[9] LIM1.DRS = ´0´, all-one´s pattern; 12 MHz at system interface
	I_{DD33T1}	–	–	370		T1 application [10] LIM1.DRS = ´0´, PRBS pattern; 1.5 MHz at system interface
Average power supply current at 1.8 V supply (digital line interface mode)	I_{DD18E1}	–	–	350	mA	E1 application [11] LIM1.DRS = ´1´, PRBS pattern; 16 MHz at system interface
Average power supply current at 3.3 V supply (digital line interface mode)	I_{DD33T1}	–	–	25	mA	
Input leakage current	I_{IL11}	–	–	1	µA	$V_{IN} = V_{DD}$ [12]; all except RDO
Input leakage current	I_{IL12}	–	–	1	µA	$V_{IN} = V_{SS}$ [6]; all except RDO
Input pullup current	I_{IP}	2	–	15	µA	$V_{IN} = V_{SS}$
Output leakage current	I_{OZ1}	–	–	1	µA	V_{OUT} = tristate[1] $V_{SS} < V_{meas} < V_{DD}$ measured against V_{DD} and V_{SS}; all except XL1/2
Transmitter leakage current	I_{TL}	–	–	30	µA	XL1/2 = V_{DDX}; XPM2.XLT = ´1´
		–	–	30		XL1/2 = V_{SSX}; XPM2.XLT = ´1´
Transmitter output impedance	R_X	–	–	3	Ω	Applies to XL1and XL2[13]
Transmitter output current	I_X	–	–	105	mA	XL1, XL2
Differential peak voltage of a mark (between XL1 and XL2)	V_X	–	–	2.15	V	–

Table 139 DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Receiver peak voltage of a mark (at RL1 or RL2)	V_{RL12}	-0.45	–	3.8	V	RL1, RL2
		-0.75	–	4.1		RZ signals; must only be applied during T1 pulse over/undershoot according to ANSI T1.403-1999
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_{RL12}	–	–	4.0	V	RL1, RL2
				4.63	V	RZ signals; must only be applied during T1 pulse over/undershoot according to ANSI T1.403-1999
Receiver input impedance	Z_R	–	50	–	kΩ	13)
Receiver sensitivity	S_{RSH}	0	–	10	dB	RL1, RL2 LIM0.EQON = ´0´ (short-haul)
Receiver sensitivity	S_{RLH}	-43	–	0	dB	RL1, RL2 LIM0.EQON = ´1´ (E1, long-haul)
		-36	–	0		RL1, RL2 LIM0.EQON = ´1´ (T1/J1, long-haul)
Receiver input threshold	V_{RTH}	–	45	–	%	LIM2.SLT(1:0) = ´11_b´ 13)
		–	50	–		LIM2.SLT(1:0) = ´10_b´ 13) default setting
		–	55	–		LIM2.SLT(1:0) = ´00_b´ 13)
		–	67	–		LIM2.SLT(1:0) = ´01_b´ 13)
Loss-Of-signal (LOS) detection limit	V_{LOS}	1560	–	1710	mV	RIL(2:0) = ´000_b´ 13)
		790	–	960		RIL(2:0) = ´001_b´ 13)
		430	–	500		RIL(2:0) = ´010_b´14)
		220	–	260		RIL(2:0) = ´011_b´ 13)
		125	–	130		RIL(2:0) = ´100_b´ 13)
		65	–	70		RIL(2:0) = ´101_b´ 13)
		35	–	40		RIL(2:0) = ´110_b´ 13)
		10	–	15		RIL(2:0) = ´111_b´ 13)

1) Applies to all input pins except analog pins RLx

2) Applies to all output pins except pins XLx

3) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 163**.

4) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 163**.

5) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 164**.

6) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 163**.
7) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 163**.
8) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 163**.
9) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 164**.
10) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 163**.
11) Wiring conditions and external circuit configuration according to **Figure 125** and **Table 163**.
12) Pin leakage is measured in a test mode with all internal pullups disabled. RDO pins are not tristatable, no leakage is measured.
13) Parameter not tested in production
14) Value measured in production to fulfil ITU-T G.775

Note: Typical characteristics specify mean values expected over the production spread. If not specified otherwise, typical characteristics apply at T_A = 25 °C and 3.3 V supply voltage.

10.1 AC Characteristics

10.1.1 Master Clock Timing

Figure 98 shows the timing and **Table 140** the appropriate timing parameter values of the master clock at the pin MCLK. The accuracy is required to fulfill the jitter requirements, see **Chapter 3.4.6**, **Chapter 3.6.5** and **Chapter 3.7.4**.

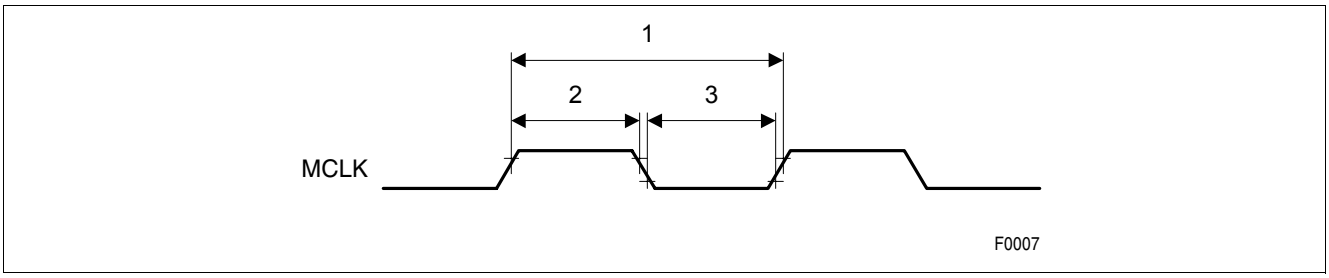


Figure 98 MCLK Timing

Table 140 MCLK Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Clock period of MCLK	1	–	488	–	ns	E1, fixed mode
		–	648	–		T1/J1, fixed mode
		50	–	980.4		E1/T1/J1, flexible mode
High phase of MCLK	2	40	–	–	%	–
Low phase of MCLK	3	40	–	–	%	–
Clock accuracy	–	32[1)]	–	28[2)]	ppm	–

1) If clock divider programming fits without rounding

2) If clock divider programming requires rounding

10.1.2 JTAG Boundary Scan Interface

Figure 99 shows the timing and **Table 141** the appropriate timing parameter values at the JTAG pins to perform a boundary scan test of the OctalFALC™, see **Chapter 3.6.4**.

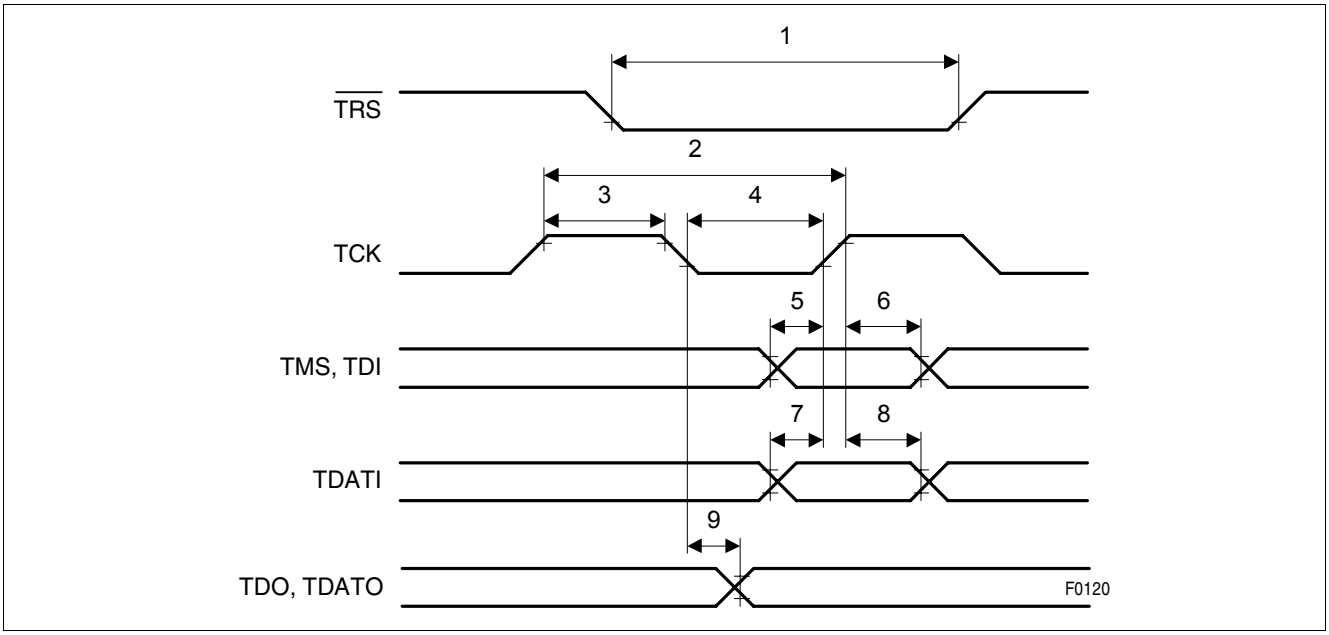


Figure 99 JTAG Boundary Scan Timing

Table 141 JTAG Boundary Scan Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
$\overline{TRS}$ reset active low time	1	200	–	–	ns	–
TCK period	2	250	–	–	ns	–
TCK high time	3	80	–	–	ns	–
TCK low time	4	80	–	–	ns	–
TMS, TDI setup time	5	40	–	–	ns	–
TMS, TDI hold time	6	40	–	–	ns	–
TDATI setup time	7	40	–	–	ns	–
TDATI hold time	8	40	–	–	ns	–
TDO, TDATO output delay	9	-	–	100	ns	–

10.1.3 Reset

Figure 100 shows the timing and **Table 142** the appropriate timing parameter value at the pin $\overline{RES}$ to perform a reset of the OctalFALC™.

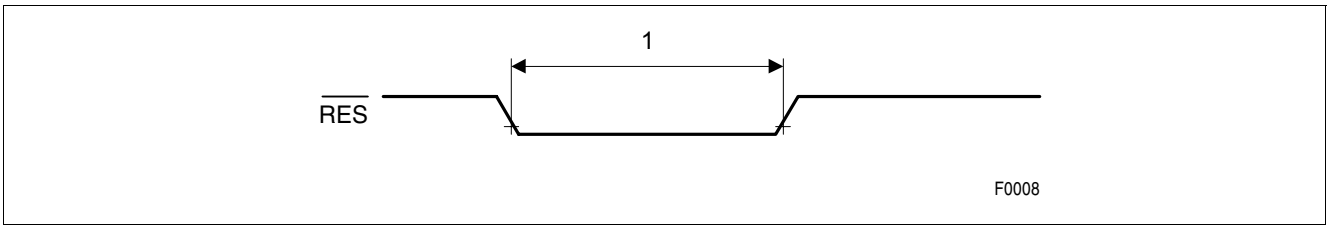


Figure 100 Reset Timing

Table 142 Reset Timing Parameter Value

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
$\overline{RES}$ pulse width low	1	10[1)]	–	–	µs	–

1) While MCLK is running

10.1.4 Asynchronous Microprocessor Interface

10.1.4.1 Intel Bus Interface Mode

Figure 101 to **Figure 104** show the timing of the SCI Interface and **Table 143** the appropriate timing parameter values.

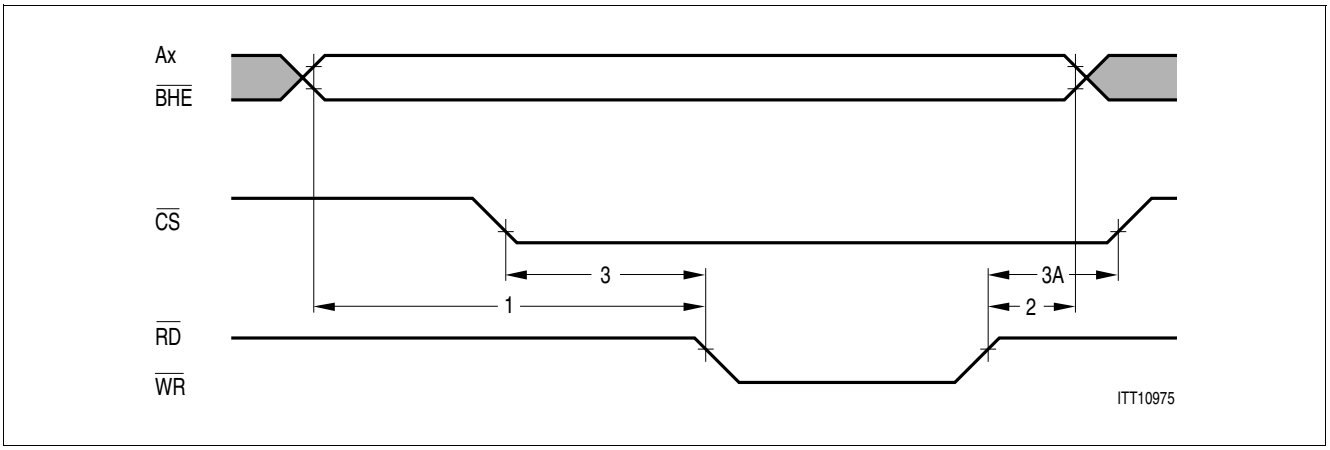


Figure 101 Intel Non-Multiplexed Address Timing

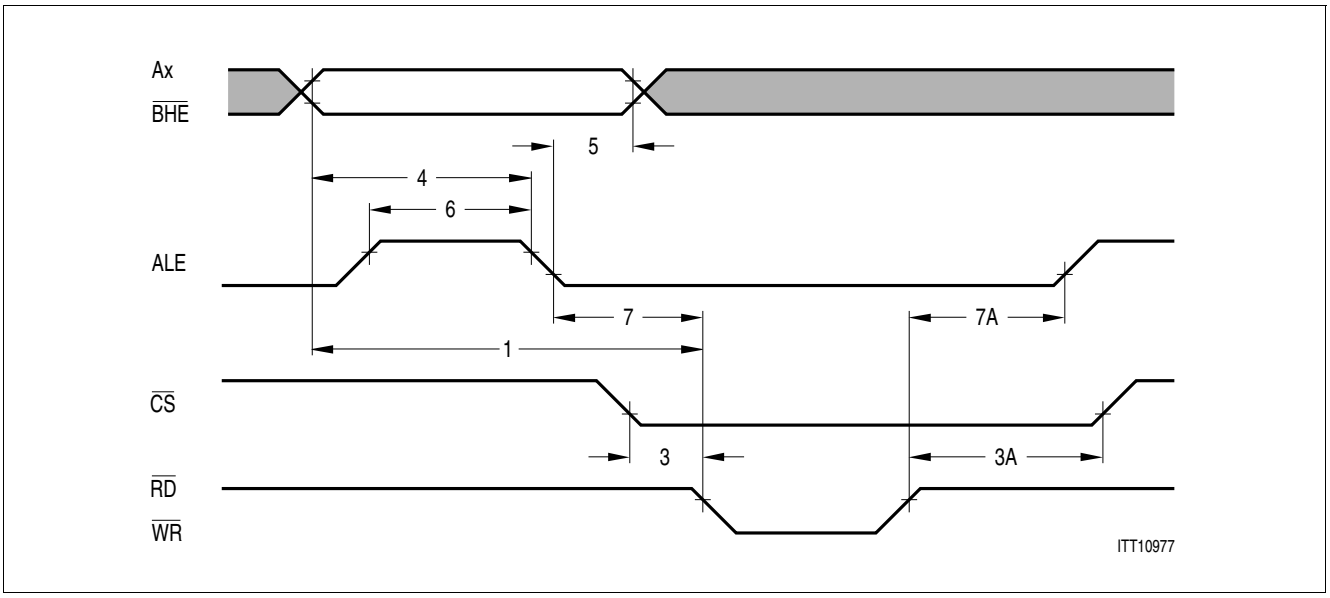


Figure 102 Intel Multiplexed Address Timing

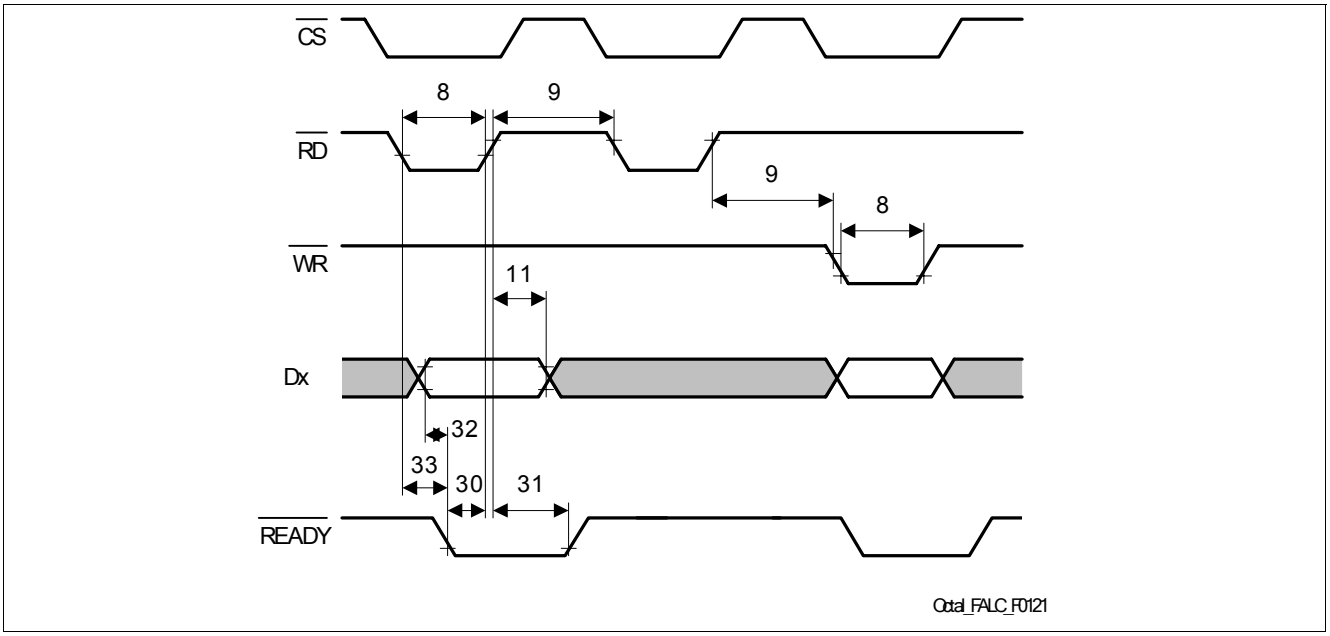


Figure 103 Intel Read Cycle Timing

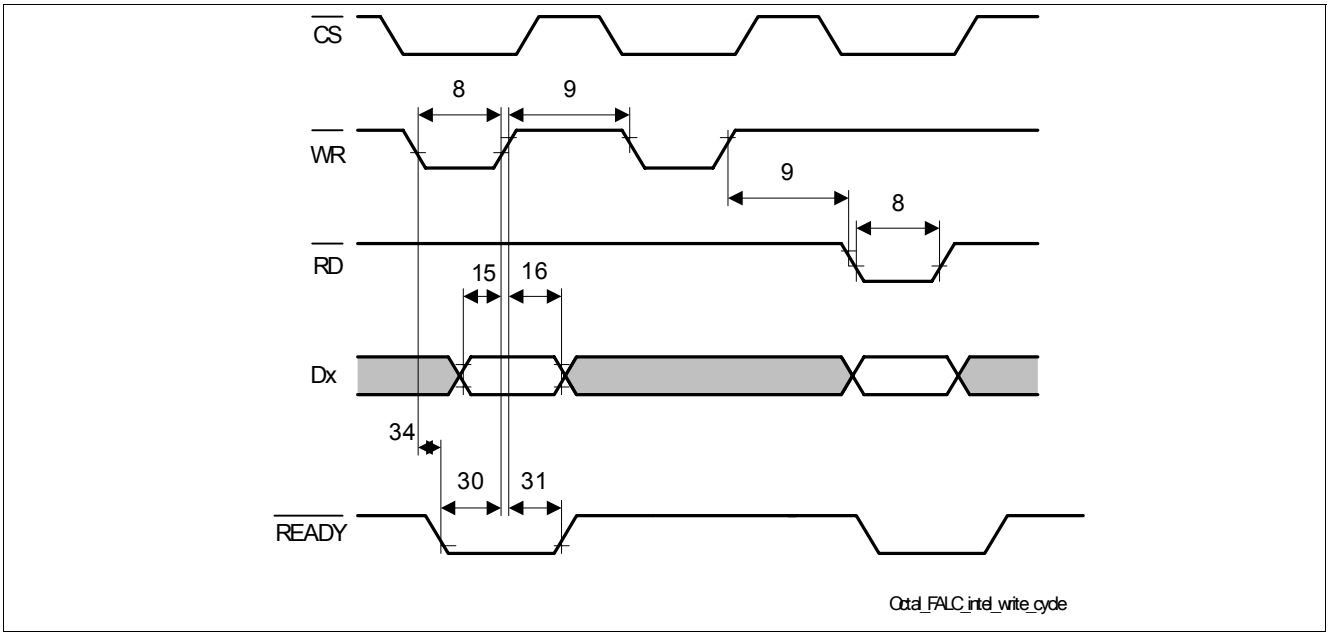


Figure 104 Intel Write Cycle Timing

Table 143 Intel Bus Interface Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Address, $\overline{BHE}$ setup time	1	5	–	–	ns	–
Address, $\overline{BHE}$ hold time	2	0	–	–	ns	–
$\overline{CS}$ setup time	3	0	–	–	ns	–
$\overline{CS}$ hold time	3A	0	–	–	ns	–
Address, $\overline{BHE}$ stable before ALE inactive	4	10	–	–	ns	–

Table 143 Intel Bus Interface Timing Parameter Values (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Address, $\overline{BHE}$ hold after ALE inactive	5	10	–	–	ns	–
ALE pulse width	6	30	–	–	ns	–
ALE setup time before $\overline{RD}$ or $\overline{WR}$	7	0	–	–	ns	–
ALE hold time after $\overline{RD}$ or $\overline{WR}$	7A	30	–	–	ns	–
$\overline{RD}$, $\overline{WR}$ pulse width	8	80	–	–	ns	–
RD, WR control interval	9	70	–	–	ns	–
Data hold after $\overline{RD}$ inactive	11	10	–	30	ns	–
Data stable before $\overline{WR}$ inactive	15	30	–	–	ns	–
Data hold after $\overline{WR}$ inactive	16	10	–	–	ns	–
$\overline{RD}$ or $\overline{WR}$ delay after $\overline{READY}$	30	–	–	40	ns	–
$\overline{READY}$ hold time after $\overline{RD}$ or $\overline{WR}$	31	5	–	–	ns	–
Data stable before $\overline{READY}$	32	–	–	90	ns	–
$\overline{RD}$ to $\overline{READY}$ delay	33	–	–	90	ns	–
$\overline{WR}$ to $\overline{READY}$ delay	34	–	–	90	ns	–

10.1.4.2 Motorola Bus Interface Mode

Figure 105 and **Figure 106** show the timing of the SCI Interface and **Table 144** the appropriate timing parameter values.

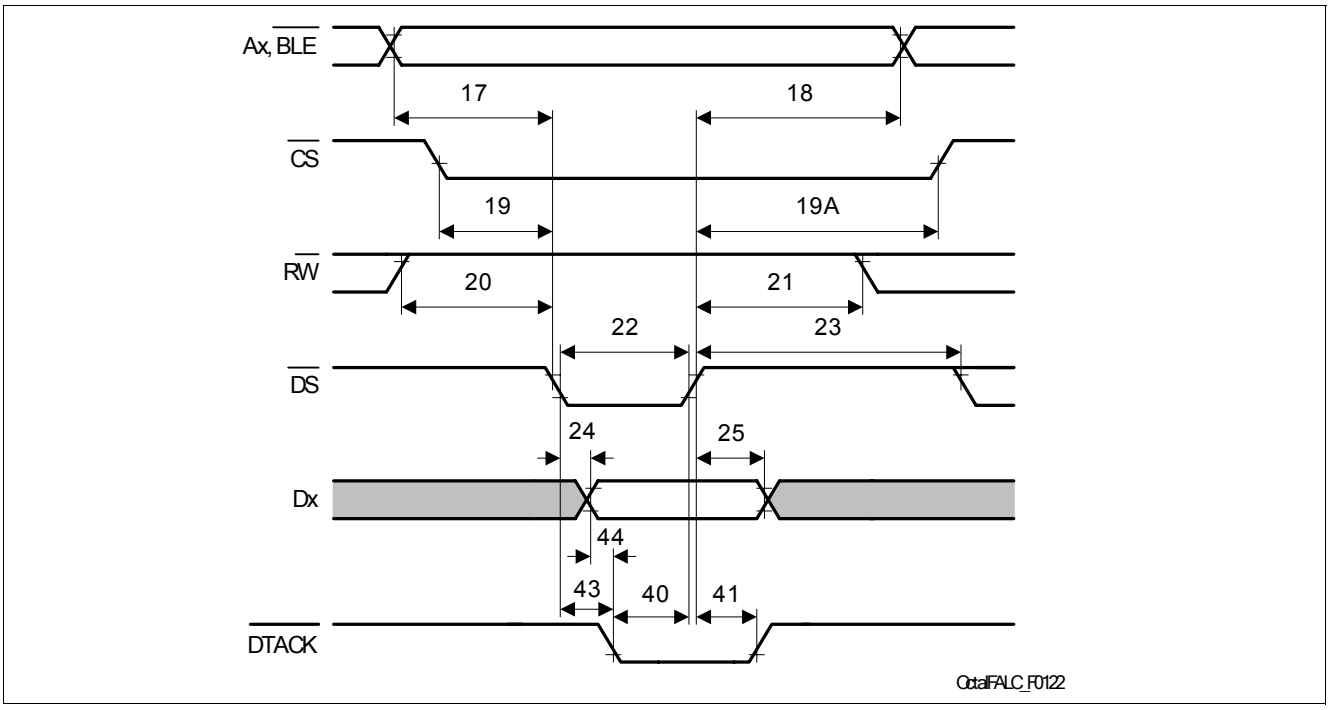


Figure 105 Motorola Read Cycle Timing

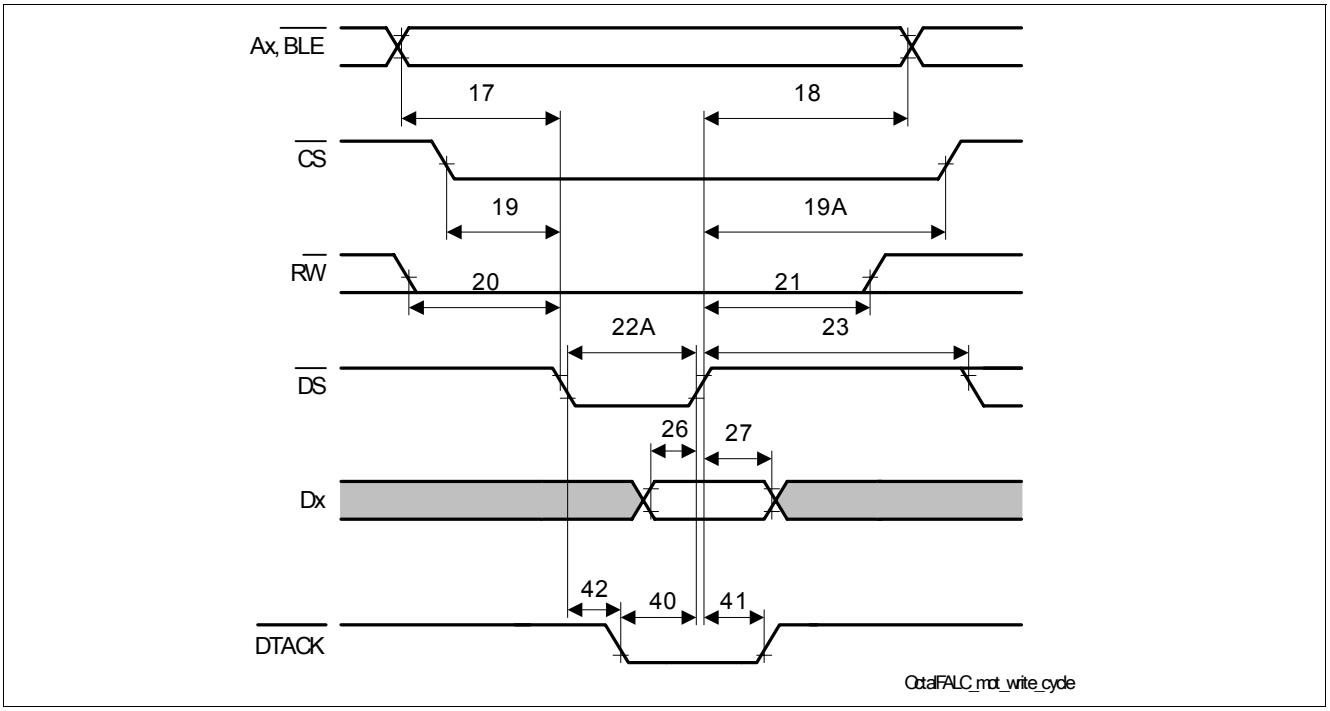


Figure 106 Motorola Write Cycle Timing

Table 144 Motorola Bus Interface Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Address, $\overline{BLE}$ setup time before $\overline{DS}$ active	17	15	–	–	ns	–
Address, $\overline{BLE}$ hold after $\overline{DS}$ inactive	18	0	–	–	ns	–
$\overline{CS}$ active before $\overline{DS}$ active	19	0	–	–	ns	–
$\overline{CS}$ hold after $\overline{DS}$ inactive	19A	0	–	–	ns	–
R$\overline{W}$ stable before $\overline{DS}$ active	20	10	–	–	ns	–
R$\overline{W}$ hold after $\overline{DS}$ inactive	21	0	–	–	ns	–
$\overline{DS}$ pulse width (read access)	22	80	–	–	ns	–
$\overline{DS}$ pulse width (write access)	22A	80	–	–	ns	–
$\overline{DS}$ control interval	23	70	–	–	ns	–
Data valid after $\overline{DS}$ active (read access)	24	–	–	75	ns	–
Data hold after $\overline{DS}$ inactive (read access)	25	–	–	30	ns	–
Data stable before $\overline{DS}$ active (write access)	26	30	–	–	ns	–
Data hold after $\overline{DS}$ inactive (write access)	27	10	–	–	ns	–
$\overline{DS}$ delay after $\overline{DTACK}$	40	–	–	25	ns	–
$\overline{DTACK}$ hold time after $\overline{DS}$ inactive	41	10	–	–	ns	–

Table 144 Motorola Bus Interface Timing Parameter Values (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
$\overline{DS}$ to $\overline{DTACK}$ delay for write	42	–	–	100	ns	–
$\overline{DS}$ to $\overline{DTACK}$ delay for read	43	–	–	100	ns	–
Data strobe before $\overline{DTACK}$	44	0	–	–	ns	–

10.1.4.3 SCI Interface

Figure 107 shows the timing of the SCI Interface and **Table 145** the appropriate timing parameter values.

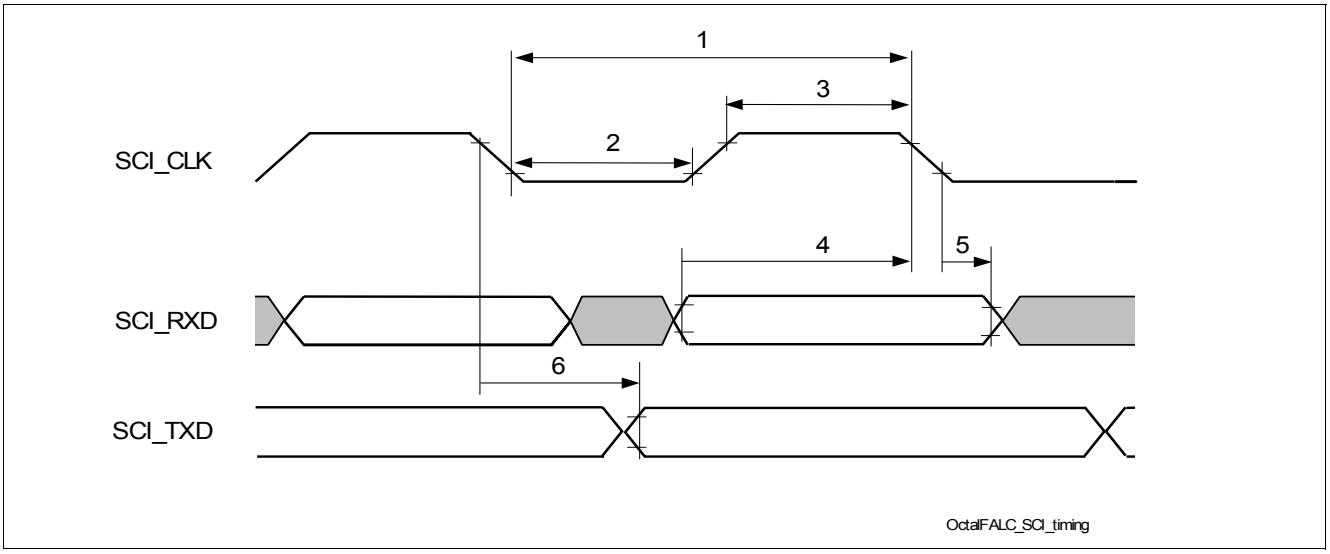


Figure 107 SCI Interface Timing

Table 145 SCI Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SCI_CLK cycle time in full duplex mode	1	170	–	–	ns	–
SCI_CLK cycle time in half duplex mode	1	500	–	–	ns	–
SCI_CLK clock low time	2	76.5	–	–	ns	–
SCI_CLK clock high time	3	76.5	–	–	ns	–
SCI_RXD setup time before SCI_CLK	4	0	–	–	ns	–
SCI_RXD hold time after SCI_CLK	5	0	–	–	ns	–
SCI_TXD delay time after SCI_CLK	6	–	–	30	ns	–

10.1.4.4 SPI Interface

Figure 108 shows the timing of the SCI Interface and **Table 146** the appropriate timing parameter values.

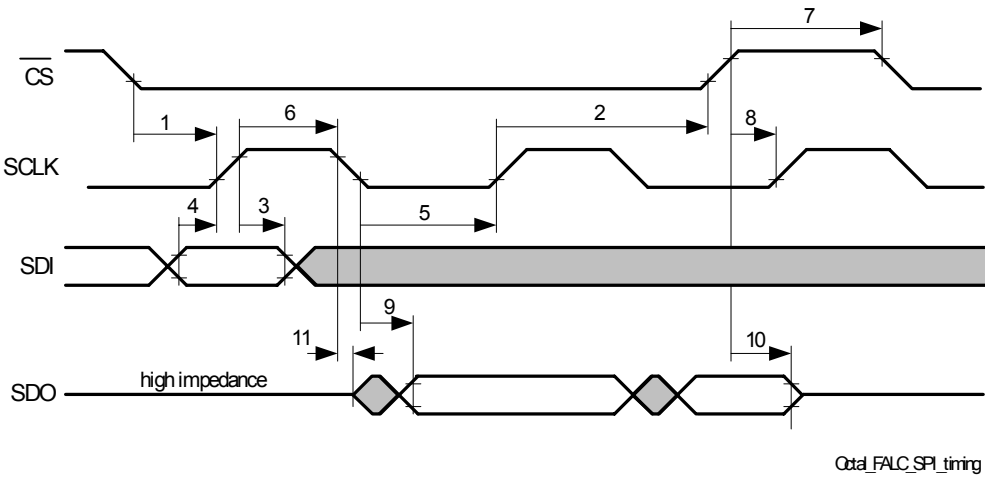


Figure 108 SPI Interface Timing

Table 146 SPI Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SCLK frequency	–	–	–	100	MHz	–
$\overline{CS}$ setup time before SCLK	1	40	–	–	ns	–
$\overline{CS}$ hold time after SCLK	2	40	–	–	ns	–
SDI hold time after SCLK	3	40	–	–	ns	–
SDI setup time before SCLK	4	40	–	–	ns	–
SCLK low time	5	45	–	–	ns	–
SCLK high time	6	45	–	–	ns	–
$\overline{CS}$ high time	7	100	–	–	ns	–
Clock disable time before SCLK	8	50	–	–	ns	–
SDO output stable after SCLK	9	–	–	40	ns	–
SDO output hold after $\overline{CS}$ disable	10	–	–	40	ns	–
SDO output high impedance after SCLK	11	0	–	–	ns	–

10.1.5 Digital Line Interface

Figure 109 and **Figure 110** show the timing and **Table 147**, **Table 148** the appropriate timing parameter values at the digital line interface of the OctalFALC™.

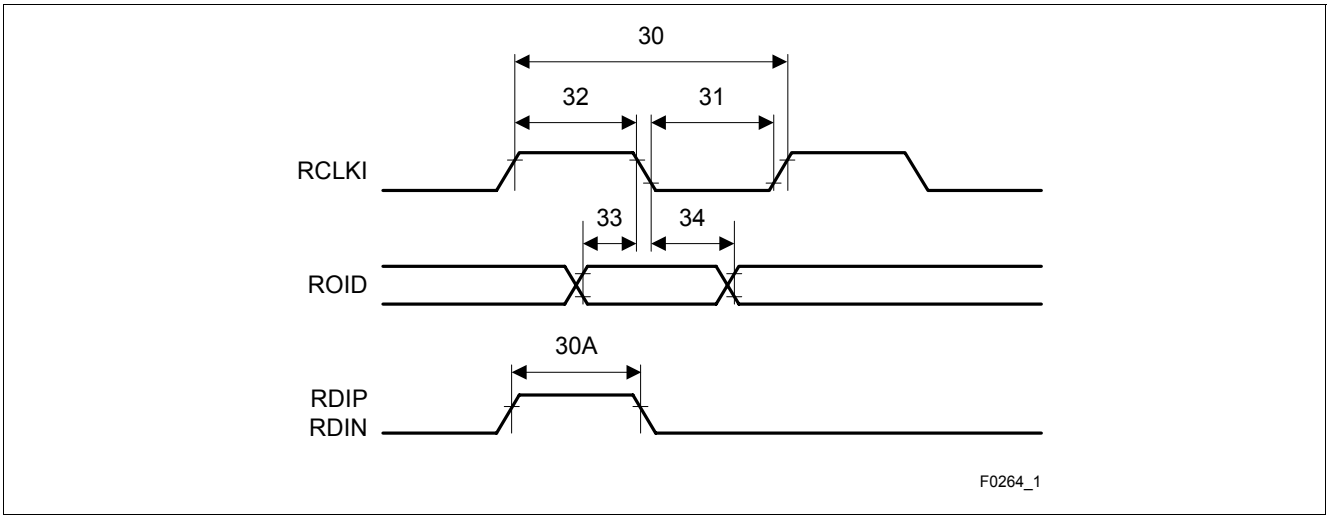


Figure 109 Digital Line Interface Receive Timing

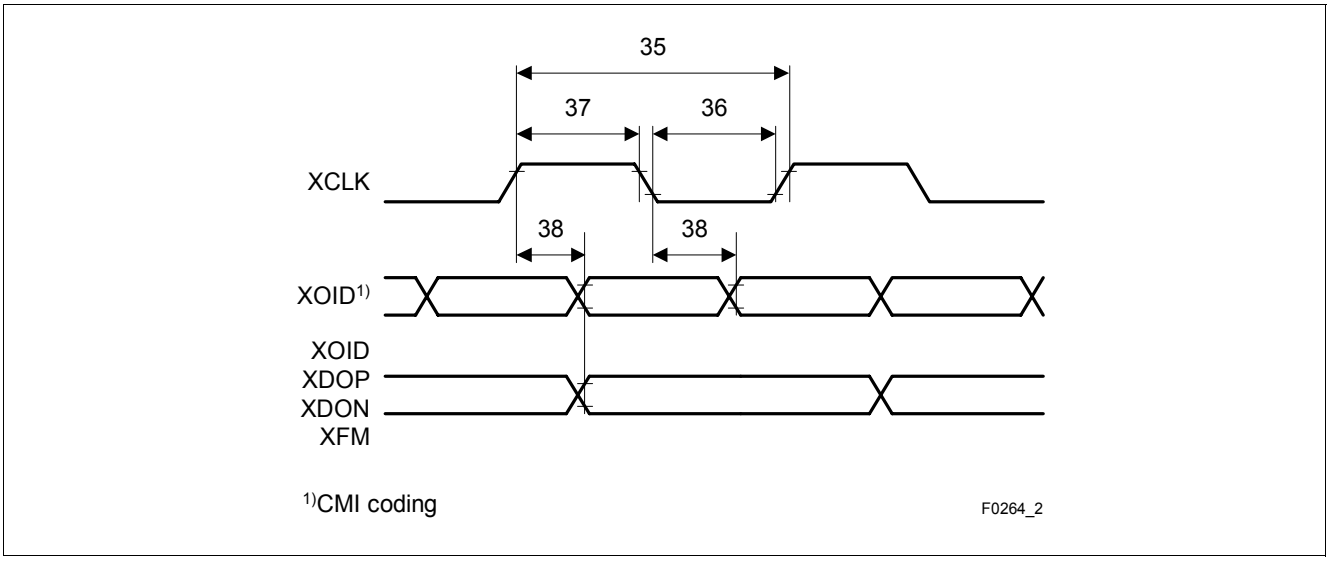


Figure 110 Digital Line Interface Transmit Timing

Table 147 Digital Line Interface Parameter Values for E1

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
RCLKI clock period	30	–	488	–	ns	–
RDIP/RDIN period high	30A	122	244	366	ns	–
RCLKI clock period low	31	180	–	–	ns	–
RCLKI clock period high	32	180	–	–	ns	–
ROID setup	33	50	–	–	ns	–
ROID hold	34	50	–	–	ns	–
XCLK clock period	35	–	488	–	ns	–
XCLK clock period low	36	190	–	–	ns	–
XCLK clock period low[1)]	36	150	–	–	ns	–
XCLK clock period high	37	190	–	–	ns	–

Table 147 Digital Line Interface Parameter Values for E1 (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
XCLK clock period high[1)]	37	150	–	–	ns	–
XOID delay[2)]	38	–	–	60	ns	–
XDOP/XDON delay[3)]	38	–	–	–	–	–

1) Depends on input RCLKI in optical interface and remote loop without transmit jitter attenuator enabled (LIM1.JATT/RL=01)

2) NRZ coding

3) HDB3/AMI/B8ZS coding

Table 148 Digital Line Interface Parameter Values for T1

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
RCLKI clock period	30	–	648	–	ns	–
RDIP/RDIN period high	30A	162	324	486	ns	–
RCLKI clock period low	31	240	–	–	ns	–
RCLKI clock period high	32	240	–	–	ns	–
ROID setup	33	50	–	–	ns	–
ROID hold	34	50	–	–	ns	–
XCLK clock period	35	–	648	–	ns	–
XCLK clock period low	36	230	–	–	ns	–
XCLK clock period low1)	36	200	–	–	ns	–
XCLK clock period high	37	230	–	–	ns	–
XCLK clock period high[1)]	37	200	–	–	ns	–
XOID delay[2)]	38	–	–	60	ns	–
XDOP/XDON delay[3)]	38	–	–	–	–	–

1) Depends on input RCLKI in optical interface and remote loop without transmit jitter attenuator enabled (LIM1.JATT/RL=01)

2) NRZ coding

3) HDB3/AMI/B8ZS coding

10.1.6 System Interface

Figure 111 to **Figure 120** show the timing and **Table 149** to **Table 158** the appropriate timing parameter values at the sysem interface of the OctalFALC™.

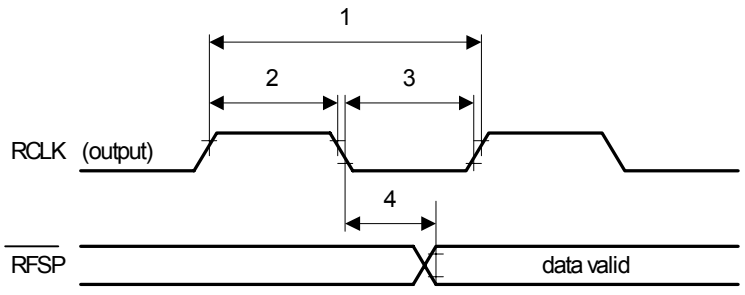


Figure 111 RCLK, $\overline{\text{RFSP}}$ Output Timing

Table 149 RCLK, $\overline{\text{RFSP}}$ Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
RCLK period E1 (2.048 MHz)	1	–	488	–	ns	–
RCLK period E1 (2.048 MHz × 4)	1	–	122	–	ns	–
RCLK period T1/J1 (1.544 MHz)	1	–	648	–	ns	–
RCLK period T1/J1 (1.544 MHz × 4)	1	–	162	–	ns	–
RCLK pulse high	2	40	–	60	%	–
RCLK pulse low	3	40	–	60	%	–
$\overline{\text{RFSP}}$ delay	4	–	–	80	ns	–

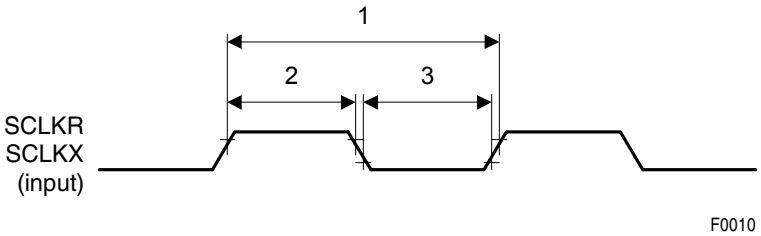


Figure 112 SCLKR/SCLKX Input Timing

Table 150 SCLKR/SCLKX Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SCLKR/SCLKX period at 16.384 MHz	1	–	61	–	ns	–
SCLKR/SCLKX period at 8.192 MHz	1	–	122	–	ns	–

Table 150 SCLKR/SCLKX Timing Parameter Values (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SCLKR/SCLKX period at 4.096 MHz	1	–	244	–	ns	–
SCLKR/SCLKX period at 2.048 MHz	1	–	488	–	ns	–
SCLKR/SCLKX period at 12.352 MHz	1	–	81	–	ns	–
SCLKR/SCLKX period at 6.176 MHz	1	–	162	–	ns	–
SCLKR/SCLKX period at 3.088 MHz	1	–	324	–	ns	–
SCLKR/SCLKX period at 1.544 MHz	1	–	648	–	ns	–
SCLKR/SCLKX pulse high	2	40	–	–	%	–
SCLKR/SCLKX pulse low	3	40	–	–	%	–

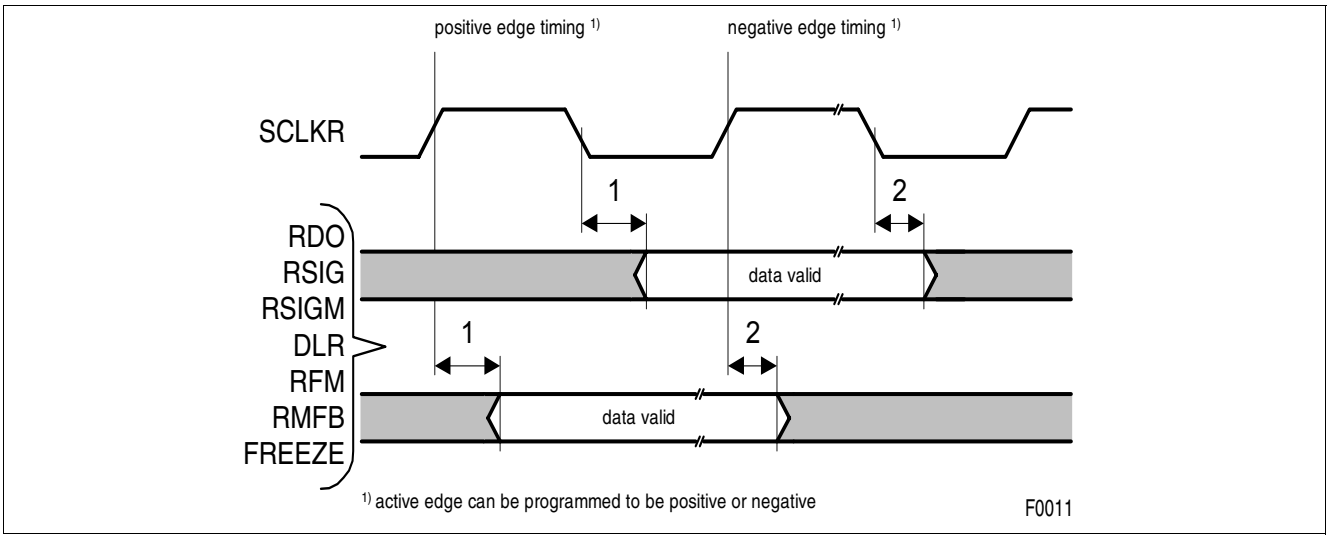


Figure 113 System Interface Marker Timing (Receive)

Table 151 System Interface Marker Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SCLKR input Mode[1)]						
RDO delay	1	0	–	35	ns	–
RSIGM, RMFB, DLR, RFM, FREEZE, RSIG marker delay	2	0	–	45	ns	–
SCLKR Output Mode [1)]						
RDO delay	1A	-10	–	-20	ns	–
RSIGM, RMFB, DLR, RFM, FREEZE, RSIG marker delay	2A	-10	–	-20	ns	–

1) SCLKR can be input or output.

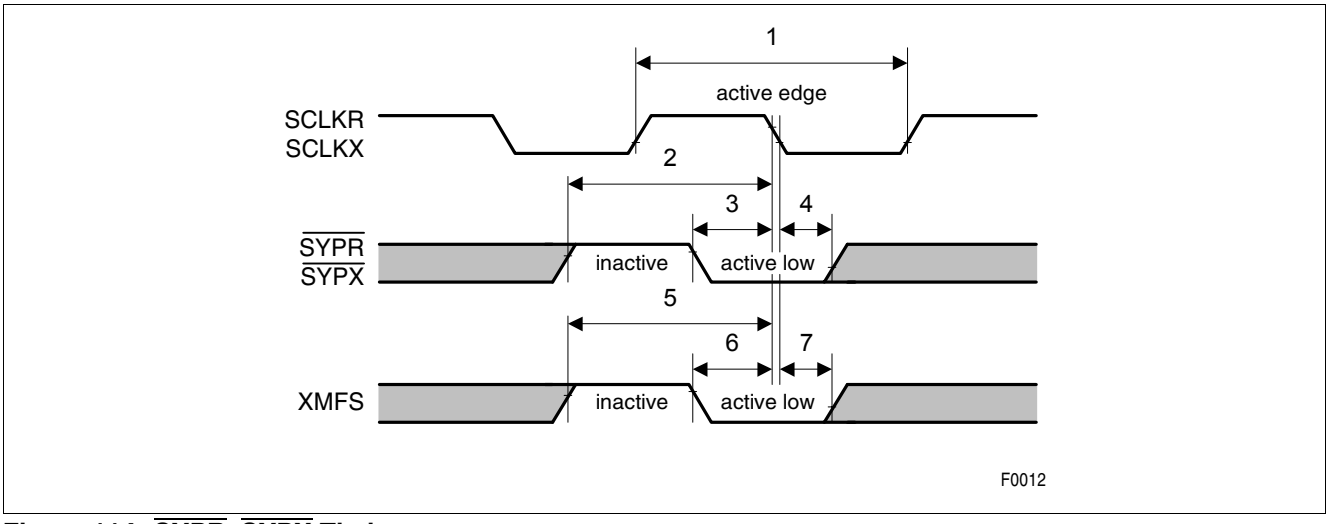


Figure 114 $\overline{\text{SYPR}}$, $\overline{\text{SYPX}}$ Timing

Table 152 $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.[1)]	Max.		
SCLKR input Mode						
SCLKR period	1	61	–	648	ns	–
$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ inactive setup time	2	1 x t_1	–	–	ns	–
$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ setup time	3	5	–	–	ns	–
$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ hold time	4	15	–	–	ns	–
XMFS inactive setup time	5	1 x t_1	–	–	ns	–
XMFS setup time	6	5	–	–	ns	–
XMFS hold time	7	15	–	–	ns	–
SCLKR Output Mode						
SCLKR period	1	61	–	648	ns	–
$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ inactive setup time	2	1 x t_1	–	–	ns	–
$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ setup time	3	10	–	–	ns	–
$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ hold time	4	0	–	–	ns	–
XMFS inactive setup time	5	1 x t_1	–	–	ns	–
XMFS setup time	6	10	–	–	ns	–
XMFS hold time	7	0	–	–	ns	–

1) Typical value, not tested in production

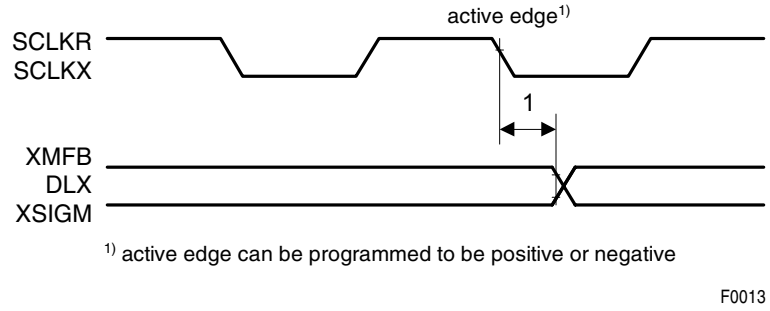


Figure 115 System Interface Marker Timing (Transmit)

Table 153 System Interface Marker Timing Parameter Values 1)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SCLKR input Mode						
XMFB, DLX, XSIGM delay	1	–	–	100	ns	–
SCLKR Output Mode						
XMFB, DLX, XSIGM delay	1	–	–	10	ns	–

1) Parameters based on SCLKR when CMR2.IXSC = 1 and on SCLKX when CMR2.IXSC = ´0´ (input mode only)

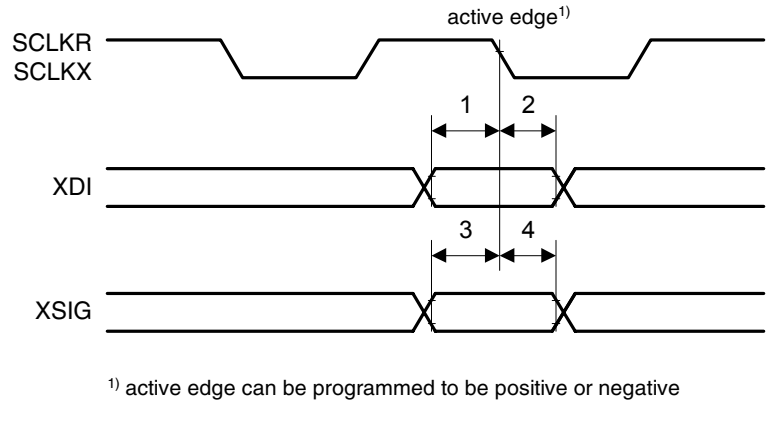


Figure 116 XDI, XSIG Timing

Table 154 XDI, XSIG Timing Parameter Values1)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SCLKR input Mode						
XDI setup time	1	5	–	–	ns	–
XDI hold time	2	15	–	–	ns	–
XSIG setup time	3	5	–	–	ns	–
XSIG hold time	4	15	–	–	ns	–
SCLKR Output Mode						

Table 154 XDI, XSIG Timing Parameter Values[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
XDI setup time	1	10	–	–	ns	–
XDI hold time	2	20	–	–	ns	–
XSIG setup time	3	10	–	–	ns	–
XSIG hold time	4	20	–	–	ns	–

1) Parameters based on SCLKR when CMR2.IXSC = 1 and on SCLKX when CMR2.IXSC = 0 (input mode only)

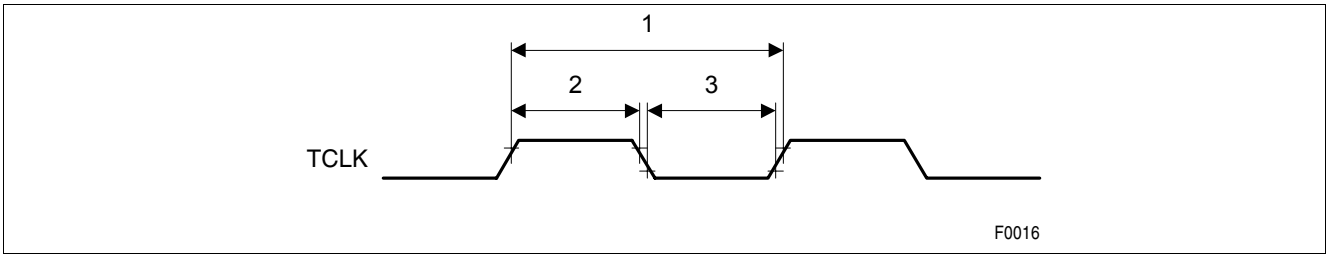


Figure 117 TCLK Input Timing

Table 155 TCLK Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
TCLK period E1 (2.048 MHz)	1	–	488	–	ns	–
TCLK period E1 (2.048 MHz × 4)	1	–	122	–	ns	–
TCLK period T1/J1 (1.544 MHz)	1	–	648	–	ns	–
TCLK period T1/J1 (1.544 MHz × 4)	1	–	162	–	ns	–
TCLK high	2	40	–	–	%	–
TCLK low	3	40	–	–	%	–

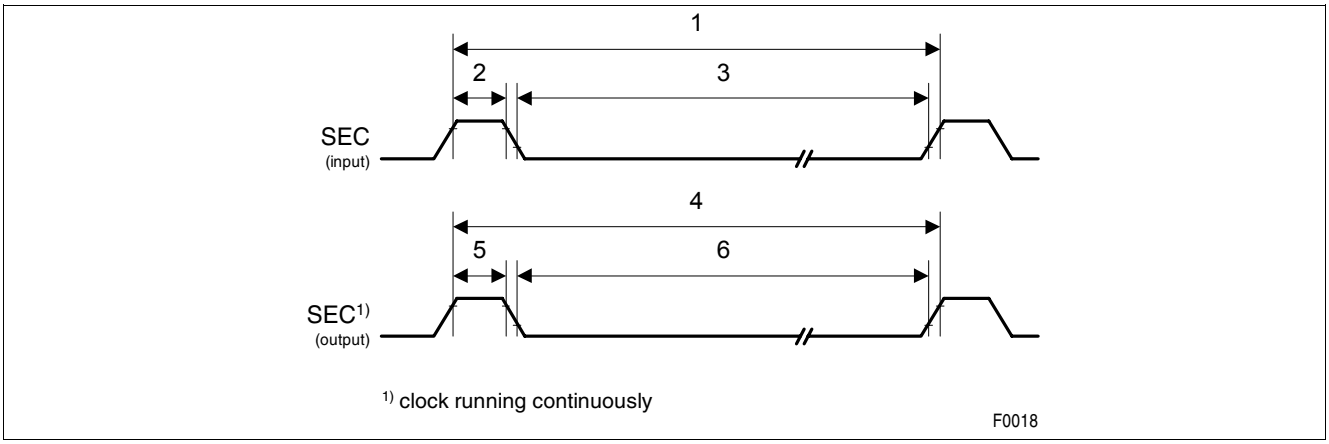


Figure 118 SEC Timing

Table 156 SEC Timing Parameter Values

Parameter[1]	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SEC input period E1/T1/J1	1	–	1	–	s	–
SEC input high E1	2	976	–	–	ns	–
SEC input high T1/J1	2	1296	–	–	ns	–
SEC input low E1	3	976	–	–	ns	–
SEC input low T1/J1	3	1296	–	–	ns	–
SEC output period E1/T1/J1	4	–	1	–	s	–
SEC high output E1	5	976	–	–	ns	–
SEC high output T1/J1	6	1296	–	–	ns	–

1) Typical value, not tested in production

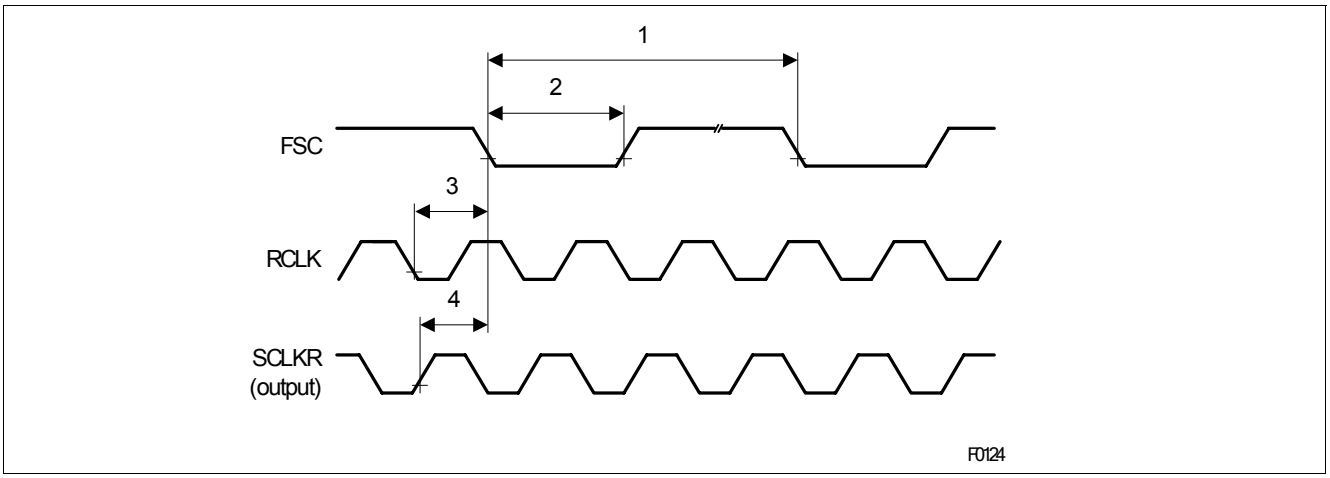


Figure 119 FSC Timing

Table 157 FSC Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
FSC[1] period	1	–	125	–	µs	–
FSC high/low active time E1	2	–	244	–	ns	–
FSC high/low active time T1/J1	2	–	324	–	ns	–
RCLK to FSC delay	3	–	50	80	ns	–
SCLKR to FSC delay[2]	4	–	50	80	ns	–

1) FSC can be programmed to be active high or active low (only the active low timing diagram is shown here)

2) Only valid in case SCLKR is sourced by the DCO-R clock (FSC is always sourced by the DCO-R clock.)

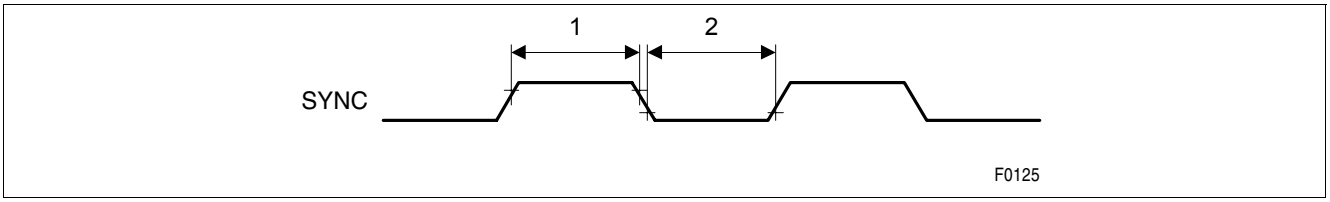


Figure 120 SYNC Timing

Table 158 SYNC Timing Parameter Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
SYNC high time	1	122	–	–	ns	–
SYNC low time	2	125	–	–	ns	–

10.1.7 Pulse Templates - Transmitter

The transmitter inludes a programmable pulse shaper to generate transmit pulse masks according to :

- For T1: FCC68; ANSI T1. 403 1999, figure 4; ITU-T G703 11/2001, figure 10 (for different cable lengths), see **Figure 122**. For measurement configuration were R_{load} = 100 Ω see **Figure 33**.
- For E1: ITU-T G703 11/2001, figure 15 (for 0 m cable length), see **Figure 121**; ITU-T G703 11/2001, figure 20 (for DCIM mode). For measurement configuration were R_{load} = 120 Ω or R_{load} = 75 Ω see **Figure 32**.

The transmit pulse form is programmed either

- By the registers XMP(2:0) compatible to the QuadFALC®, see see **Table 22** and **Table 23**, if the register bit XPM2.XPDIS is cleared
- Or by the registers TXP(16:1), if the register bit XPM2.XPDIS is set, see **Table 25** and **Table 26**.

10.1.7.1 Pulse Template E1

With the given values in **Table 23** or **Table 26**, for transformer ratio: 1 : 2.4, cable type AWG24 and with R_{load} = 120 Ω the pulse mask according to ITU-T G703 11/2001, see **Figure 121**, is fulfiled.

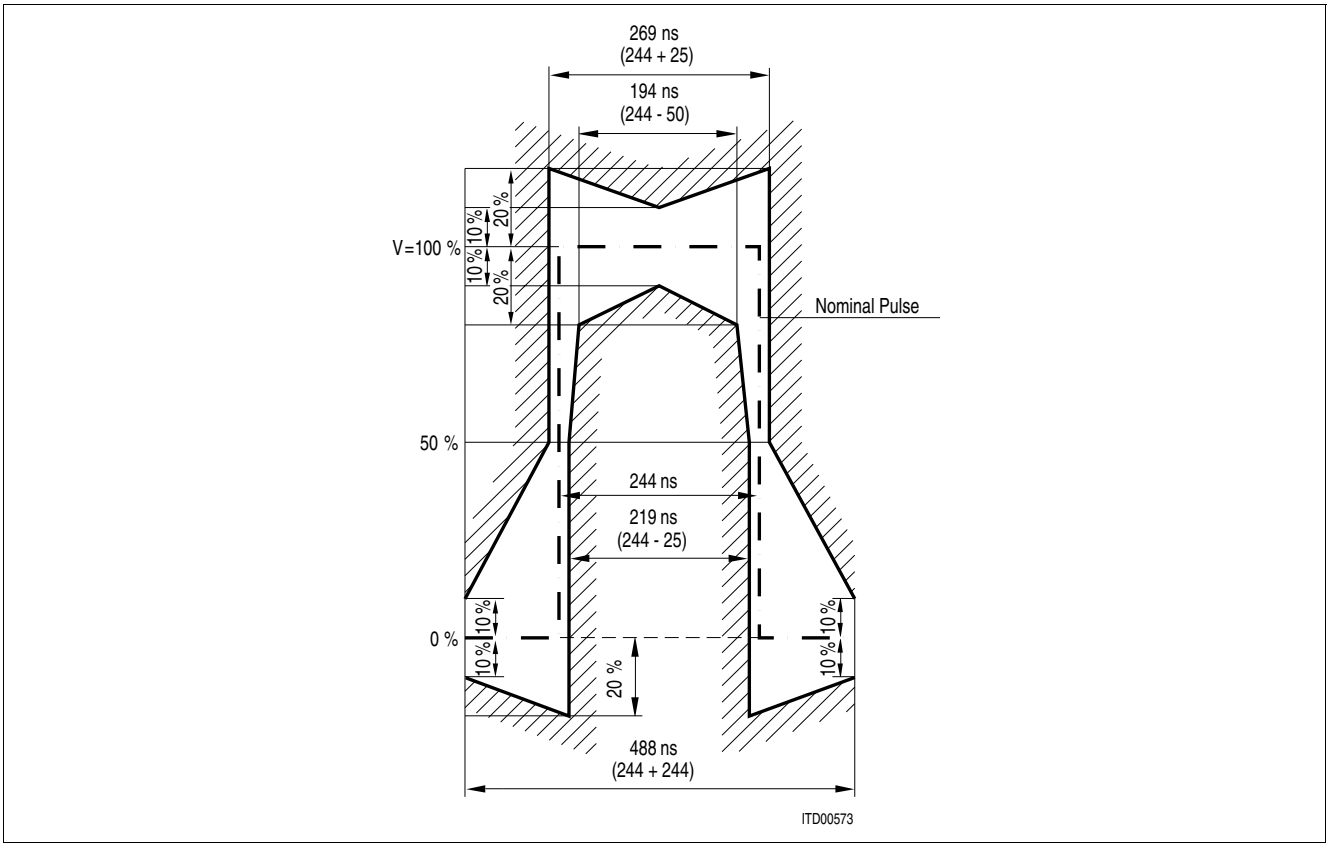


Figure 121 E1 Pulse Shape at Transmitter Output

10.1.7.2 Pulse Template T1

With the given values in **Table 22** or **Table 25**, for transformer ratio: 1 : 2.4, cable type AWG24 and with R_{load} = 100 Ω the pulse mask according to ITU-T G703 11/2001, figure 10, see **Figure 122**, is fulfiled.

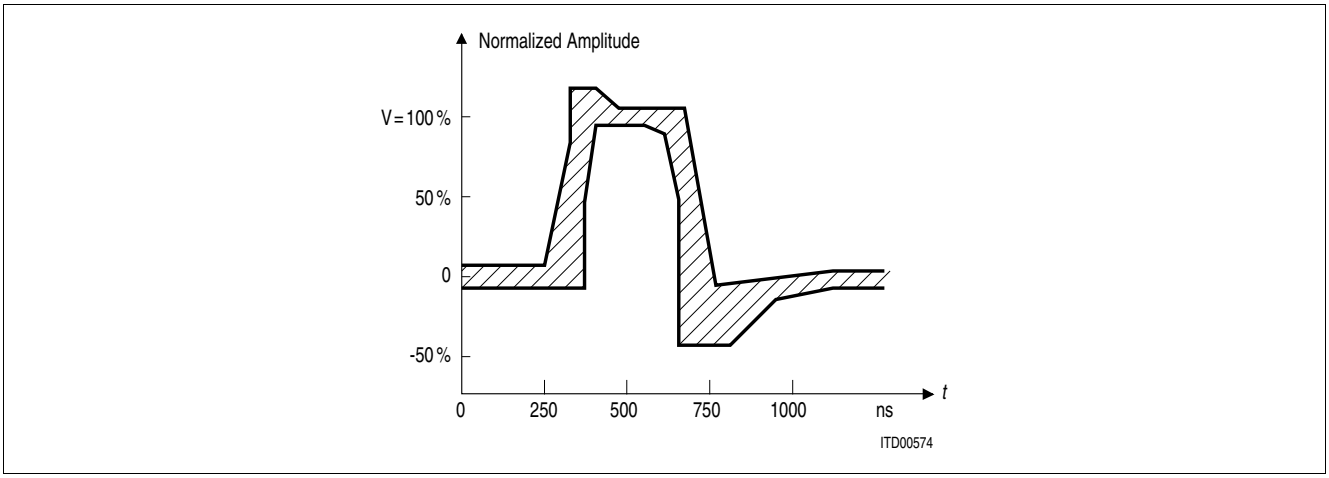


Figure 122 T1 Pulse Shape at the Cross Connect Point

Table 159 T1 Pulse Template at Cross Connect Point (T1.102 [1])

Maximum Curve		Minimum Curve	
Time [ns]	**Level [%][2]**	**Time [ns]**	**Level [%]**
0	5	0	-5
250	5	350	-5
325	80	350	50
325	115	400	95
425	115	500	95
500	105	600	90
675	105	650	50
725	-7	650	-45
1100	5	800	-45
1250	5	925	-20
		1100	-5
		1250	-5

1) Requirements of ITU-T G.703 are also fulfilled

2) 100 % value must be in the range of 2.4 V and 3.6 V;
tested at 0 and 200 m using PIC 22AWG cable characteristics.

10.2 Capacitances

Values of capacitances of the input and of the output pins of the OctalFALC™ are listed in **Table 160**.

Table 160 Capacitances

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{IN}	5	–	10	pF	–
Output capacitance [1]	C_{OUT}	8	–	15	pF	All except XLx
Output capacitance [1]	C_{OUT}	8	–	20	pF	XLx

1) Not tested in production

10.3 Package Characteristics

Text???

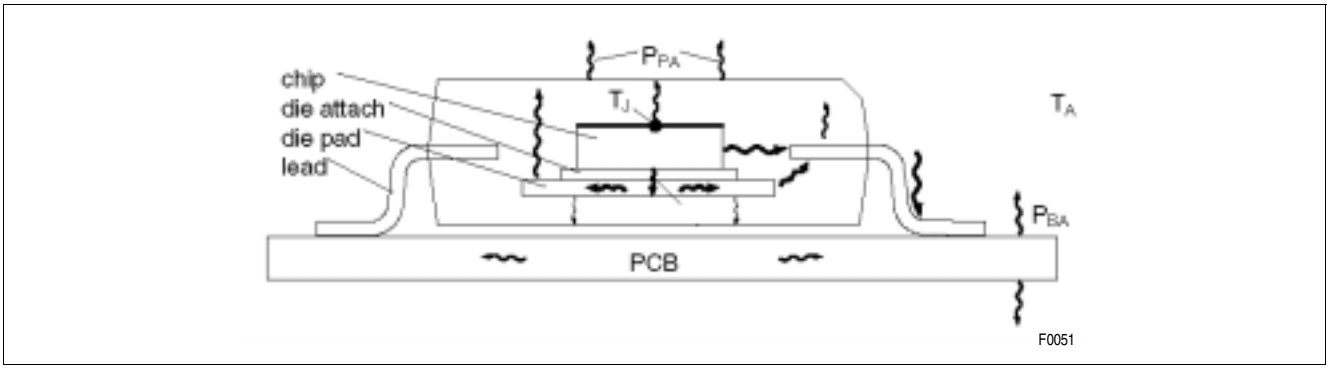


Figure 123 Thermal Behavior of Package

Table 161 Package Characteristic Values

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal Resistance MQFP	R_{thjam} 1)	–	47	–	K/W	Single layer PCB, no convection
	R_{thjc} 2)	–	9	–	K/W	
Thermal Resistance BGA	R_{thjab} 1)	–	29	–	K/W	Single layer PCB, natural convection
Junction Temperature	R_j	–		125	°C	–

1) $R_{thja} = (T_{junction} - T_{ambient})$/Power: Not tested in production.

2) $R_{thjc} = (T_{junction} - T_{case})$/Power: Not tested in production.

10.4 Test Configuration

10.4.1 AC Tests

The values for AC characterstics of the chapters above are based on the following definitions of levels and load capacitances:

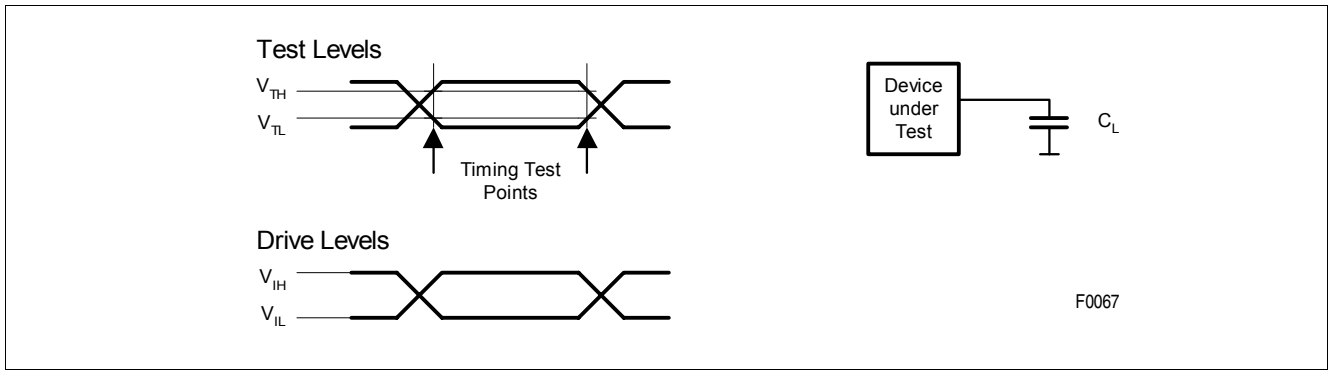


Figure 124 Input/Output Waveforms for AC Testing

Table 162 AC Test Conditions

Parameter	Symbol	Test Values	Unit	Notes
Load Capacitance	C_L	50	pF	–
Input Voltage high	V_{IH}	2.4	V	All except RLx
Input Voltage low	V_{IL}	0.4	V	All except RLx
Test Voltage high	V_{TH}	2.0	V	All except XLx
Test Voltage low	V_{TL}	0.8	V	All except XLx

10.4.2 Power Supply Test

For power supply test all eight channels of the OctalFALC™ are active. Transmitter and receiver are configured as for typical applicatons. The transmitted data are looped back to the receiver by a short line as shown in **Figure 125**. On the system side the interfaces of all channels work independent from another (no multiplex mode is configured).

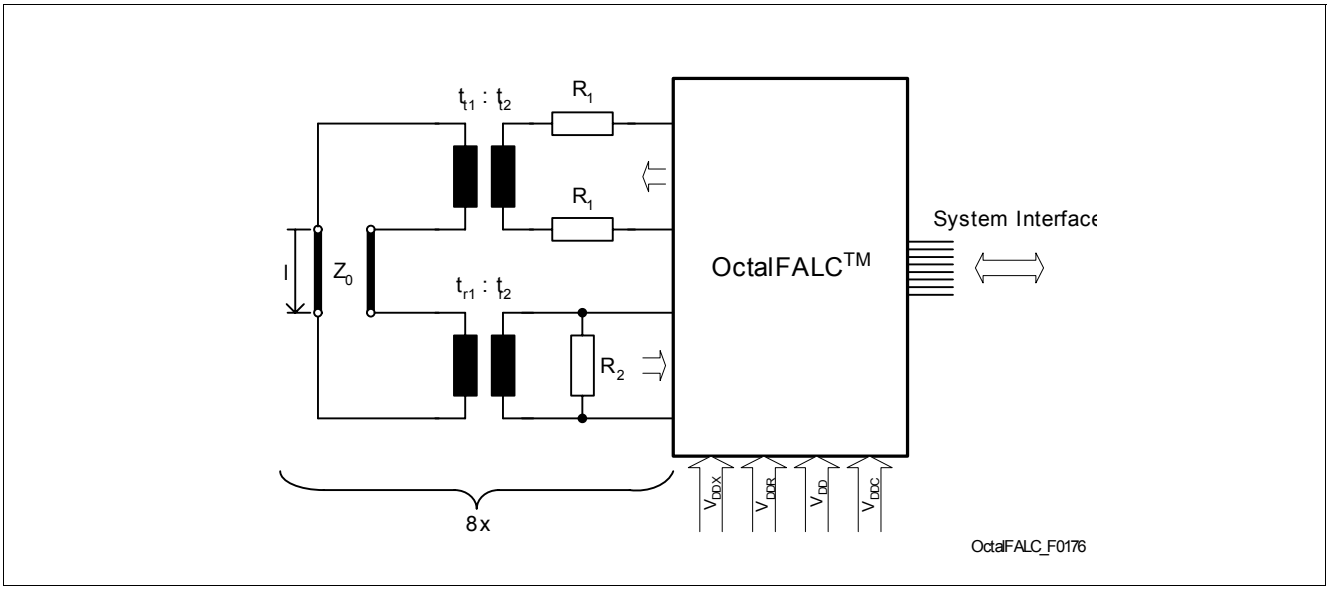


Figure 125 Device Configuration for Power Supply Testing

Table 163 Power Supply Test Conditions E1

Parameter	Symbol	Test Values	Unit	Notes
Load Resistance at transmitter	R_1	7.5	Ω	1%; XL3 and XL4 are left open; PC6.TSRE = ´0´
Termination Resistance at receiver	R_2	120	Ω	1%; (LIM0.RTRS =´0´)
Line Impedance	R_L	120	Ω	–
Line Length	l	< 0.2	m	–
Transformer Ratio Transmit	tt1 : tt2	2.4 : 1		–
Transformer Ratio Receive	tr1 : tr2	1 : 1		–
System interface Frequency	SCLKX SCLKR	2.048	MHz	–
Test Signal	–	2^{15}-1	–	PRBS pattern
Pulse Mask Programming (compatible to QuadFALC®)	XPM2	40_H	–	Pulse mask according to ITU-T G703 11/2001, see **Figure 121**
	XPM1	03_H		
	XPM0	$7B_H$		
Ambient Temperature	–	85	°C	–

Table 164 Power Supply Test Conditions T1/J1

Parameter	Symbol	Test Values	Unit	Notes
Load Resistance	R_1	2	Ω	1%; XL3 and XL4 are left open; PC6.TSRE = ´0´
Termination Resistance	R_2	100	Ω	1%; (LIM0.RTRS =´0´)
Line Impedance	R_L	100	Ω	–
Line Length	l	< 0.2	m	–
Transformer Ratio Transmit	tt1 : tt2	2.4 : 1	–	–
Transformer Ratio Receive	tr1 : tr2	1 : 1	–	–

Table 164 Power Supply Test Conditions T1/J1 (cont'd)

Parameter	Symbol	Test Values	Unit	Notes
System interface Frequency	SCLKX SCLKR	1.544	MHz	–
Test Signal	–	2^{15}-1	–	PRBS pattern
Pulse Mask Programming (compatible to QuadFALC®)	XPM2	02_H	–	Pulse mask according to ITU-T G703 11/2001, figure 10, see **Figure 122**
	XPM1	27_H		
	XPM0	$9F_H$		
Ambient Temperature	–	85	°C	–

11 Operational Description

11.1 Operational Overview

Every of the eight channels of the OctalFALC™ can be operated in two modes, selected by the register bit GCM2.VFREQ_EN, see **Chapter 3.4.6**:

- In the so called “flexible master clocking mode” (GCM2.VFREQ_EN = ´1´) all eight ports can work in E1 or in T1 mode individually, independent from another.
- In the so called “clocking fixed mode” (GCM2.VFREQ_EN = ´0´) all eight ports must work together either in E1 or in T1 mode.

The OctalFALC™ can operate either in two basic modes which are selected by strapping of the pin COMP, see **Chapter 3.1**:

- COMP = ´1´: The “QuadFALC® Compatibility Mode” allows to use the device like two separate QuadFALC®s (“pseudo QuadFALC®”s). The “Compatibility Mode” option allows an easy migration of designs from QuadFALC® to OctalFALC™ without the need for *software* changes. As for the QuadFALC® the register addresses are 10 bits wide.
- COMP = ´0´: The “OctalFALC™ Generic Mode” handles the device as a single entity.

The device is programmable via one of the three integrated micro controller interfaces which are selected by strapping of the pins IM(1:0):

- The asynchronous interface has two modes: Intel (IM(1:0) = ´00_b´) and Motorola (IM(1:0) = ´01_b´). This interface enables byte or word access to all control and status registers, see **Chapter 3.4.1.1**.
- SPI interface (IM(1:0) = ´10_b´), see **Chapter 3.4.2.2**.
- SCI interface (IM(1:0) = ´11_b´), see **Chapter 3.4.2.1**.

The OctalFALC™ has three different kinds of registers:

- The control registers configure the whole device and have write and read access.
- The status registers are read-only and are updated continuously. Normally, the processor reads the status registers periodically to analyze the alarm status and signaling data.
- The interrupt status registers are read-only and are cleared by reading (“rsc”). They are updated (set) continuously. Normally, the processor reads the interrupt status registers after an interrupt occurs (at pin INT in generic mode or at INT1, INT2 in compatibility mode). Masking can be done with the appropriate interrupt mask registers. Mask registers are control registers.

All this registers can be separate into two groups:

- Global registers are not belonging especially to one of the eight channels. The higher address byte is ´00_H´, see also **Table 63**.
- The other registers are belonging to one of the eight channels. The higher address bytes - marked as ´xx_H´ in the register description - are identical to the numbers 0 up to 7 of the appropriate channels. So every of this registers exist eight times in the whole device with the higher address bytes ´00_H´ to ´07_H´ .

11.2 Device Reset

After the device is powered up, the OctalFALC™ must be forced to the reset state first.

The OctalFALC™ is forced to the reset state if a low signal is input on pin $\overline{\text{RES}}$ for a minimum period of 10 µs, see **Figure 100**. During reset the OctalFALC™

- Needs an active clock on pin MCLK
- The pin COMP must have a defined value to select the basic mode
- The pins IM(1:0) must have defined values to select the micro controller interface.
- Only if IM(1:0) = ´11_b´ (SCI interface is selected) the pins A(5:0) must have defined values to select the SCI source address of the device.
- Only if IM1 = ´1´ (SCI or SPI interface is selected) the pins D(15:5) must have defined values to configure the central PLL in the master clocking unit of the device.

During and after reset all internal flip-flops are reset and most of the control registers are initialized with default values.

After reset the complete device is initialized, especially to E1 operation and “flexible master clocking mode”. All new features against the QuadFALC® are disabled. The complete initialization is listed in **Table 165**. Additionally all interrupt mask registers IMR(7:0) are initialized to ´FF_H´, so that not masking is performed.

After reset the OctalFALC™ must be configured first. General guidelines for configuration are described in **Chapter 11.4** for E1 mode and **Chapter 11.5** for T1/J1 mode.

For reset see also **Chapter 3.4.6.1**.

11.3 Device Initialization

After reset, the OctalFALC™ is initialized for E1 doubleframe format with register values listed in the following table.

Table 165 Initial Values after Reset

Register	Reset Value	Meaning
FMR0	´00_H´	NRZ Coding, no alarm simulation.
FMR1, FMR2	´00_H´	E1-doubleframe format, 2 Mbit/s system data rate, no AIS transmission to remote end or system interface, payload loop off.
SIC1, SIC2, SIC3	´00_H´, ´00_H´, ´00_H´	8.192 MHz system clocking rate, receive buffer 2 frames, transmit buffer bypass, data sampled or transmitted on the falling edge of SCLKR/X, automatic freeze signaling, data is active in the first channel phase
LOOP, XSW, XSP, TSWM	´00_H´,´00_H´, ´00_H´, ´00_H´	Channel loop-back and single frame mode are disabled. All bits of the transmitted service word are cleared. Spare bit values are cleared. No transparent mode active.
XC0 XC1	´00_H´, ´$9C_H$´	The transmit clock offset is cleared. The transmit time slot offset is cleared.
RC0, RC1	´00_H´, ´$9C_H$´	The receive clock slot offset is cleared. The receive time slot offset is cleared.
IDLE, ICB(4:1)	´00_H´, ´00_H´	Idle channel code is cleared. Normal operation (no “Idle Channel” selected).
LIM0, LIM1, PCD, PCR	´00_H´, ´00_H´, ´00_H´, ´00_H´	Slave Mode, local loop off Analog interface selected; remote loop off; Pulse count for LOS detection cleared; Pulse count for LOS recovery cleared
XPM(2:0)	´40_H´, ´03_H´, ´$7B_H$´	E1 Transmit pulse template for 0 m but with unreduced amplitude (note that transmitter is in tristate mode)
IMR(5:0)	´FF_H´	All interrupts are disabled
RTR(4:1) TTR(4:1) TSS2 TSS3	All ´00_H´ All ´00_H´ ´00_H´ ´00_H´	No time slots selected
GCR	´00_H´	Internal second timer, power on
CMR1	´00_H´	RCLK output: DPLL clock, DCO-X enabled, DCO-X internal reference clock
CMR2	´00_H´	SCLKR selected, SCLKX selected, receive synchronization pulse sourced by $\overline{\text{SYPR}}$, transmit synchronization pulse sourced by $\overline{\text{SYPX}}$
PC(3:1)	´00_H´, ´$F0_H$´ ´00_H´, ´00_H´	Functions of ports RP(A to B) are $\overline{\text{SYPR}}$ input, function of port RPC is RCLK output (but is only pulled up, because PC5.CRP = ´0´ after reset), functions of ports XP(A to B) are$\overline{\text{SYPX}}$ output. Note that register PC4 is not valid in general for selection of the multi function ports.

Table 165 Initial Values after Reset (cont'd)

Register	Reset Value	Meaning
PC5 PC6	´00_H´ ´00_H´	SCLKR, SCLKX, RCLK configured to inputs, XMFS active low
MODE MODE2 MODE3	´00_H´ ´00_H´ ´00_H´	Signaling controller is disabled and attached to the line side
RAH(2:1) RAL(2:1)	´FD_H´, ´FF_H´, ´FF_H´, ´FF_H´	Compare register for receive address cleared
GCM(6:1)	GCM2 = ´10_H´, others ´00_H´	"Flexible master clocking mode" selected
RTR(4:1) TTR(4:1) TSS2 TSS3	All ´00_H´ All ´00_H´ ´00_H´ ´00_H´	No time slots selected
FMR4	´00_H´	Minimum number of frames for RA and RDI condition, E1 only
SIC4	´00_H´	No further clock edge selection for $\overline{SYPR}$ and $\overline{SYPX}$ is possible
CMR(6:4)	´00_H´	Recovered line clock drives RCLK
GPC2	´00_H´	Source for SEC and RCLK1 is channel 1 (only valid for COMP = ´0´)
TXP(16:1)	TXP(1:8) = ´38_H´ TXP(9:16) = ´00_H´	This registers are not used after reset because XPM2.XPDIS = ´0´
GPC(5:3)	´65_H´, ´43_H´, ´21_H´	Source for RCLK1 up to RCLK7 are the appropriate channels (only valid for COMP = ´0´)
GPC6	´07_H´	QuadFALC® compatible system interface multiplexed modes are selected, source for RCLK8 is channel 8 (both only valid for COMP = ´0´)
INBLDTR	´00_H´	Minimum In-band loop detection time
ALS	´00_H´	No automatic loop switching is performed
PRBSTS(4:1)	All ´00_H´	No time slots are selected for PRBS pattern

The activity level of port XMFS can be selected to be active high or active low by programming PC5.CXMFS. This bit must not be set, if XMFS is not enabled as an input. XMFS input selection is done by programming one of the twoTransmit Multifunction Ports, using registers PC1.XPC1(3:0) or PC2.XPC2(3:0), to ´0001_b´.

Note: For every channel XMFS must not be used together with $\overline{SYPX}$ on different Multifunction Ports.

11.4 Device Configuration in E1 Mode

E1 Configuration

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after reset goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 166** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit FMR1.PMOD should always be kept low (otherwise T1/J1 mode is selected).

Table 166 Configuration Parameters (E1)

Basic Set Up	
Master clocking mode	GCM(8:1) according to external MCLK clock frequency
E1 mode select	FMR1.PMOD = ´0´
Clock system configuration	CMR(3:1), GPC1; if COMP = ´0´ CMR(6:4) and GPC(6:2)
Specification of line interface	LIM0, LIM1, XPM(2:0)
Specification of transmit pulse mask	XPM(2:0) or TXP(16:1)
Line interface coding	FMR0.XC(1:0), FMR0.RC(1:0)
Loss-of-signal detection/recovery conditions	PCD, PCR, LIM1, LIM2
System clocking and data rate	SIC1.SSCC(1:0), SIC1.SSD1,FMR1.SSD0 CMR2.IRSP/IRSC/IXSP/IXSC
System interface multiplex mode	GPC1.SMM, GPC6.SSI16
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS
Multi Function Port selection	PC(3:1)
Operational Set Up	
Select framing	FMR2.RFS(1:0), FMR1.XFS
Framing additions	RC1.ASY4, RC1.SWD
Synchronization mode	FMR1.AFR, FMR2.ALMF
Signaling mode	XSP, XSW, FMR1.ENSA, XSA(8:4), TSWM, MODE, CCR1, CCR2, RAH(2:1), RAL(2:1)

Features like channel loop-back, idle channel activation, extensions for signaling support, alarm simulation, etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Note: Read access to unused register addresses: value should be ignored. Write access to unused register addresses: should be avoided, or set to “00” hex. All control registers (except XFIFO, XS(16:1), CMDR, CMDR(4:2), DEC) are of type Read/Write.

Specific E1 Register Settings

The following is a suggestion for a basic configuration to meet most of the E1 requirements. Depending on different applications and requirement any other configuration can be used.

Table 167 Line Interface Configuration (E1)

FMR0.XC0/ FMR0.RC0/ LIM1.DRS FMR3.CMI	The OctalFALC™ supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI and HDB3 are supported. For the digital line interface modes (dual- or single-rail) the OctalFALC™ supports AMI, HDB3, CMI (with and without HDB3 precoding) and NRZ.
PCD = ´$0A_H$´	LOS detection after 176 consecutive “zeros” (fulfills G.775).
PCR = ´15_H´	LOS recovery after 22 “ones” in the PCD interval. (fulfills G.775).
LIM1.RIL(2:0) = ´02_H´	LOS threshold of 0.6 V (fulfills G.775).

E1 Framer Configuration

The selection of the following modes during the basic configuration supports the ETSI requirements for E-Bit Access, remote alarm and synchronization (please refer also to OctalFALC™ driver code of the evaluation system

EASY 22554 and application notes) and helps to reduce the software load. They are very helpful especially to meet requirements as specified in ETS300 011.

Table 168 Framer Configuration (E1)

XSP.AXS = ´1´	ETS300 011 C4.x for instance requires the sending of E-Bits in TS0 if CRC4 errors have been detected. By programming XSP.AXS = ´1´ the submultiframe status is inserted automatically in the next outgoing multiframe.
XSP.EBP = ´1´	If the OctalFALC™ has reached asynchronous state the E-Bit is cleared if XSP.EBP = 0 and set if XSP.EBP = 1. ETS300 011 requires that the E-Bit is set in asynchronous state.
FMR2.AXRA = ´1´	The transmission of RAI via the line interface is done automatically by the OctalFALC™ in case of loss of frame alignment (FRS0.LFA = ´1´). If basic framing has been reinstalled RAI is automatically reset.
FMR2.FRS(2:1) = ´10_b´ FMR1.AFR = ´1´	In this mode a search of double framing is automatically restarted, if no CRC4 multiframing is found within 8 ms. Together with FMR2.AXRA = ´1´ this mode is essential to meet ETS300 011 and reduces the processor load heavily.
FMR2.ALMF = ´1´	The receiver initiates a new basic- and multiframing research if more than 914 CRC4 errors have been detected in one second.
FMR2.FRS(1:0) = ´11_b´	In the interworking mode the OctalFALC™ stays in double framing format if no multiframe pattern is found in a time interval of 400 ms. This is also indicated by a 400 ms interrupt. Additionally the extended interworking mode (FMR3.EXTIW = ´1´) will activate after 400 ms the remote alarm (FMR2.AXRA = ´1´) and will still search the multiframing without switching completely to the double framing. A complete resynchronization in an 8 ms interval is not initiated.

Table 169 HDLC Controller Configuration (E1)

MODE = ´88_H´ MODE2= ´88_H´ MODE3= ´88_H´	HDLC channel 1 receiver active, no address comparison, attached to line side. HDLC channel 2 receiver active, no address comparison, attached to line side. HDLC channel 2 receiver active, no address comparison, attached to line side.
CCR1 = ´18_H´ CCR3= ´08_H´ CCR4= ´08_H´	Enable signaling via TS(31:0), interframe time fill with continuous flags (channel 1). Interframe time fill with continuous flags (channel 2). Interframe time fill with continuous flags (channel 3).
IMR0.RME = ´0´ IMR0.RPF = ´0´ IMR1.XPR = ´0´ IMR4.RME2 =´0´ IMR4.RPF2 = ´0´ IMR5.XPR2 = ´0´ IMR5.RME3 = ´0´ IMR5.RPF3 = ´0´ IMR5.XPR3 = ´0´	Unmask interrupts for HDLC processor requests.
RTR3.TS16 = ´1´ TTR3.TS16 = ´1´ TSEO = ´00_H´ TSBS1 = ´FF_H´ TSBS2= ´FF_H´ TSBS3= ´FF_H´ TSS2= ´01_H´ TSS3= ´02_H´	Select TS16 for HDLC data reception and transmission. Even and odd frames are used for HDLC reception and transmission. Select all bits of selected time slot (channel 1). Select all bits of selected time slot (channel 2). Select all bits of selected time slot (channel 3). Select time slot 1 for HDLC channel 2. Select time slot 2 for HDLC channel 3.

Table 170 CAS-CC Configuration (E1)

XSP.CASEN = ´1´ CCR1.EITS = ´0´	Send CAS info stored in the XS(16:1) registers.
IMR0.CASC = ´0´	Enable interrupt with any data change in the RS(16:1) registers.

Attention: After the device configuration a software reset must be executed by setting of bits CMDR.XRES/RRES.

11.5 Device Configuration in T1/J1 Mode

After reset, the OctalFALC™ is initialized for E1 doubleframe format. To configure T1/J1 mode, bit FMR1.PMOD has to be set high. After the internal clocking is settled to T1/J1mode (takes up to 20 µs), the following register values are initialized:

T1/J1 Initialization

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after $\overline{\text{RES}}$ goes inactive (high). Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 171** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit FMR1.PMOD must always be kept high (otherwise E1 mode is selected). J1 mode is selected by additionally setting RC0.SJR = ´1´.

Features like channel loop-back, idle channel activation, clear channel activation, extensions for signaling support, alarm simulation, etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Table 171 Configuration Parameters (T1/J1)

Basic Set Up	**T1**	**J1**
Master clocking mode	GCM(6:1) according to external MCLK clock frequency	
T1/J1 mode select	FMR1.PMOD = ´1´, RC0.SJR = ´0´	FMR1.PMOD = ´1´, RC0.SJR = ´1´
Clock system configuration	CMR(3:1), GPC1; if COMP = ´0´ CMR(6:4) and GPC(6:2)	
Specification of line interface	LIM0, LIM1,	
Specification of transmit pulse mask	XPM(2:0) or TXP(16:1)	
Line interface coding	FMR0.XC(1:0), FMR0.RC(1:0)	
Loss-of-signal detection/recovery conditions	PCD, PCR, LIM1, LIM2	
System clocking and data rate	SIC1.SSC(1:0), SIC1.SSD1, FMR1.SSD0, CMR1.IRSP/IRSC/IXSP/IXSC	
System interface multiplex mode	GPC1.SMM, GPC6.SSI16	
Channel translation mode	FMR1.CTM	
Transmit offset counters	XC0.XCO, XC1.XTO	
Receive offset counters	RC0.RCO, RC1.RTO	
AIS to system interface	FMR2.DAIS/SAIS	
Multi Function Port selection	PC(3:1)	
Operational Set Up		
Select framing	FMR4.FM(1:0)	

Table 171 Configuration Parameters (T1/J1) (cont'd)

Basic Set Up	T1	J1
Framing additions	FMR1.CRC, FMR0.SRAF	
Synchronization mode	FMR4.AUTO, FMR4.SSC(1:0), FMR2.MCSP, FMR2.SSP	
Signaling mode	FMR5.EIBR, XC0.BRM, MODE, MODE2, MODE3, CCR1, CCR2, RAH(2:1), RAL(2:1)	

Note: Read access to unused register addresses: value should be ignored. Write access to unused register addresses: should be avoided, or set to ´00_H´. All control registers (except XFIFO, XS(12:1), CMDR, DEC) are of type read/write

Specific T1/J1 Configuration

The following is a suggestion for a basic configuration to meet most of the T1/J1 requirements. Depending on different applications and requirements any other configuration can be used.

Table 172 Line Interface Configuration (T1/J1)

Register	Function
FMR0.XC0/1 FMR0.RC0/1 LIM1.DRS CCB(3:1) SIC3.CMI	The OctalFALC™ supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI (with and without bit 7stuffing) and B8ZS are supported. For the digital line interface modes (dual- or single-rail) the OctalFALC™ supports AMI (with and without bit 7 stuffing), B8ZS (with and without B8ZS precoding) and NRZ.
PCD = ´$0A_H$´	LOS detection after 176 consecutive "zeros" (fulfills G.775/Telcordia (Bellcore)/AT&T)
PCR = ´15_H´	LOS recovery after 22 "ones" in the PCD interval (fulfills G.775, Bellcore/AT&T).
LIM1.RIL(2:0) = ´02_H´	LOS threshold of 0.6 V (fulfills G.775).
GCR.SCI = ´1´	Additional Recovery Interrupts. Help to meet alarm activation and deactivation conditions in time.
LIM2.LOS1 = ´1´	Automatic pulse-density check on 15 consecutive zeros for LOS recovery condition (Bellcore requirement)

Table 173 Framer Configuration (T1/J1)

Register	Function	
	T1	J1
FMR4.SSC(1:0)	Selection of framing sync conditions	
FMR4.FM(1:0)	Select framing format	
FMR2.AXRA = ´1´	The transmission of RAI via the line interface is done automatically by the OctalFALC™ in case of Loss of Frame Alignment (FRS0.LFA = ´1´). If framing has been reinstalled RAI is automatically reset	
FMR4.AUTO = ´1	Automatic synchronization in case of definite framing candidate (FRS0.FSRF). In case of multiple framing candidates and CRC6 errors different resynchronization conditions can be programmed via FMR2.MCSP/SSP.	
RCO.SJR[1] = ´1´ FMR0.SRAF = ´0´ XSW.XRA = ´1´		Remote alarm handling via DL-channel according to ITU-T JG.704 using pattern "1111111111111111_b"
RCO.SJR = ´0´	CRC6 calculation without FS/DL-bits	
RCO.SJR = ´1´		CRC6 calculation including FS/DL-bits

Table 173 Framer Configuration (T1/J1) (cont'd)

Register	Function	
	T1	J1
FMR4.AUTO = ´1´	Automatic synchronization in case of definite framing candidate (FRS0.FSRF). In case of multiple framing candidates and CRC6 errors different resynchronization conditions can be programmed via FMR2.MCSP/SSP.	
FMR4.SSC1 = ´1´ FMR4.SSC0 = ´1´ FMR2.MCSP = ´0´ FMR2.SSP = ´1´		Synchronization and resynchronization conditions, for details see register description

1) Remote alarm handling and CRC6 calculation are commonly selected by RC0.SJR

Table 174 HDLC Controller Configuration (T1/J1)

MODE = ´88_H´ MODE2= ´88_H´ MODE3= ´88_H´	HDLC channel 1 receiver active, no address comparison. HDLC channel 2 receiver active, no address comparison. HDLC channel 2 receiver active, no address comparison.
CCR1 = ´18_H´ CCR3= ´08_H´ CCR4= ´08_H´	Enable signaling via TS(24:1), interframe time fill with continuous flags (channel 1). Interframe time fill with continuous flags (channel 2). Interframe time fill with continuous flags (channel 3).
IMR0.RME = ´0´ IMR0.RPF = ´0´ IMR1.XPR = ´0´ IMR4.RME2 = ´0´ IMR4.RPF2 = ´0´ IMR5.XPR2 = ´0´ IMR5.RME3 = ´0´ IMR5.RPF3 = ´0´ IMR5.XPR3 = ´0´	Unmask interrupts for HDLC processor requests.
RTR4.0 = ´1´ TTR4.0 = ´1´ TSEO = ´00_H´ TSBS1 = ´FF_H´ TSBS2 = ´FF_H´ TSBS3 = ´FF_H´ TSS2 = ´01_H´ TSS3 = ´02_H´	Select time slot 24 for HDLC data reception and transmission. Even and odd frames are used for HDLC reception and transmission. Select all bits of selected time slot (channel 1). Select all bits of selected time slot (channel 2). Select all bits of selected time slot (channel 3). Select time slot 1 for HDLC channel 2. Select time slot 2 for HDLC channel 3.

Table 175 Configuration of the CAS-BR Controller (T1/J1)

FMR5.EIBR = ´1´	Enable CAS-BR Mode Send CAS-BR information stored in XS(12:1)
IMR1.CASE = ´0´ IMR0.RSC = ´0´	Enable interrupts which indicate the access to the XS(12:1) CAS-BR registers and any data change in RS(12:1)

Note: After the device configuration a software reset should be executed by setting of bits CMDR.XRES/RRES.

11.6 Device Configuration for Digital Clock Interface Mode (DCIM)

The following table shows the necessary configuration for the Digital Clock Interface Mode (DCIM), see ITU-T G.703 11/2001, chapter 13. The receive clock at RL1/RL2 (2.048MHz) is supported at multi function port RPC. The transmit clock at SCLKX (2.048MHz) is transmitted at XL1/XL2.

DCIM mode is standardized only for 2.048 MHz (E1 mode, FMR1.PMOD = ´0´). The OctalFALC™ can handle also 1.544MHz if FMR1.PMOD = ´1´.

Table 176 Device Configuration for DCIM Mode

FMR1.PMOD	Selects 2.048 MHz or 1.544 MHz, see text above
LIM0.DCIM = ´1´	Selects DCIM mode.
LIM1.RL = ´0´	TX clock mode.
CMR1.DXSS = ´0´	
CMR1.DXJA = ´0´	
LIM1.DRS = ´0´ FMR0.RC(1:0) = ´10_b´	Line interface mode RX
FMR0.XC(1:0) = ´10_b´	Line interface mode TX
PC1.RPC1(3:0) = ´1111_b´	Select RCLK as output
PC5.CRP = ´1´	
CMR1.DRSS(1:0) or CMR5.DRSS(2:0) : select the appropriate channel	RX clock mode
CMR1.DCS = ´1´	
LIM0.MAS = ´0´	
CMR1.RS(1:0) = ´10_b´ or CMR4.RS(2:0) = ´010_b´	
GCM(1:8) see **Chapter 3.4.6** and **GCM6_E**	Configure clock system
LIM2.SCF, CMR6.SCFX, CMR2.ECFAX, CMR2.ECFAR, CMR3:CFAX(3:0), CMR3.CFAR(3:0), CMR4.IAR(4:0), CMR5.IAX(4:0): see **Chapter 3.6.5** and **Table 15**	Configure DCO-X and DCO-R
SIC1.RBS(1:0) = ´10_b´	Configure elastic buffers
SIC1.XBS(1:0) = ´11_b´	

12 Signaling Controller Operating Modes

The three HDLC controllers can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way, to satisfy almost any practical requirements.

There are 4 different operating modes which can be set via the mode registers (MODE, MODE2 and MODE3).

If not mentioned otherwise, all functions described for HDLC channel 1 apply to channel 2 and 3 as well.

12.1 HDLC Mode

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Depending on the selected address mode, the OctalFALC™ can perform a 1- or 2-byte address recognition (MODE.MDS0).

If a 2-byte address field is selected, the high address byte is compared to the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address is recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the OctalFALC™ can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match any of the address combinations, are ignored by the OctalFALC™.

In case of a 1-byte address, RAL1 and RAL2 are used as compare registers. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. Additional information can also be read from a special register (RSIS).

As defined by the HDLC protocol, the OctalFALC™ performs the zero bit insertion/deletion (bit stuffing) in the transmit/receive data stream automatically. That means, it is guaranteed that at least one “0” will appear after 5 consecutive “1”s.

12.1.1 Non-Auto Mode

(MODE.MDS(2:1) = ´01_b´; MODE2.MDS22.21 =´01_b´; MODE3.MDS32.31 =´01_b´)

Characteristics: address recognition, flag- and CRC generation/check, bit stuffing

All frames with valid addresses are forwarded directly via the RFIFO (RFIFO2, RFIFO3) to the system memory.

12.1.2 Transparent Mode 1

(MODE.MDS(2:0) = ´101_b´; MODE2.MDS2(2:0) =´101_b´; MODE3.MDS3(2:0) =´101_b´)

Characteristics: address recognition, flag- and CRC generation/check, bit stuffing

Only the high byte of a 2-byte address field is compared to registers RAH(2:1). The whole frame excluding the first address byte is stored in RFIFO (RFIFO2, RFIFO3).

12.1.3 Transparent Mode 0

(MODE.MDS(2:0) = ´100_b´; MODE2.MDS2(2:0)=´100_b´; MODE3.MDS3(2:0)=´100_b´)

Characteristics: flag- and CRC generation/check, bit stuffing

No address recognition is performed and each frame is stored in the RFIFO (RFIFO2, RFIFO3).

12.1.4 SS7 Support

SS7 protocol is supported for channel 1 only by means of several hardware features.

12.1.5 Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames in the different operating modes.

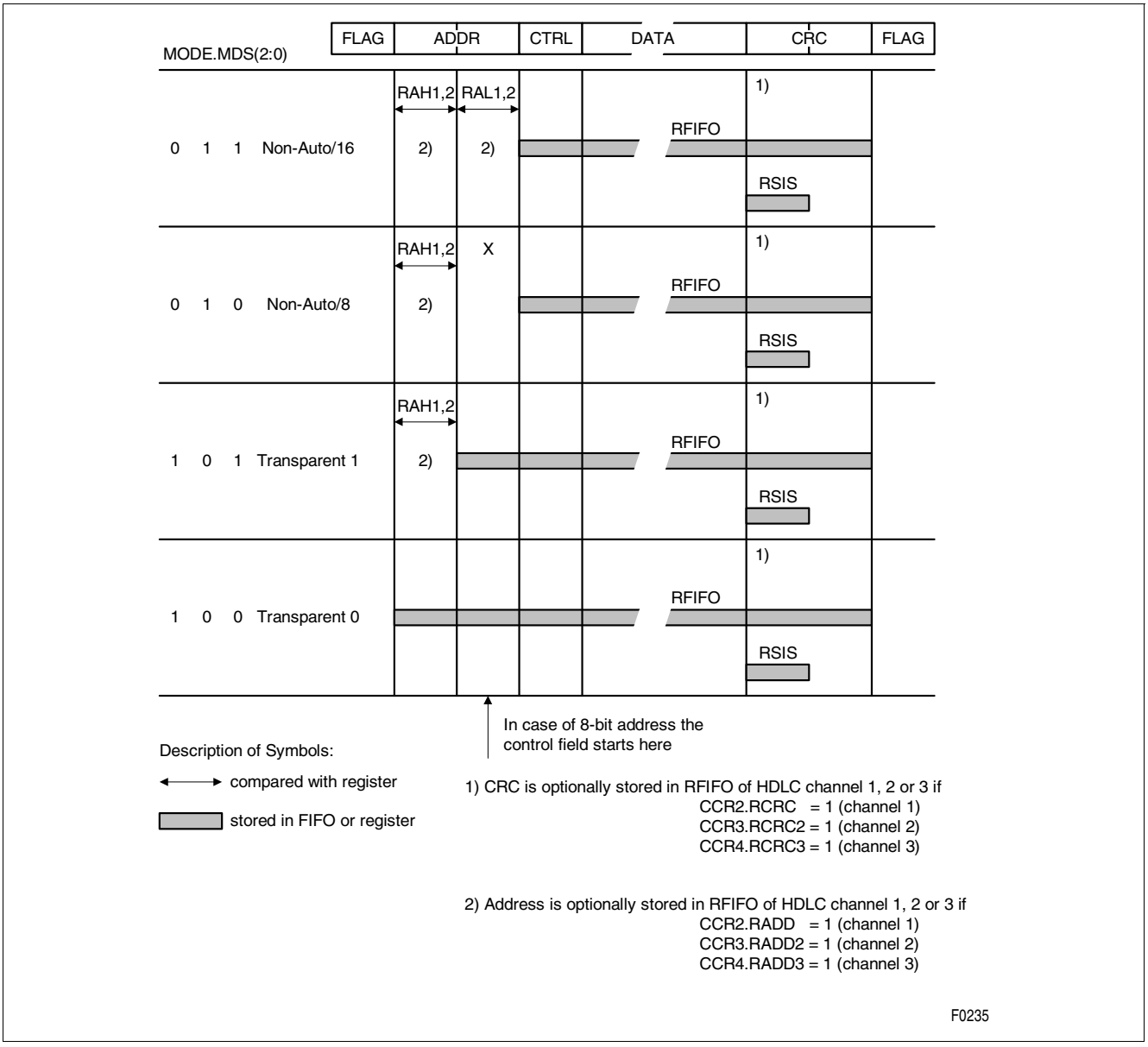


Figure 126 HDLC Receive Data Flow

12.1.6 Transmit Data Flow

The frames can be transmitted as shown below.

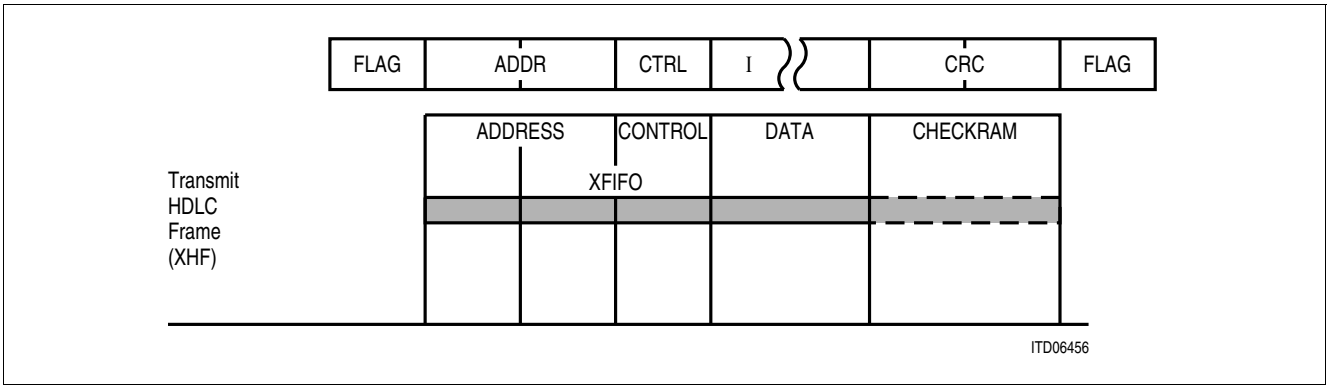


Figure 127 HDLC Transmit Data Flow

Transmitting a HDLC frame via register CMDR.XTF (or CMDR2.XTF2/CMDR3.XTF3 for channel 2/3), the address, the control fields and the data field have to be entered in the XFIFO (XFIFO2, XFIFO3).

If CCR2.XCRC (or CCR3.XCRC2/CCR4.XCRC3 for channel 2/3) is set, the CRC checksum will not be generated internally. The checksum has to be provided via the transmit FIFO (XFIFO, XFIFO2, XFIFO3) as the last two bytes. The transmitted frame is closed automatically with a closing flag only.

The OctalFALC™ does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

12.2 Extended Transparent Mode

Characteristics: fully transparent

In no HDLC mode, fully transparent data transmission/reception without HDLC framing is performed, i.e. without flag generation/recognition, CRC generation/check, or bit stuffing. This feature can be profitably used e.g. for:

- Specific protocol variations
- Transmission of a BOM frame (channel 1 only)
- Test purposes

Data transmission is always performed out of the XFIFO (XFIFO2, XFIFO3). In transparent mode, the receive data is shifted into the RFIFO (RFIFO2, RFIFO3).

Note: If a 1-byte frame is sent in extended transparent mode, in addition to interrupt ISR1.XPR (transmit pool ready) the interrupt ISR1.XDU (transmit buffer underrun) is set and XFIFO is blocked.

12.3 Signaling Controller Functions

12.3.1 Transparent Transmission and Reception

When programmed in the extended transparent mode via the MODE registers (MODE.MDS(2:0) = ´111_b´, MODE2.MDS2(2:0)=´111_b´, MODE3.MDS3(2:0)=´111_b´), the OctalFALC™ performs fully transparent data transmission and reception without HDLC framing, i.e. without

- Flag insertion and deletion
- CRC generation and checking
- Bit stuffing

In order to enable fully transparent data transfer, bit MODE.HRAC (MODE2.HRAC2, MODE3.HRAC3) has to be set.

Received data is always shifted into RFIFO (RFIFO2, RFIFO3).

Data transmission is always performed out of XFIFO (XFIFO2, XFIFO3) by shifting the contents of XFIFO into the outgoing data stream directly. Transmission is initiated by setting CMDR.XTF (´04_H´). A synchronization byte ´FF_H´ is sent automatically before the first byte of the XFIFO is transmitted.

Cyclic Transmission (fully transparent)

If the extended transparent mode is selected, the OctalFALC™ supports the continuous transmission of the contents of the transmit FIFOs.

After having written 1 up to 64 bytes to XFIFO (XFIFO2, XFIFO3), the command XREP&XTF (CMDR = ´00100100_b´ = ´24_H´) forces the OctalFALC™ to transmit the data stored in XFIFO to the remote end repeatedly.

Note: The cyclic transmission continues until a reset command (CMDR.SRES) is issued or with resetting of CMDR.XREP, after which continuous "1"s are transmitted. During cyclic transmission the XREP-bit has to be set with every write operation to CMDR. The same handling applies to CMDR2 and CMDR3 for HDLC channels 2 an 3.

12.3.2 CRC on/off Features

As an option in HDLC mode the internal handling of the received and transmitted CRC checksum can be influenced via control bits CCR2.RCRC and CCR2.XCRC (channel 2: CCR3.RCRC2, CCR3.XCRC2, channel 3: CCR4.RCRC3, CCR4.XCRC3).

- Receive Direction

The received CRC checksum is always assumed to be in the 2 last bytes of a frame (CRC-ITU), immediately preceding a closing flag. If CCR2.RCRC is set, the received CRC checksum is written to RFIFO where it precedes the frame status byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If HDLC mode is selected, the limits for "Valid Frame" check are modified (refer to description of bit RSIS.VFR).

- Transmit Direction

If CCR2.XCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame is closed automatically by a closing flag only.

The OctalFALC™ does not check whether the length of the frame, i.e. the number of bytes to be transmitted is valid or not.

12.3.3 Receive Address Pushed to RFIFO

The address field of received frames can be pushed to the receive FIFOs (first one or two bytes of a frame). This function is used together with extended address recognition. It is enabled by setting control bit CCR2.RADD (CCR3.RADD2, CCR4.RADD3).

12.3.4 HDLC Data Transmission

In transmit direction 2 x 64 byte FIFO buffers are provided for each HDLC channel. After checking the XFIFO status by polling bit SIS.XFW (SIS2.XFW2, SIS3,XFW3) or after an interrupt ISR1.XPR (ISR5.XPR2, ISR5.XPR3, Transmit Pool Ready), up to 32 bytes can be entered by the external micro controller to the XFIFOs.

The transmission of a frame can be started by issuing a XTF or XHF command via the command registers. If the transmit command does not include an end of message indication (CMDR.XME, CMDR3.XME2, CMDR4.XME3), the OctalFALC™ will repeatedly request for the next data block by means of an XPR interrupt as soon as no more than 64bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the external micro controller.

This process is repeated until the external micro controller indicates the end of message by XME command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive frames can share a flag, or can be transmitted as back-to-back frames, if service of the XFIFOs is fast enough.

In case no more data is available in the XFIFOs prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the external micro controller is notified by interrupt ISR1.XDU (ISR4.XDU2, ISR5.XDU3). The frame can be aborted by software using CMDR.SRES (CMDR3.SRES2, CMDR4.SRES3).

The data transmission sequence, from the external micro controller's point of view, is outlined in **Figure 128**.

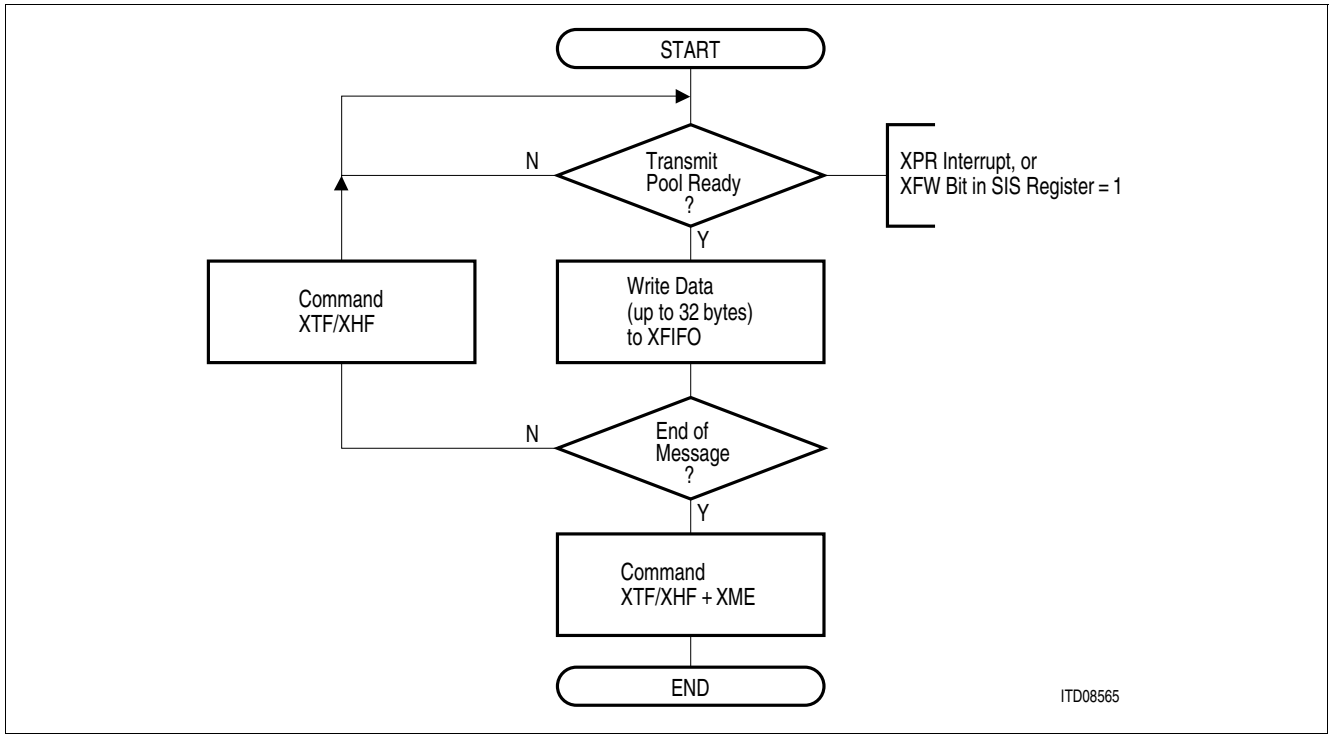


Figure 128 Interrupt Driven Data Transmission (flow diagram)

The activities at both serial and external micro controller interface during frame transmission (supposed frame length = 70 bytes) shown in **Figure 129**.

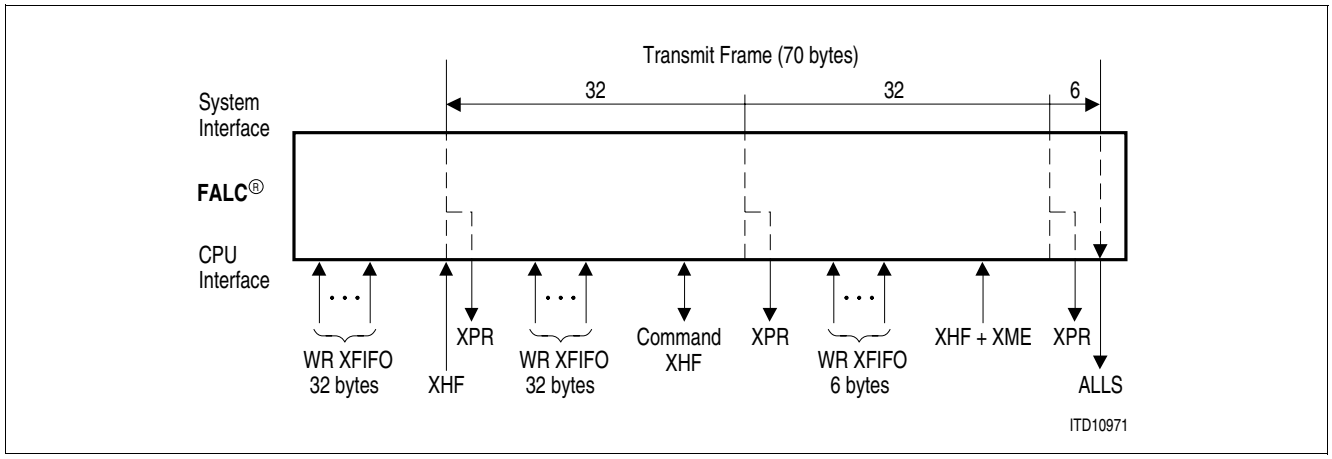


Figure 129 Interrupt Driven Transmission Example

12.3.5 HDLC Data Reception

Up to 2 x 64 byte FIFO buffers are also provided in receive direction for each HDLC channel. There are different interrupt indications concerned with the reception of data:

- RPF (RPF2, RPF3, receive pool full) interrupt, indicating that a 64-byte block of data can be read from RFIFO (RFIFO2, RFIFO3) and the received message is not yet complete.
- RME (RME2, RME3, receive message end) interrupt, indicating that the reception of one message is completed.

The following figure gives an example of a reception sequence, assuming that a “long” frame (66 bytes) followed by two short frames (6 bytes each) are received.

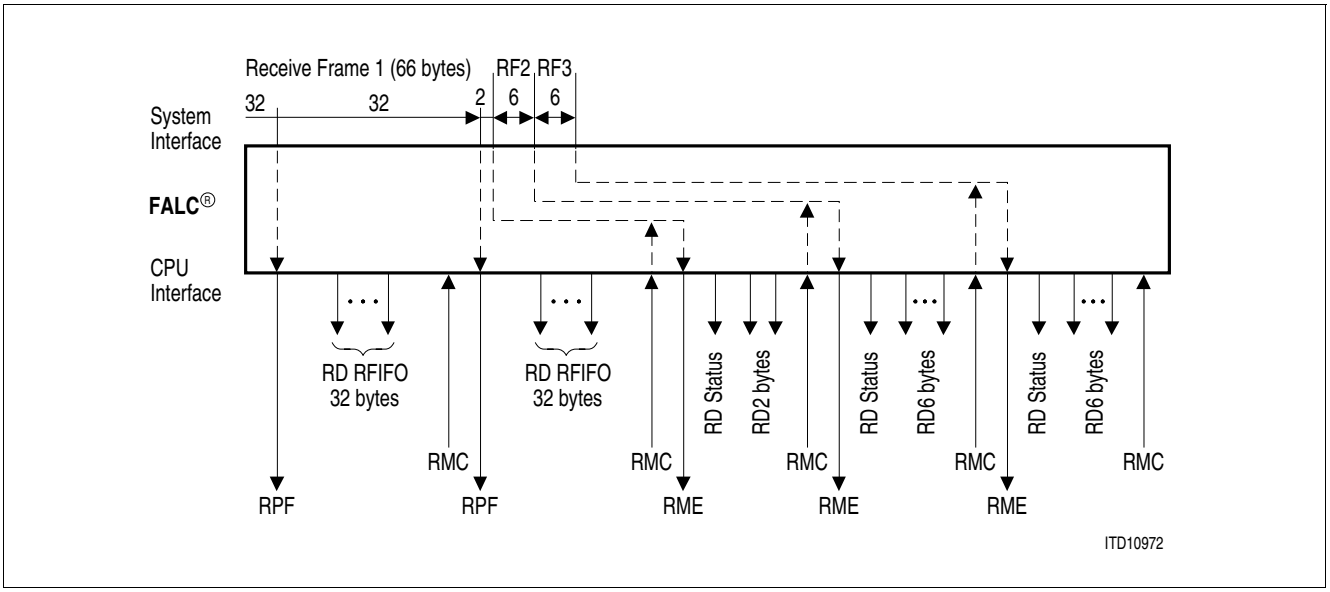


Figure 130 Interrupt Driven Reception Sequence Example

12.3.6 S_a-bit Access (E1)

The OctalFALC™ supports the S_a-bit signaling of time slot 0 of every other frame as follows:

- Access via registers RSW/XSW
- Access via registers RSA(8:4)/XSA(8:4) capable of storing the information for a complete multiframe
- Access via the 64 byte deep receive/transmit FIFO of the integrated signaling controller (HDLC channel 1 only). This Sa-bit access gives the opportunity to transmit/receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Enabling is done by setting of bit CCR1.EITS and resetting of registers TTR(4:1), RTR(4:1) and FMR1.ENSA. Data written to the XFIFO will be transmitted subsequently in the Sa-bit positions defined by register XC0.SA8E to SA84E and the corresponding bits of TSWM.TSA(8:4). Any combination of Sa-bits can be selected. After the data has been sent out completely an “all ones” or Flags (CCR1.ITF) is transmitted. The continuous transmission of a transparent bit stream, which is stored in the XFIFO, can be enabled. With the setting of bit MODE.HRAC the received Sa-bits can be forwarded to the receive FIFO. The access to and from the FIFOs is supported by ISR0.RME/RPF and ISR1.XPR/ALS.

12.3.7 Bit Oriented Message Mode (T1/J1)

The OctalFALC™ supports signaling and maintenance functions for T1/J1 primary rate Interfaces using the Extended Super Frame format. The HDLC channel 1 of the device supports the DL-channel protocol for ESF format according to T1.403-1989 ANSI or to AT&T TR54016 specification. The HDLC and Bit Oriented Message (BOM) -Receiver can be switched on/off independently. If the OctalFALC™ is used for HDLC formats only, the BOM receiver has to be switched off. If HDLC and BOM receiver has been switched on (MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. Storing of received DL-bit information in the RFIFO of the signaling controller and transmitting the XFIFO contents in the DL-bit positions is enabled by CCR1.EDLX/EITS = ´10_b´. After hardware-reset (pin $\overline{\text{RES}}$ low) or software-reset (CMDR.RRES = ´1´) the OctalFALC™ operates in HDLC mode. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the OctalFALC™ switches back to HDLC mode. Operating in BOM mode, the OctalFALC™ is able to receive an HDLC frame immediately, i.e. without any preceding flags.

In BOM mode, the following byte format is assumed (the left most bit is received first; ´111111110xxxxxx0_b´).

The OctalFALC™ uses the ´FF_H´ byte for synchronization, the next byte is stored in RFIFO (first bit received: LSB) if it starts and ends with a ´0´. Bytes starting and ending with a ´1´ are not stored. If there are no 8 consecutive ones detected within 32 bits, an interrupt is generated. However, byte sampling is not stopped.

Byte sampling in BOM Mode (T1/J1)

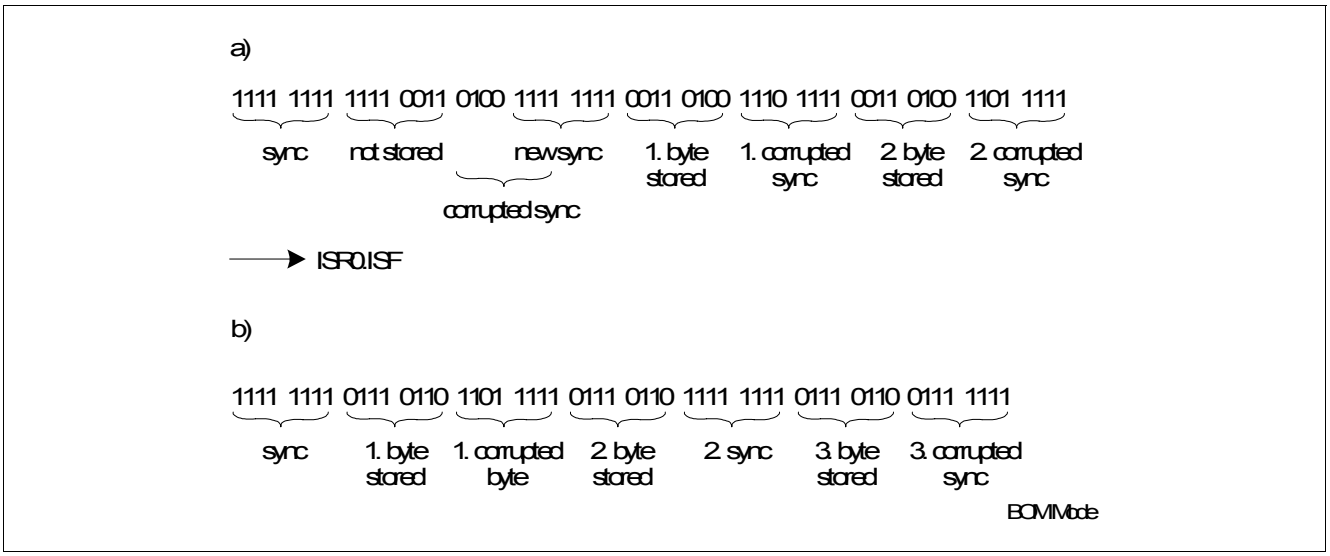


Figure 131 BOM Mode

Three different BOM reception modes can be programmed (CCR1.BRM, CCR2.RBFE).

10 Byte Packets

CCR1.BRM = ´0´

After storing 10 bytes in RFIFO the receive status byte marking a BOM frame (RSIS.HFR) is added as the eleventh byte and an interrupt (ISR0.RME) is generated. The sampling of data bytes continues and interrupts are generated every 10 bytes until an HDLC flag is detected.

Continuous Reception

CCR1.BRM = ´1´

Interrupts are generated every 64 (32, 16, 4, 2) bytes. After detecting an HDLC flag, byte sampling is stopped, the receive status byte is stored in RFIFO and an RME interrupt is generated.

Reception with enabled BOM filter: CCR2.RBFE = ´1´ The BOM receiver will only accept BOM frames after detecting 7 out of 10 equal BOM pattern. The BOM pattern is stored in the RFIFO adding a receive status byte, marking a BOM frame (RSIS.HFR) and generating an interrupt status ISR0.RME. The current state of the BOM receiver is indicated in register SIS.IVB. When the valid BOM pattern disappears an interrupt ISR0.BIV is generated.

The user can switch between these modes at any time. Byte sampling can be stopped by deactivating the BOM receiver (MODE.BRAC). In this case the receive status byte is added, an interrupt is generated and HDLC mode is entered. Whether the OctalFALC™ operates in HDLC or BOM mode are checked by reading the signaling status register (SIS.BOM).

13 Appendix

13.1 Protection Circuitry

The design in **Figure 132** shows an example of how to build up a generic E1/T1/J1 platform. The circuit shown has been successfully checked against ITU-T K.20 and K.21 lightning surge tests (basic level).

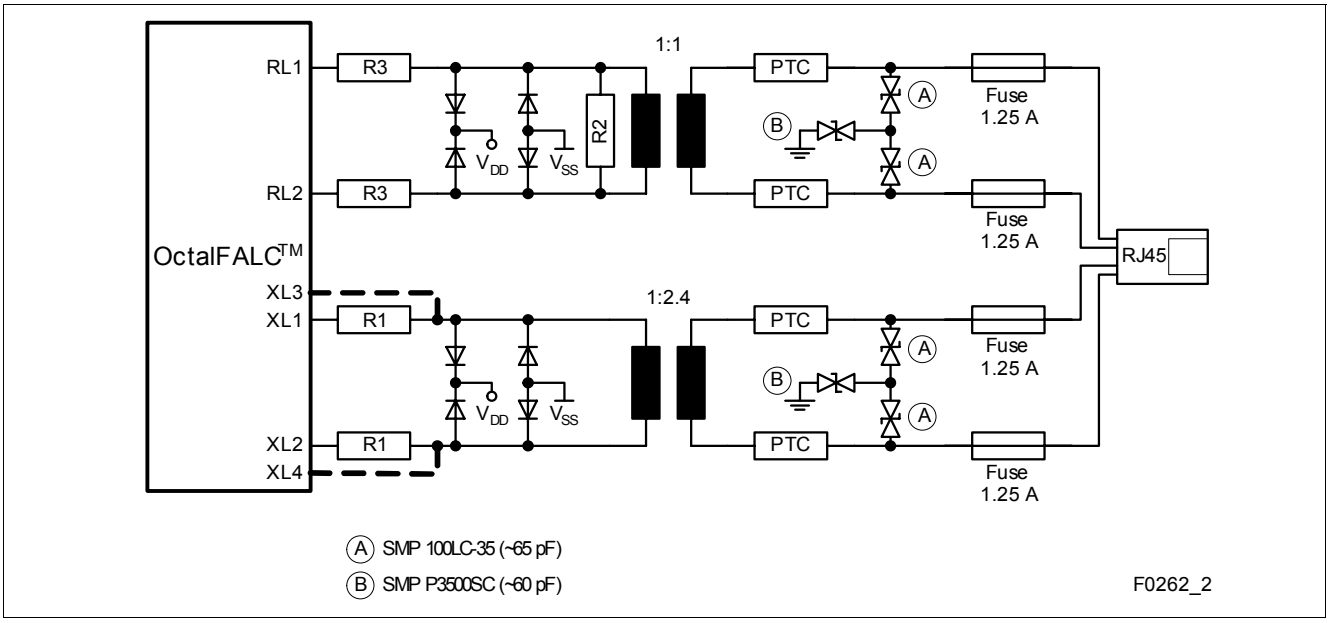


Figure 132 Protection Circuitry Examples (shown for one channel)

13.2 Application Notes

Several application notes and technical documentation provide additional information. Online access to supporting information is available on the internet page:

http://www.infineon.com/octalfalc

On the same page you find as well the

- Boundary Scan File for OctalFALC™ Version 1.1 (BSDL File)

13.3 Software Support

The following software package is provided together with the OctalFALC™ Reference System EASY 22558:

- E1 and T1 driver functions supporting different ETSI, AT&T and Telcordia (former: Bellcore) requirements. This driver software supports line attenuation up to 43 dB for E1.
- IBIS model for OctalFALC™ Version 1.1 (according to ANSI/EIA-656)
- “Flexible Master Clock Calculator”, which calculates the required settings for the registers GCM(1:8) depending on the external master clock frequency (MCLK)
- “External Line Front End Calculator”, which provides an easy method to optimize the external components depending on the selected application type. r

The both calculators run under a Win9x/NT environment. Calculation results are traced an can be stored in a file or printed out for documentation.

Screen shots of both programs are shown in **Figure 133** and **Figure 134** below.

Figure 133 Screen Shot of the “Master Clock Frequency Calculator”

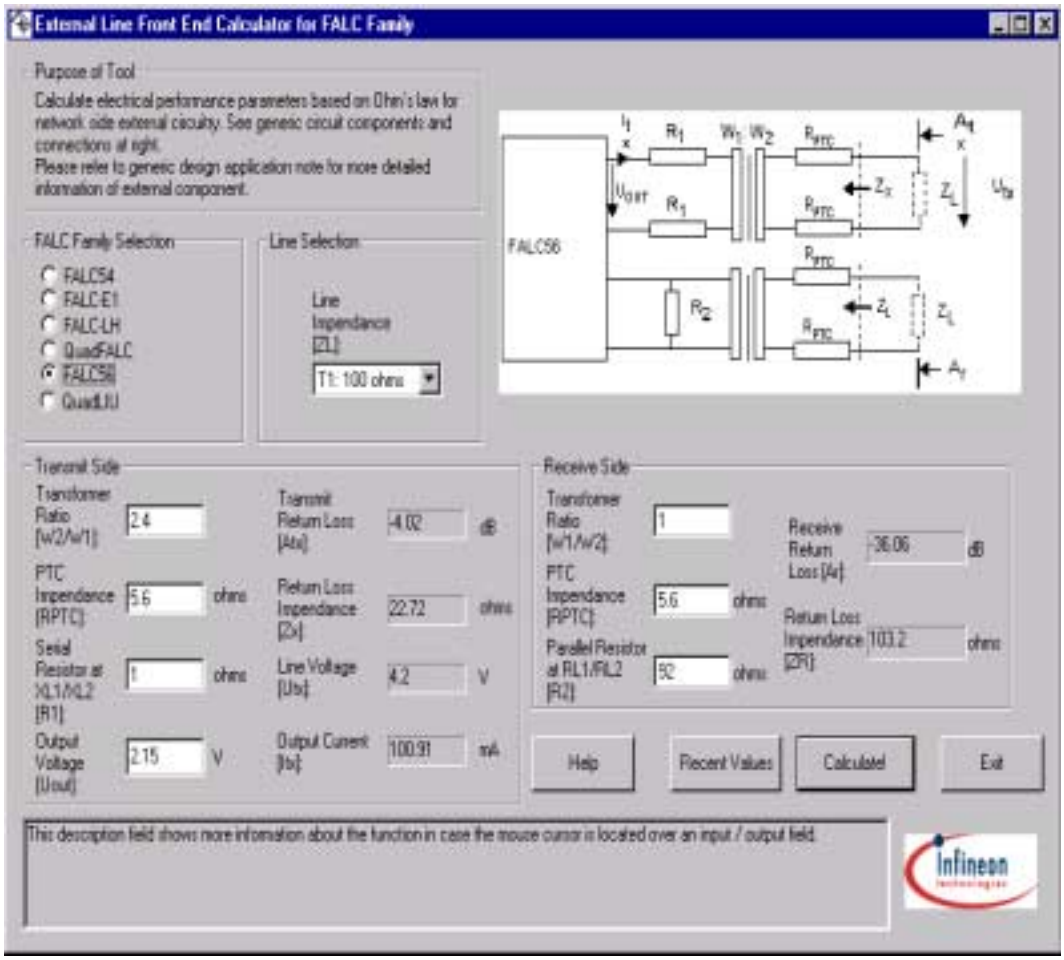


Figure 134 Screen Shot of the “External Line Frontend Calculator”

Terminology

A	
A/D	Analog to digital
ADC	Analog to Digital Converter
AIS	Alarm Indication Signal (blue alarm)
AGC	Automatic Gain Control
ALOS	Analog Loss Of Signal
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
ATM	Asynchronous Transfer Mode
AUXP	AUXiliary Pattern
B	
B8ZS	Binary 8 Zero Supression (Line coding to avoid too long strings of consecutive "0")
BEC	Bit Error Counter
BER	Bit Error Rate
BFA	Basic Frame Alignment
BOM	Bit Oriented Message (Out-band loop code)
Bellcore	Bell Communications Research
BPV	BiPolar Violation
BR	Bit-Robbing
BSN	Backward Sequence Number
C	
CAS	Channel Associated Signaling
CAS-BR	Channel Associated Signaling - Bit Robbing
CAS-CC	Channel Associated Signaling - Common Channel
CCS	Common Channel Signaling
CDR	Clock and Data Recovery
CIS	Channel Interrupt Status
CMI	Coded Mark Inversion code (also known as 1T2B code)
CR	Command/Response (special bit in PPR)
CRC	Cyclic Redundancy Check
CSU	Channel service unit
CVC	Code violation counter
D	
D/A	Digital to Analog
DAC	Digital to Analog Converter
DCIM	Digital Clock Interface Mode
DCO	Digitally Controlled Oscillator
DCO-R	DCO of receiver
DCO-X	DCO of transmitter
DL	Digital Loop
DPLL	Digitally controlled Phase Locked Loop

DS1	Digital Signal level 1
E	
EA	Extended Address (special bit in PPR)
ESD	ElectroStatic Discharge
EASY	Evaluation system for FALC products
ESF	Extended SuperFrame (F24) format
EQ	EQualizer
ETSI	European Telecommunication Standards Institute
F	
FALC®	Framing And Line interface Component
FAS	Frame Alignment Sequence
FCC	US Federal Communication Commission
FCS	Frame Check Sequence (used in PPR)
FEC	Frame Error Counter
FISU	Fill In Signaling Unit
FIFO	First In First Out buffer
FPS	Framing Pattern Sequence
FSN	Forward Sequence Number
G	
GIS	Global Interrupt Status
H	
HBM	Human body model for ESD classification
HDB3	High density bipolar of order 3
HDLC	High level Data Link Control
I	
IBIS	I/O buffer information specification (ANSI/EIA-656)
IBL	In Band Loop
ISDN	Integrated Services Digital Network
ITU	International Telecommunications Group
J	
JATT	Jitter ATTenuator
JTAG	Joined Test Action Group
L	
LAPD	Link Access Procedure on D-channel
LBO	Line Build Out
LCV	Line Code Violation
LIU	Line Interface Unit
LFA	Loss of Frame Alignment
LL	Local Loop
LLB	Line Loop Back
LOS	Loss of Signal (red alarm)
LSB	Least Significant Bit
LSSU	Link status signaling unit

M

MF	MultiFrame
MFP	Multi Function Port
MSB	Most Significant Bit
MSU	Message Signaling Unit
MUX	MUltipleXer

N

NRZ	Non Return to Zero signal

P

PCM	Pulse Code Modulation
PD	Pull Down resistor
PDV	Pulse Density Violation
PLB	Payload Loop Back
PLL	Phase Locked Loop
PMQFP	Plastic Metric Quad Flat Pack (device package)
PPR	Periodical Performance Report
PRBS	Pseudo Random Binary Sequence
PTQFP	Plastic Thin Metric Quad Flat Pack (device package)
PU	Pull Up resistor

R

RAI	Remote Alarm Indication (yellow alarm)
RAM	Random Access Memory
RDI	Remote Defect Indication
RL	Remote Loop
RLM	Receive Line Monitoring
ROM	Read-Only Memory
RX	Receiver

S

SAPI	Service Access Point Identifier (special octet in PPR)
SCI	Serial ControlInterface
SF	SuperFrame
SPI	Serial Peripheral Interface
SS7	Signaling System #7
Sidactor	Overvoltage protection device for transmission lines

T

TAP	Test Access Port
TEI	Terminal Endpoint Identifier (special octet in PPR)
TS	Time Slot
TX	Transmitter

U

UI	Unit Interval

Z

ZCS	Zero Code Suppression

Index

Index

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